CS2001

1.2 A Switching Regulator, and 5.0 V, 100 mA Linear Regulator with $\overline{\text{RESET}}$

The CS2001 is a smart power supply ASIC utilized in automotive airbag systems. It contains a current–mode switching regulator with a 1.2 A on–chip switch and a 5.0 V, 100 mA linear regulator. The linear output capacitor must be 3.3 μF or greater with an ESR in the range of 100 mΩ to 1.0 Ω. If the ESR of the cap is less than 100 mΩ, a series resistor must be used. The switcher can be configured in either a boost or flyback topology. The boost topology produces energy reserve voltage VER which is externally adjustable (25 V maximum) through the resistor divider connected to the V_{FB} pin. In the event of fault conditions that produce V_{FB} either open or shorted, the switcher is shut down.

Under normal operating conditions ($V_{BAT} > 8.0$ V), the current loading on the linear regulator is directed through V_{BAT}. A low battery or loss of battery condition switches the supply for the linear regulator from V_{BAT} to VER and shuts down the switcher using the ASIC's internal "smartswitch." This switchover feature minimizes the power dissipation in both the linear and switcher output devices and saves the cost of using a larger inductor.

The NERD (No Energy Reserve Detected) pin is a dual function output. If V_{OUT} is not in regulation, it provides a Power On Reset function whose time interval is externally adjustable with the capacitor. This interval can be seen on the RESETB pin, which allows for clean power–up and power–down of the microprocessor. Once V_{OUT} is in regulation, the logic level of the NERD output (usually low) indicates to the microprocessor whether or not the VER pin is connected.

A switched–capacitor voltage tripler accepts input voltage VER and produces output voltage V_{CHG} (typically VER + 8.0 V). This voltage is used in the system to drive high–side FETs.

This part is capable of withstanding a 50 V peak transient voltage. The linear regulator will not shut down during this event.
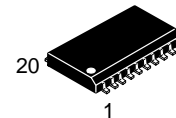
Features
- Linear Regulator 5.0 V ±2% @ 100 mA
- Switching Regulator 1.2 A Peak Internal Switch
- Voltage Tripler
- Smart Functions
  - Smartswitch
  - RESET
  - Energy Reserve Status
- Protection
  - Overtemperature
  - Current Limit
  - 50 V Peak Transient Capability
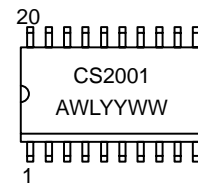- Internally Fused Leads in SO–20L Package
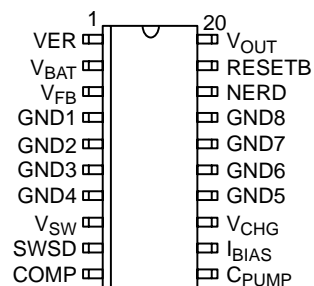

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**SO–20L
DWF SUFFIX
CASE 751D**

MARKING DIAGRAM

CS2001
AWLYYWW

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS

1		20
VER		V_{OUT}
V_{BAT}		RESETB
V_{FB}		NERD
GND1		GND8
GND2		GND7
GND3		GND6
GND4		GND5
V_{SW}		V_{CHG}
SWSD		I_{BIAS}
COMP		C_{PUMP}

ORDERING INFORMATION

Device	Package	Shipping
CS2001YDWF20	SO–20L	37 Units/Rail
CS2001YDWFR20	SO–20L	1000 Tape & Reel

December, 2000 – Rev. 5

CS2001
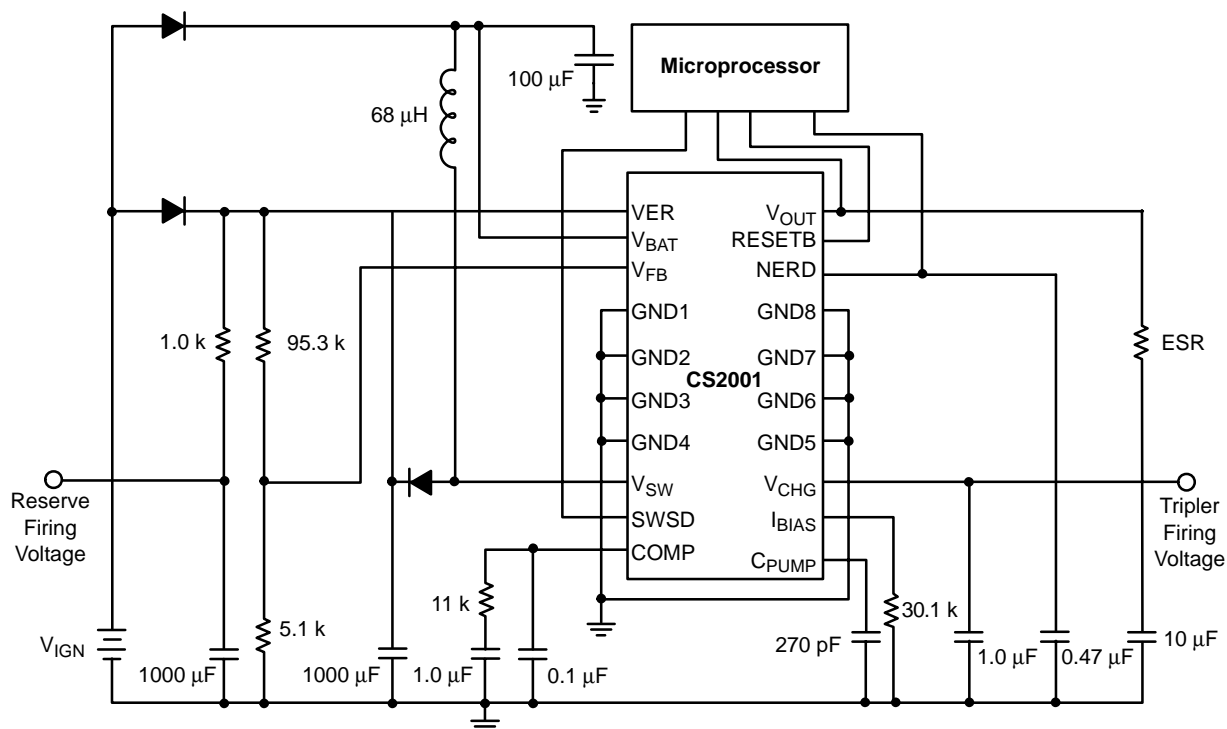
Figure 1. Application Diagram

ABSOLUTE MAXIMUM RATINGS*

Rating	Value	Unit
V$_{BAT}$	−0.5 to 25	V
VER	−0.5 to 25	V
V$_{OUT}$	−0.5 to 7.0	V
Digital Input/Output Voltage	−0.5 to 7.0	V
Peak Transient Voltage (36 V Load Dump @ 14 V Battery Voltage)	50	V
Storage Temperature Range	−55 to 150	°C
Junction to Free Air Thermal Impedance	55	°C/W
ESD Susceptibility (Human Body Model)	4.0	kV
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1.)	230 peak	°C
T$_A$	−40 to 85	°C
T$_J$	−40 to 150	°C

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

CS2001

ELECTRICAL CHARACTERISTICS (8.0 V ≤ V$_{BAT}$ ≤ 16 V, 8.0 V ≤ VER ≤ 25 V, 1.0 mA ≤ I$_{V(OUT)}$ ≤ 100 mA, T$_{TEST}$ = −40°C to 125°C; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Linear Regulator					
Output Voltage	Output Driven from V$_{BAT}$, VER = 25 V Output Driven from VER, V$_{BAT}$ = 0 V	4.9 4.9	– –	5.1 5.1	V V

Regulator Bias Current (from V$_{BAT}$)	I$_{V(BAT)}$ @ I$_{V(OUT)}$ = −100 mA,
	  SWSD = 4.0 V, V$_{BAT}$ = 16 V, VER = 25 V
	    T = −40°C
	    T = 25°C
	    T = 125°C
		
		–
		–
		–
			
			–
			–
			–
				
				8.0
				7.0
				6.0
					
					mA
					mA
					mA

Regulator Bias Current (from VER)	I$_{VER}$ @ I$_{V(OUT)}$ = −100 mA,
	  SWSD = 4.0 V, V$_{BAT}$ = 0 V, VER = 25 V
	    T = −40°C
	    T = 25°C
	    T = 125°C
		
		–
		–
		–
			
			–
			–
			–
				
				11
				9.0
				8.0
					
					mA
					mA
					mA

Dropout Voltage V$_{BAT}$ − V$_{OUT}$	VER = 25 V, I$_{V(OUT)}$ = −100 mA (Probe Only)	–	–	1.5	V
Dropout Voltage VER − V$_{OUT}$	V$_{BAT}$ = 0 V, I$_{V(OUT)}$ = −100 mA	–	–	1.5	V
Smart Switch Threshold V$_{BAT}$ to VER	VER = 25 V, I$_{V(OUT)}$ = −50 mA	6.5	–	8.0	V
Smart Switch Threshold Hysteresis	VER = 25 V, I$_{V(OUT)}$ = −50 mA	0.5	–	1.0	V
V$_{OUT}$ Output Noise	V$_{BAT}$ = 16 V, VER = 25 V, I$_{V(OUT)}$ = − 1.0 mA, C = 10 µF, ESR = 0.5 Ω	–	–	0.05	V
Line Regulation	–	–	–	0.025	V
Load Regulation	–	–	–	0.025	V
Output Current Limit	–	120	–	–	mA
Switching Regulator	**VER = 25V, I$_{V(OUT)}$ = −1.0 mA**				
Switching Frequency	C$_{PUMP}$ 270 pF, R$_{I(BIAS)}$ = 30.1 kΩ	135	150	165	kHz
Pump Drive Current	ΔI$_{V(BAT)}$ for 0 A ≤ I$_{V(SW)}$ ≤ 1.2 A	–	–	50	mA
Switch Saturation Voltage	I$_{V(SW)}$ = 1.2 A	–	–	1.6	V
Output Current Limit	–	1.2	–	2.4	A
V$_{FB}$ Regulation	–	1.238	1.27	1.303	V
V$_{FB}$ Input Current	V$_{FB}$ Above Short Low Detection Level	–	–	1.0	µA
V$_{FB}$ Input Shorted Low Detection Level	–	200	250	300	mV
C$_{PUMP}$ Short Detection Threshold	–	200	250	300	mV
Maximum Duty Cycle	–	80	–	95	%
V$_{SW}$ Leakage Current	I$_{V(SW)}$ @ V$_{SW}$ = 50 V, SWSD = V$_{OUT}$	–	–	100	µA
Voltage Tripler	**V$_{BAT}$ = 16 V, I$_{V(OUT)}$ = −1.0 mA, C$_{CHG}$ = 1.5 µF**				
Output Voltage Clamp V$_{CHG}$ − VER	VER = 8.0 V, I$_{V(CHG)}$ = −30 µA VER = 12 V, I$_{V(CHG)}$ = −90 µA	6.25 6.25	8.0 8.0	13 13	V V
Initial Charge Time	C$_{CHG}$ = 0.15 µF, VER = 8.0 V, V$_{CHG}$ = 14.25 V	–	–	30	ms
Maximum Output Voltage Clamp V$_{CHG}$	–	25	32.5	40	V
Output Voltage Clamp V$_{CHG}$	VER = 28 V, I$_{V(CHG)}$ = 0 µA	25	32.5	40	V
Short Circuit Path Current Limit VER to V$_{CHG}$	–	–	–	3.0	mA

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ELECTRICAL CHARACTERISTICS (continued) (8.0 V ≤ V_{BAT} ≤ 16 V, 8.0 V ≤ VER ≤ 25 V, 1.0 mA ≤ $I_{V(OUT)}$ ≤ 100 mA,
T_{TEST} = −40°C to 125°C; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
RESETB OUTPUT	**V_{BAT} = 0 V**				
High Threshold	V_{OUT} Increasing	4.525	4.75	4.85	V
Low Threshold	V_{OUT} Decreasing	4.5	4.65	4.825	V
Hysteresis	–	25	100	200	mV
Output Low Voltage	V_{OUT} = 1.0 V, I_{RESETB} = 100 µA I_{RESETB} = 1.0 mA, V_{OUT} = 4.5 V	– –	– –	0.5 0.5	V V
Pull–Up Resistor	RESETB = 1.0 V	25	50	100	kΩ
SWSD Input	**V_{BAT} = 16 V, VER = 25 V, $I_{V(OUT)}$ = −1.0 mA**				
High Threshold	–	–	–	$0.7 \times V_{OUT}$	V
Low Threshold	–	$0.3 \times V_{OUT}$	–	–	V
Input Impedance	Referenced to Ground	10	20	40	kΩ
NERD OUTPUT	**V_{BAT} = 16 V, $I_{V(OUT)}$ = −1.0 mA, C_{NERD} = 0.47 µF**				
VER Detection Voltage	–	1.5	–	6.5	V
Output Low Voltage	I_{NERD} = 1.0 mA, V_{OUT} = 4.5 V	–	–	0.5	V
Pull–Up Current	NERD = 0.5 V	30	40	50	µA
Power On Delay	–	6.25	8.5	11	ms
Clamping Voltage (Low)	VER Present	1.0	1.25	1.5	V
Clamping Voltage (High)	VER Not Present	3.5	3.75	4.0	V
General					
VER Load Current	VER = 25 V, V_{BAT} = 16 V, $I_{V(OUT)}$ = −100 mA T = −40°C T = 25°C T = 125°C	 – – –	 – – –	 5.0 5.0 4.0	 mA mA mA
Thermal Shutdown	(Guaranteed by Design)	160	–	210	°C

PACKAGE PIN DESCRIPTION

PACKAGE PIN # SO–20L	PIN SYMBOL	FUNCTION
1	VER	Energy reserve input.
2	V_{BAT}	Battery input.
3	V_{FB}	Charge PUMP control voltage input.
4	GND1	Ground.
5	GND2	Ground.
6	GND3	Ground.
7	GND4	Ground.
8	V_{SW}	Charge PUMP switch collector.
9	SWSD	Charge PUMP shutdown input.
10	COMP	Charge PUMP compensation pin.
11	C_{PUMP}	Charge PUMP timing cap input.
12	I_{BIAS}	Reference current resistor pin.

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PACKAGE PIN #		
SO–20L	PIN SYMBOL	FUNCTION
13	V_{CHG}	Switched cap voltage tripler output.
14	GND5	Ground.
15	GND6	Ground.
16	GND7	Ground.
17	GND8	Ground.
18	NERD	No energy reserve detected output.
19	RESETB	Reset output.
20	V_{OUT}	Linear regulator output.
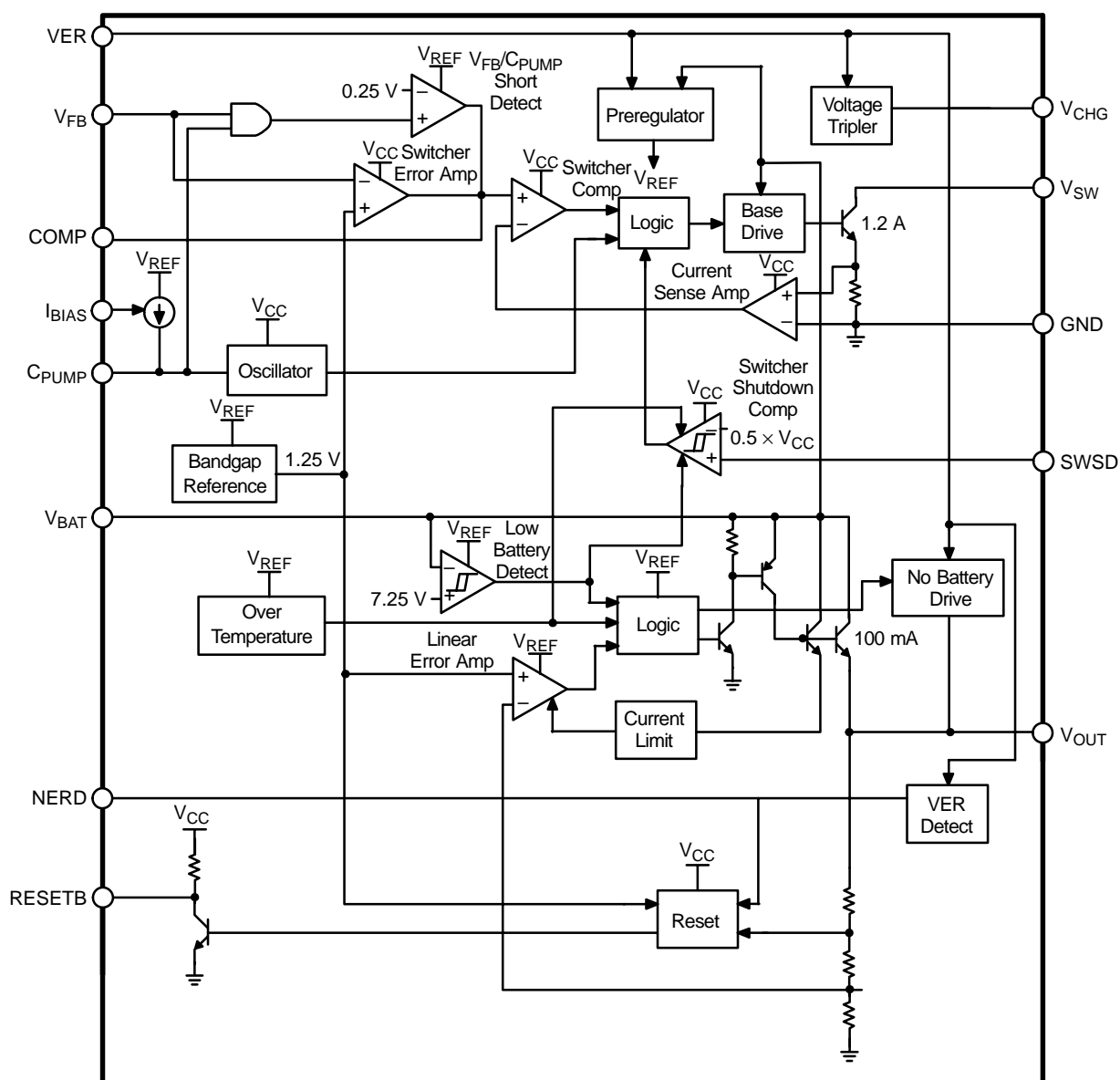
Figure 2. Block Diagram

CS2001

CIRCUIT DESCRIPTION

Figure 3 is an oscilloscope waveform showing the charge pump collector voltage, collector current and the charge pump timing capacitor during normal operation with I_{VER} = 30mA.
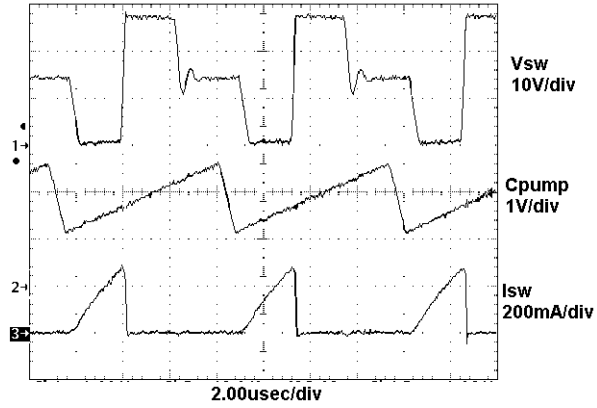
Figure 3. Typical Operation with I_{VER} = 30 mA

Figure 4 is an oscilloscope waveform showing the voltage tripler output and the energy reserve input during power up.
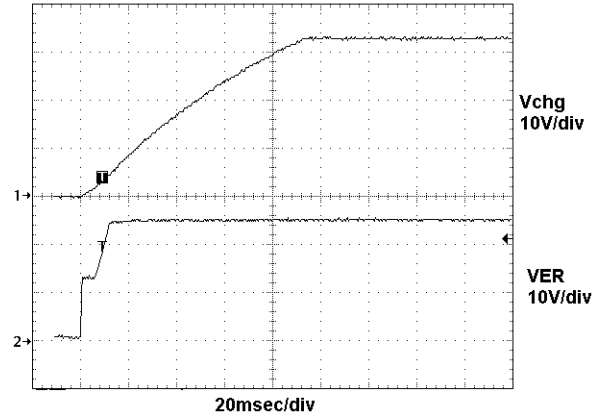
Figure 4. Startup with $R_{V(CHG)}$ = 510 k

CS2001

PACKAGE DIMENSIONS

SO–20L
DWF SUFFIX
CASE 751D–05
ISSUE F
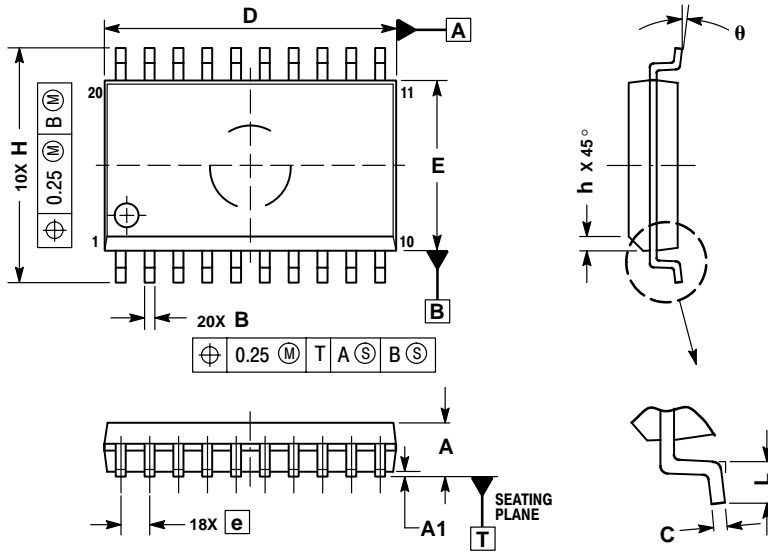
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

PACKAGE THERMAL DATA

Parameter		SO–20L	Unit
$R_{\Theta JC}$	Typical	9	°C/W
$R_{\Theta JA}$	Typical	55	°C/W

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