19-2189; Rev 1; 2/02

MAXIM

Low-Cost Integrated Offset Logic for Notebook CPU Power Supplies

General Description

The MAX1888 is a three-input decoder with three open-drain outputs. It is used with the MAX1718 or a similar DC-to-DC controller to offset the CPU core voltage in notebook computers. Designed to interface with low-voltage logic, the MAX1888 can program the controller for three independent offsets. The circuit is extremely low cost and is available in an 8-pin µMAX package.

Features

- ♦ **Simple, Low-Cost Offset Voltage Control for CPU Core Power Supplies**
- ♦ **IMVP II Logic Interface**
- ♦ **3V to 5.5V Supply Voltage**
- ♦ **Low 30µA (max) Supply Current**
- ♦ **8-Pin µMAX Package**

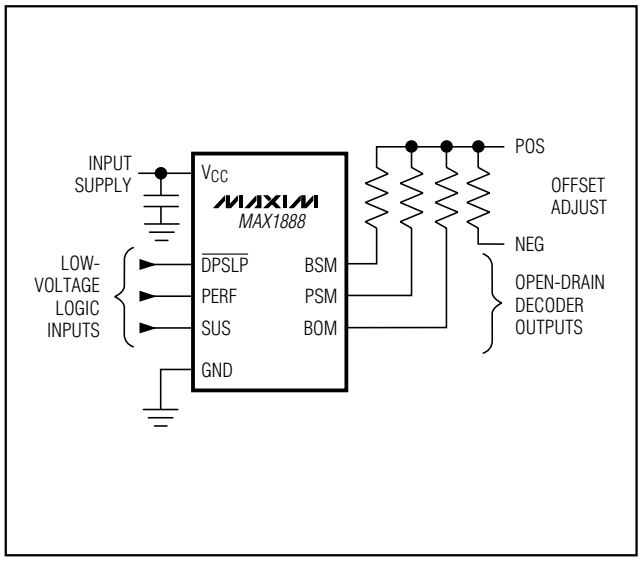
Applications

CPU Core Supplies for Intel IMVP II Notebook Computers

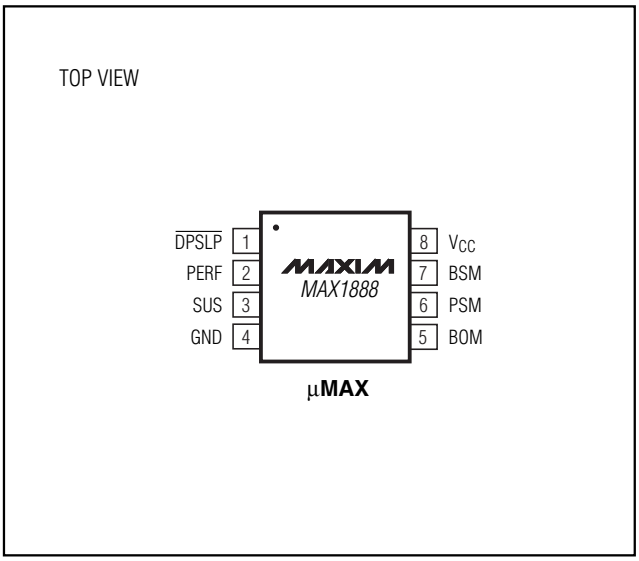
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1888EUA	-40°C to +85°C	8 µMAX

Minimal Operating Circuit



Pin Configuration



Low-Cost Integrated Offset Logic for Notebook CPU Power Supplies

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
PERF, SUS, $\overline{DPSLP}$, BOM, PSM, BSM to GND .....-0.3V to +6V
Continuous Power Dissipation
8-Pin µMAX (derate 4.5mW/°C above +70°C) 362.0mW
Extended Operating Temperature.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{CC} = +5V, T_A = -40°C to +85°C, unless otherwise noted.)

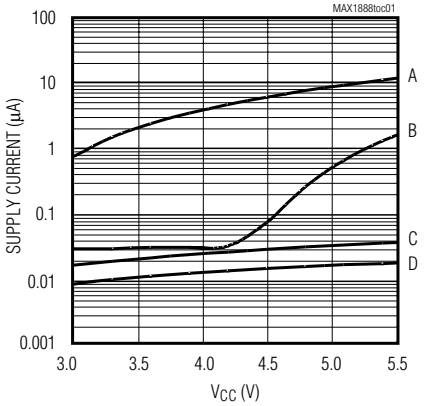
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY					
Supply Voltage Range (V_{CC})		3.0		5.5	V
BIAS					
Quiescent Supply Current (V_{CC})	All inputs = 0		< 0.01	1	µA
	All inputs = 1.5V		10	30	
LOGIC AND I/Os					
Logic Input High Voltage (PERF, SUS, $\overline{DPSLP}$), Hysteresis = 40mV (typ)	3V < V_{CC} < 5.5V	1.2			V
Logic Input Low Voltage (PERF, SUS, $\overline{DPSLP}$), Hysteresis = 40mV (typ)				0.4	V
	3V < V_{CC} < 5.5V			0.3	
Logic Input Current		-1		1	µA
Output On-Resistance (BOM, BSM, PSM)	I_{LOAD} = 5mA		20	50	Ω
	I_{LOAD} = 5mA, 3V < V_{CC} < 5.5V			100	
Output Leakage Current (BOM, BSM, PSM)	V(pin) = 5V		< 0.01	1	µA
DYNAMICS					
Propagation Delay	Falling edge, 1.5V to 0V step in 2ns		700		ns
	Rising edge, 0 to 1.5V step in 2ns		70		

Low-Cost Integrated Offset Logic for Notebook CPU Power Supplies

Typical Operating Characteristics

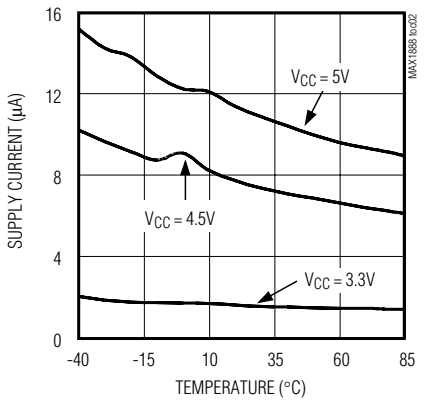
(Circuit of Figure 1, logic high = 1.5V, V_{OUT} = 1.3V, T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. SUPPLY VOLTAGE

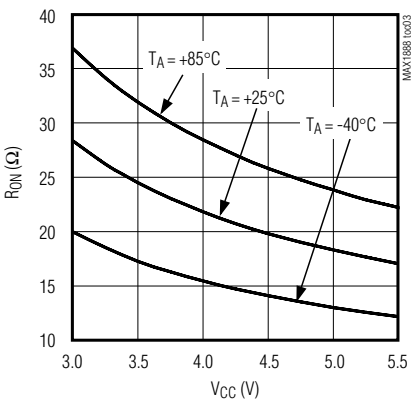


A = ALL INPUTS = 1.5V
B = ALL INPUTS = 3.3V
C = ALL INPUTS = 5V
D = ALL INPUTS = 0.4V

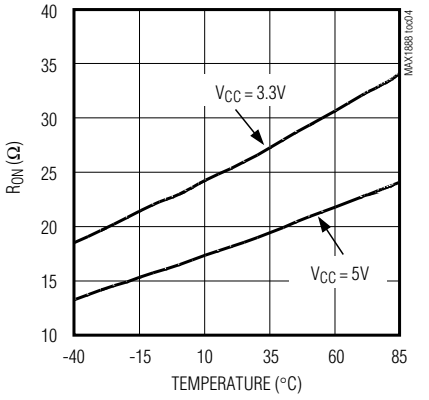
SUPPLY CURRENT vs. TEMPERATURE



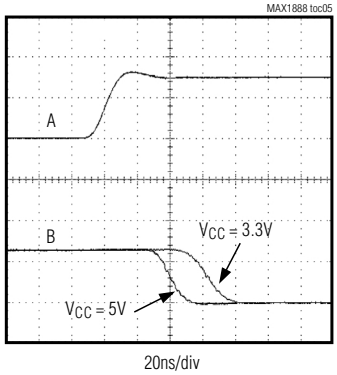
OUTPUT R_{ON} vs. SUPPLY VOLTAGE



OUTPUT R_{ON} vs. TEMPERATURE

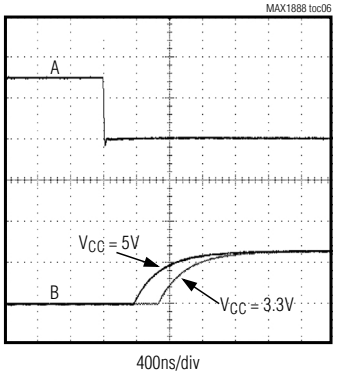


SWITCHING CHARACTERISTICS (OUTPUT TRANSITIONS INTO A 10kΩ LOAD)



A = V_{IN}, 1V/div
B = V_{OUT}, 1V/div

SWITCHING CHARACTERISTICS (OUTPUT TRANSITIONS INTO A 10kΩ LOAD)



A = V_{IN}, 1V/div
B = V_{OUT}, 1V/div

Pin Description

PIN	NAME	FUNCTION
1	$\overline{DPSLP}$	Deep-Sleep Mode Control Digital Input
2	PERF	Performance-Mode Offset Control Digital Input
3	SUS	Suspend-Mode (Deeper Sleep) Control Digital Input
4	GND	Ground
5	BOM	Open-Drain Output for Battery Operating Mode (BOM)
6	PSM	Open-Drain Output for Performance Sleep Mode (PSM)
7	BSM	Open-Drain Output for Battery Sleep Mode (BSM)
8	V_{CC}	Supply Voltage

Low-Cost Integrated Offset Logic for Notebook CPU Power Supplies

TTable 1. Truth Table

MODE	INPUTS			OUTPUTS		
	$\overline{\text{DPSLP}}$	PERF	SUS	BSM	PSM	BOM
Deeper Sleep	X	X	H	Hi-Z	Hi-Z	Hi-Z
Battery Sleep	L	L	L	L	Hi-Z	Hi-Z
Performance Sleep	L	H	L	Hi-Z	L	Hi-Z
Battery Operating	H	L	L	Hi-Z	Hi-Z	L
Performance	H	H	L	Hi-Z	Hi-Z	Hi-Z

Detailed Description

The MAX1888 is a three-input decoder with three open-drain outputs. It is used with the MAX1718 DC-to-DC controller to offset the CPU core voltage in notebook computers. The MAX1718 has two dedicated inputs (POS and NEG) that simplify the task of offsetting its output voltage. Specifically, the output voltage shifts by an amount equal to the difference between POS and NEG multiplied by a scale factor that depends on the DAC code (refer to the MAX1718 data sheet). The voltage between the POS and NEG inputs can be set with a programmable voltage-divider using the MAX1888 to connect the bottom resistor of the divider to ground (see Figure 1.)

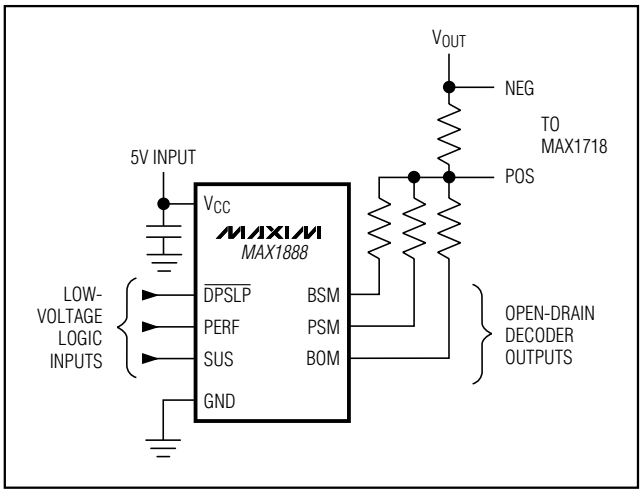


Figure 1. Simplified Application Circuit; Also Used for Obtaining Characterization Data; Offset Voltage is a Percentage of the Output Voltage.

Logic Characteristics

The Intel mobile processor specifications require independent offset to the CPU core voltage for battery sleep mode (BSM), performance sleep mode (PSM) and battery-operating mode (BOM). No offsets are required for the deeper-sleep mode ($\overline{\text{DPSLP}}$) and performance mode (PERF). Table 1 explicitly describes the logical operation of the decoder.

The decoder's inputs may come from system-level logic or directly from the CPU. To interface with low-voltage logic, the MAX1888's input logic thresholds are designed with an input-logic high voltage of 1.2V (min) and an input-logic low voltage of 0.3V (max). The logic inputs also include 40mV (typ) hysteresis to improve noise immunity.

The output on-resistance is guaranteed to be less than 100Ω over the entire supply voltage and temperature range. When loaded with a total pullup resistance greater than 10kΩ, the open-drain output resistance causes less than 1% error in impedance. If the offset voltage is set to 5% of the regulated output voltage, then the effect of the impedance error on the output voltage is approximately 0.05%, which is negligible in most applications.

The MAX1888 has rising- and falling-edge propagation delays of 70ns (typ) and 700ns (typ), respectively. Since transition times for CPU core voltage are typically much longer than these intervals, such delays are negligible. Note the time constant of the rising edge in the output voltage is set by the capacitance of the open-drain output transistor and the load impedance (see the *Typical Operating Characteristics*).

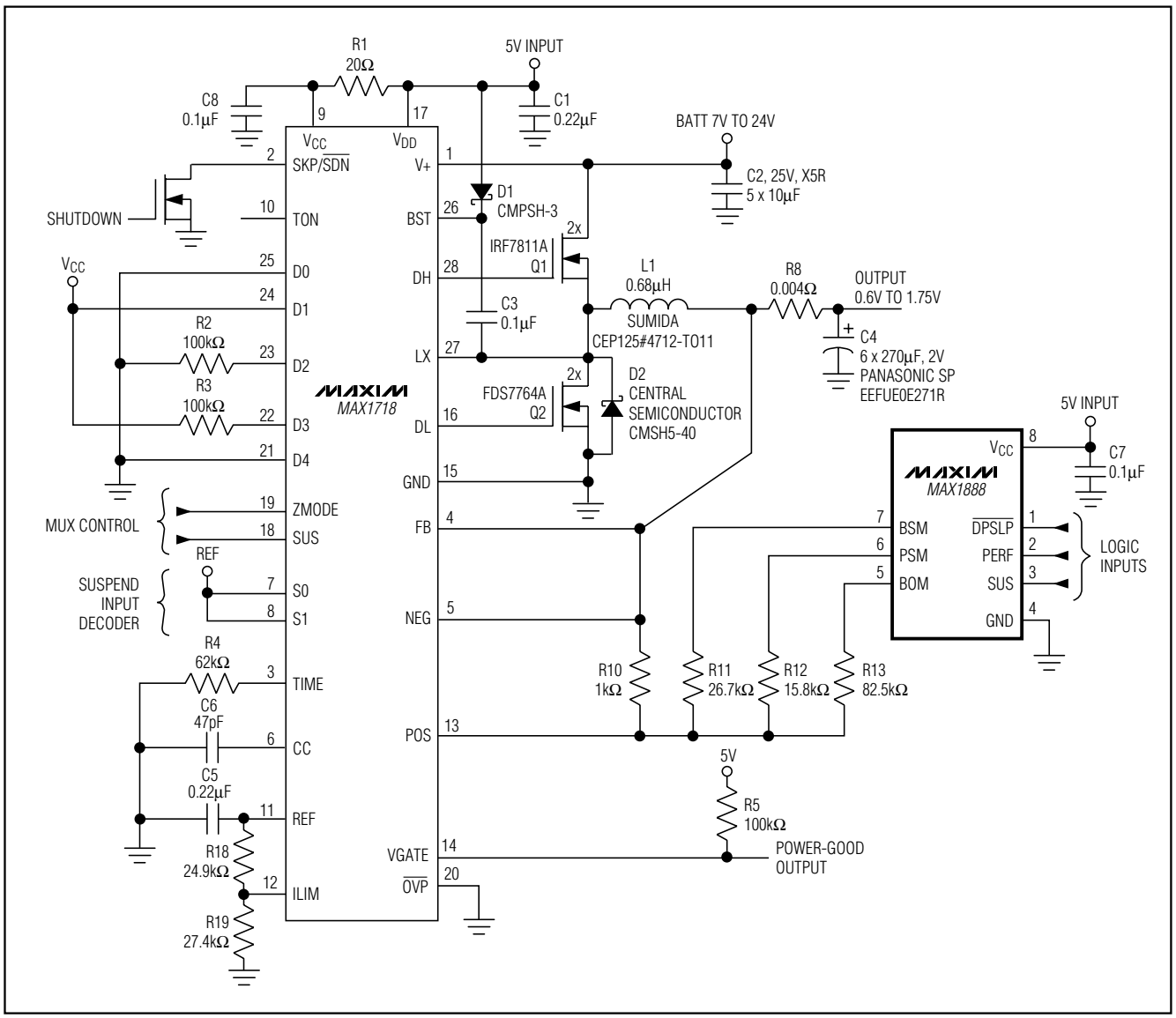


Figure 2. Typical Application Circuit

Low-Cost Integrated Offset Logic for Notebook CPU Power Supplies

Supply Current

The MAX1888 needs no shutdown control. The circuit consumes virtually no current ($I(V_{CC}) < 1\mu A$) when all the logic inputs are 0V, and less than 30µA when all the logic inputs are 1.5V. In general, the supply current increases with supply voltage and decreases with the logic input voltage. For a given supply voltage, the supply current decreases with temperature (see the *Typical Operating Characteristics*).

Applications Information

Figure 2 shows a typical CPU core supply application using the MAX1888 and the MAX1718. The voltage dividers are set to obtain negative offsets of 1%, 3%, and 5% of the output voltage for battery-operating mode (BOM), battery sleep mode (BSM), and performance sleep mode (PSM), respectively. The offset voltage is given by the following equation:

$$V_{OFFSET} = K\left(V_{POS} - V_{NEG}\right)$$

where K is the DAC code-dependent scale factor (refer to Table 3 in the MAX1718 data sheet). The offset voltage in each mode is:

$$V_{OFFSET,BOM} = -K\frac{R10}{R10 + R13}V_{OUT}$$

$$V_{OFFSET,BSM} = -K\frac{R10}{R10 + R11}V_{OUT}$$

$$V_{OFFSET,PSM} = -K\frac{R10}{R10 + R12}V_{OUT}$$

Note that divider ratio in each mode must be adjusted for a given DAC code. The circuit in Figure 2 assumes V_{OUT} = 1V with K = 0.84 and R10 = 1kΩ. The resulting values for R11, R12, R13 in the divider are 26.7kΩ, 15.8kΩ, and 82.5kΩ, respectively. Please note that these offsets are provided as an example only. Contact Intel for specific offset requirements.

The circuits in Figures 1 and 2 set the offset voltage as a percentage of the output voltage. Alternatively, the offset can be set as independent of the output voltage by biasing the POS and NEG inputs from a fixed reference voltage (see Figure 3).

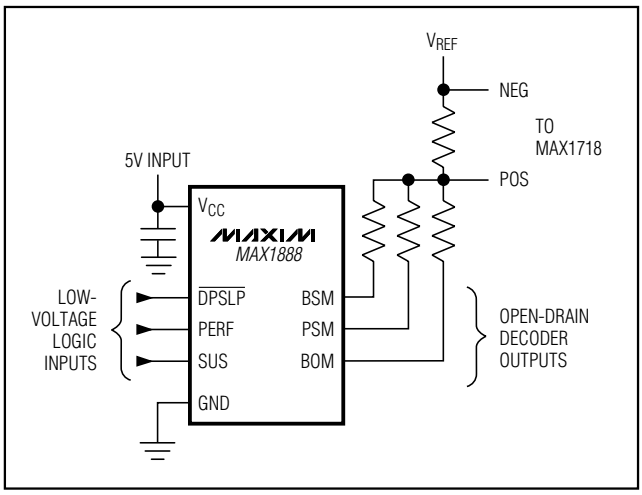


Figure 3. Using the MAX1888 to Set the Offset Voltage Independent of V_{OUT}

The MAX1888 can be inserted in the feedback path of any regulator to offset the output voltage. An external reference greater than the feedback set point is needed to affect negative offsets. The basic arrangement is shown in Figure 4.

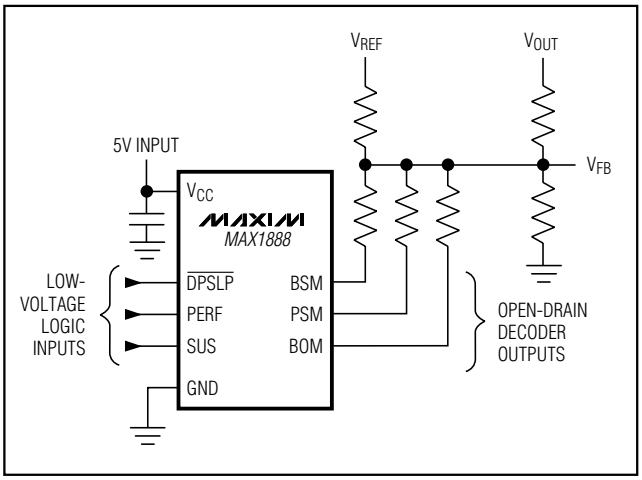


Figure 4. Inserting the MAX1888 into the Feedback Path of Any Regulator to Shift Output Voltage

Low-Cost Integrated Offset Logic for Notebook CPU Power Supplies

Layout Guidelines

Most applications do not drive the MAX1888 with high frequency signals with ultra-fast transition times. Therefore, the layout requirements are minimal. Keep the resistive voltage-divider traces away from noisy nodes and terminate the dividers through the MAX1888 to quiet analog ground. Place a 0.1µF decoupling capacitor close to the device.

Chip Information

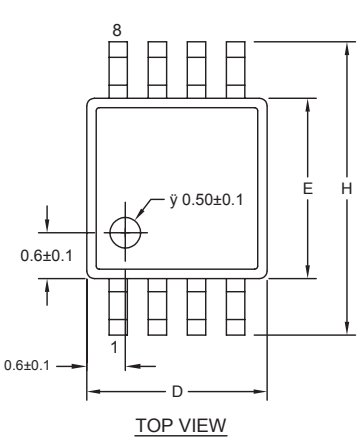
TRANSISTOR COUNT: 170

PROCESS: CMOS

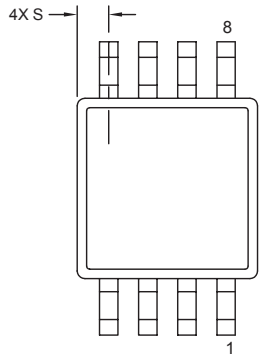
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

8LUMAXD.EPS

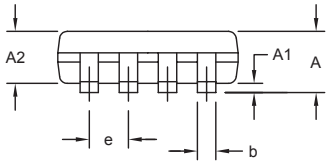


TOP VIEW

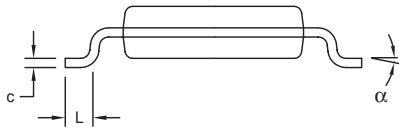


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1