NEW — EDO DRAM

DRAM

1 MEG x 4 DRAM

5V, EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

- Single +5V ±10% power supply
- JEDEC-standard pinout and packages
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN; optional Extended and SELF REFRESH modes
- Extended Data-Out (EDO) PAGE MODE access cycle
- 1,024-cycle Extended Refresh distributed across 16ms or 128ms
- EDO PAGE MODE cycle times, 25-35ns

OPTIONS	MARKING
• Timing	
60ns access	-6
70ns access	-7
• Refresh Rate	
Standard 16ms period	None
SELF REFRESH and 128ms period	S
• Packages	
Plastic SOJ (300 mil)	DJ

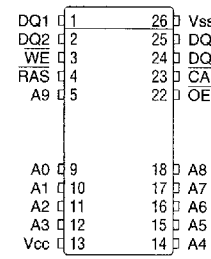
- Part Number Example: MT4C4007JDJ-7

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tCAS
-6	110ns	60ns	25ns	30ns	18ns	10ns
-7	130ns	70ns	33ns	35ns	22ns	15ns

PIN ASSIGNMENT (Top View)

20/26-Pin SOJ
(DA-1)



GENERAL DESCRIPTION

The MT4C4007J(S) is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration with optional SELF REFRESH. During READ or WRITE cycles, each of the 4 memory bits (1 bit per DQ) is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ latches the first 10 bits and $\overline{CAS}$ latches the latter 10 bits.

A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last, however, only EARLY WRITE cycles are supported. LATE WRITE cycles should not be attempted as the results are not predictable. When $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW (EARLY WRITE cycle), the output pins remain open (High-Z) until the next $\overline{CAS}$ cycle.

The four data inputs and four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

PAGE ACCESS

PAGE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A9) page boundary.

The PAGE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates PAGE operation.

EDO PAGE MODE

The MT4C4007J provides EDO PAGE MODE, which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ goes back HIGH. EDO provides for $\overline{CAS}$ precharge time (^tCP) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control provides for pipeline READs.

PAGE MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO

EDO PAGE MODE (continued)

operates as any DRAM READ or FAST-PAGE-MODE READ, except data will be held valid after $\overline{CAS}$ goes HIGH, as long as $\overline{RAS}$ and $\overline{OE}$ are held LOW and $\overline{WE}$ is held HIGH. $\overline{OE}$ can be brought LOW or HIGH while $\overline{CAS}$ and $\overline{RAS}$ are LOW, and the DQs will transition between valid data and High-Z. Using $\overline{OE}$, there are two methods to disable the outputs and keep them disabled during the $\overline{CAS}$ HIGH time. The first method is to have $\overline{OE}$ HIGH when $\overline{CAS}$ transitions HIGH and keep $\overline{OE}$ HIGH for ^{t}OEHC. This will tristate the DQs and they will remain tristate, regardless of $\overline{OE}$, until $\overline{CAS}$ falls again. The second method is to have $\overline{OE}$ LOW when $\overline{CAS}$ transitions HIGH. Then $\overline{OE}$ can pulse HIGH for a minimum of ^{t}OEP anytime during the $\overline{CAS}$ HIGH period and the DQs will tristate and remain tristate, regardless of $\overline{OE}$, until $\overline{CAS}$ falls again (please reference Figure 1 for further detail on the toggling $\overline{OE}$ condition). During cycles other than PAGE-MODE READ, the outputs are disabled at ^{t}OFF time after $\overline{RAS}$ and $\overline{CAS}$ are HIGH, or ^{t}WHZ after $\overline{WE}$ transitions LOW. The ^{t}OFF time is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last. $\overline{WE}$ can also perform the function of turning off the output drivers under certain conditions, as shown in Figure 2.

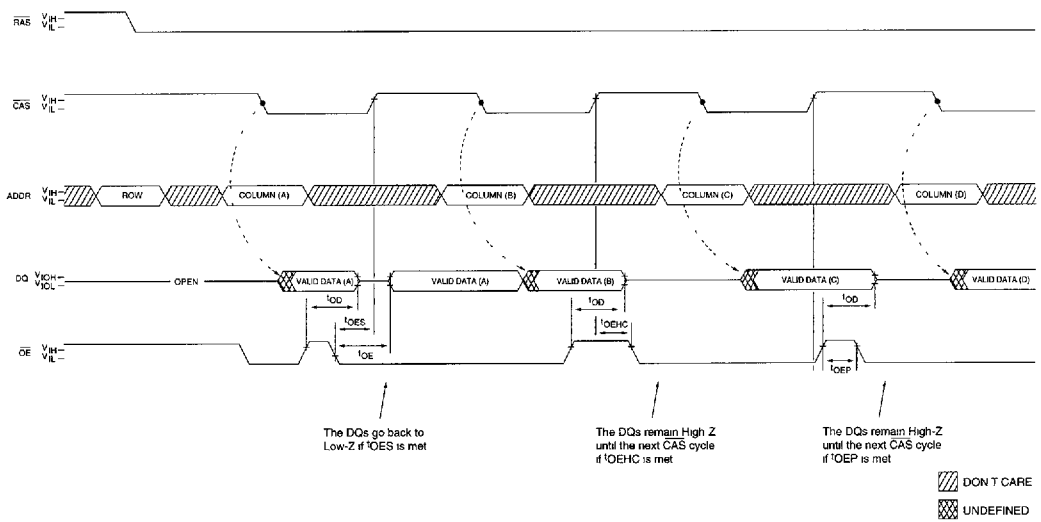


Figure 1
OUTPUT ENABLE AND DISABLE

REFRESH

Preserve correct memory cell data by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0-A9) are executed within ^{t}REF max, regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

An optional SELF REFRESH mode is also available on the MT4C4007J S. The "S" version allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding $\overline{RAS}$ LOW for the specified ^{t}RASS. Additionally, the "S" version allows for an extended refresh period of 128ms, or 125µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving $\overline{RAS}$ HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the $\overline{RAS}$ LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH. However, if the DRAM controller utilizes $\overline{RAS}$ ONLY or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time.

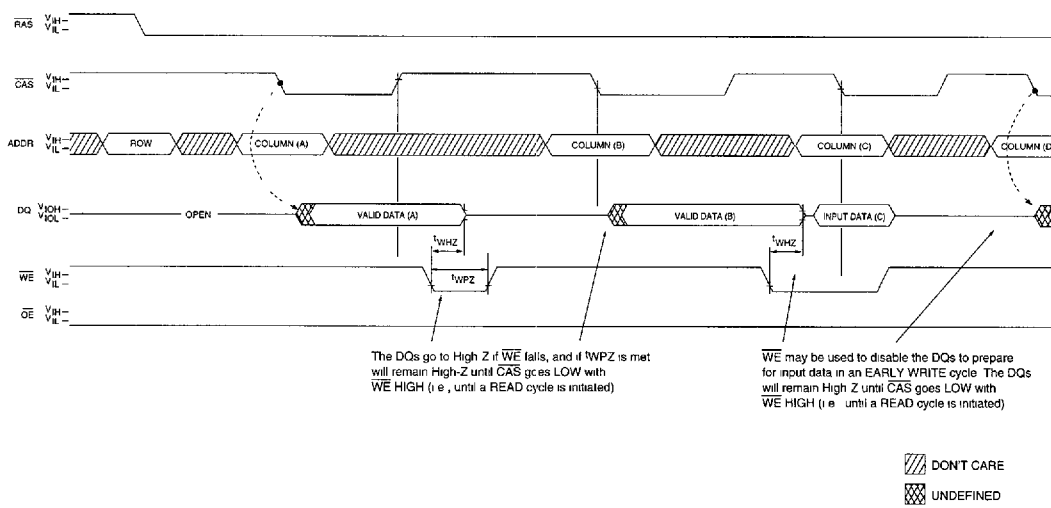
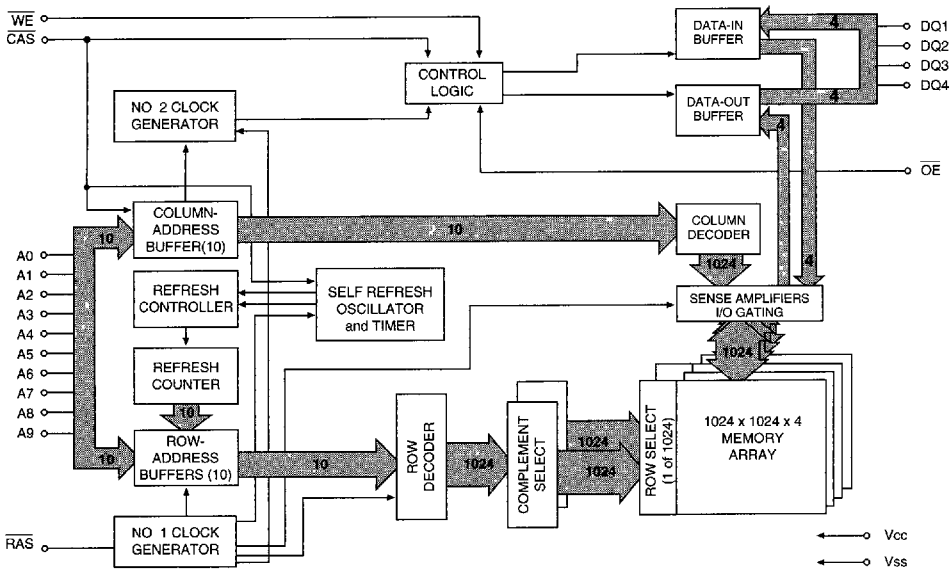


Figure 2
OUTPUT ENABLE AND DISABLE USING $\overline{WE}$

NEW — EDO DRAM

FUNCTIONAL BLOCK DIAGRAM
EDO PAGE MODE



TRUTH TABLE

FUNCTION		RAS	CAS	WE	OE	ADDRESSES tR	ADDRESSES tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
EDO-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss ..... -1.0V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)		I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)		I_{OZ}	-10	10	µA	
TTL OUTPUT LEVELS	High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
	Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	µA	
	I_{CC2} (S only)	200	200	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	110	100	mA	3, 4, 30
OPERATING CURRENT: EDO PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	80	70	mA	3, 4, 30
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	110	100	mA	3, 30
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	110	100	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current during Extended Refresh: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN); $\overline{WE}$= Vcc -0.2V; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open); ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7} (S only)	300	300	µA	3, 5, 28
REFRESH CURRENT: SELF (S version only) Average power supply current during SELF REFRESH: CBR cycle with $^tRAS \geq {}^tRASS$ (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = V_{CC} -0.2; A0-A9 and D_{IN} = Vcc -0.2V or 0.2V (D_{IN} may be left open)	I_{CC8} (S only)	300	300	µA	5, 29

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from column-address	^tAA		30		35	ns	
Column-address setup to $\overline{CAS}$ precharge during WRITE	^tACH	15		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	^tAR	45		50		ns	
Column-address setup time	^tASC	0		0		ns	
Row-address setup time	^tASR	0		0		ns	
Access time from $\overline{CAS}$	^tCAC		18		22	ns	15
Column-address hold time	^tCAH	10		15		ns	
$\overline{CAS}$ pulse width	^tCAS	10	10,000	15	10,000	ns	
$\overline{RAS}$ LOW to "don't care" during SELF REFRESH cycle	^tCHD	10		10		ns	28
$\overline{CAS}$ hold time (CBR REFRESH)	^tCHR	10		10		ns	5
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		ns	
Data output hold after $\overline{CAS}$ LOW	^tCOH	5		5		ns	
$\overline{CAS}$ precharge time	^tCP	10		10		ns	16
Access time from $\overline{CAS}$ precharge	^tCPA		35		40	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		ns	
$\overline{CAS}$ hold time	^tCSH	50		55		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^tCSR	10		10		ns	5
Write command to $\overline{CAS}$ lead time	^tCWL	15		20		ns	
Data-in hold time	^tDH	10		13		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^tDHR	45		55		ns	
Data-in setup time	^tDS	0		0		ns	22
Output disable	^tOD		15		20	ns	26
Output Enable time	^tOE		15		20	ns	23
$\overline{OE}$ HIGH hold time from $\overline{CAS}$ HIGH	^tOEHC	10		10		ns	
$\overline{OE}$ HIGH pulse width	^tOEP	10		10		ns	
$\overline{OE}$ LOW to $\overline{CAS}$ HIGH setup time	^tOES	5		5		ns	
Output buffer turn-off delay	^tOFF	3	15	3	20	ns	20
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	^tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	^tPC	25		33		ns	
Access time from $\overline{RAS}$	^tRAC		60		70	ns	14
$\overline{RAS}$ to column-address delay time	^tRAD	15	30	15	35	ns	18
Row-address hold time	^tRAH	10		10		ns	
Column-address to $\overline{RAS}$ lead time	^tRAL	30		35		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
$\overline{RAS}$ pulse width	^tRAS	60	10,000	70	10,000	ns	
$\overline{RAS}$ pulse width (EDO PAGE MODE)	^tRASP	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^tRASS	100		100		µs	28
Random READ or WRITE cycle time	^tRC	110		130		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	50	ns	17
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		ns	19
Read command setup time	^tRCS	0		0		ns	
Refresh period (1,024 cycles)	^tREF		16		16	ms	
Refresh period (1,024 cycles) S version	^tREF		128		128	ms	
$\overline{RAS}$ precharge time	^tRP	40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^tRPC	0		0		ns	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^tRPS	110		130		ns	28
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		0		ns	19
$\overline{RAS}$ hold time	^tRSH	15		20		ns	
Write command to $\overline{RAS}$ lead time	^tRWL	15		20		ns	
Transition time (rise or fall)	^tT	2	50	2	50	ns	9, 10
Write command hold time	^tWCH	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	^tWCR	45		55		ns	
$\overline{WE}$ command setup time	^tWCS	0		0		ns	21, 26
Output disable delay from $\overline{WE}$ ($\overline{CAS}$ HIGH)	^tWHZ	3	15	3	20	ns	
Write command pulse width	^tWP	10		15		ns	
$\overline{WE}$ pulse width for output disable when $\overline{CAS}$ HIGH	^tWPZ	10		10		ns	
$\overline{WE}$ hold time (CBR REFRESH)	^tWRH	10		10		ns	25
$\overline{WE}$ setup time (CBR REFRESH)	^tWRP	10		10		ns	25

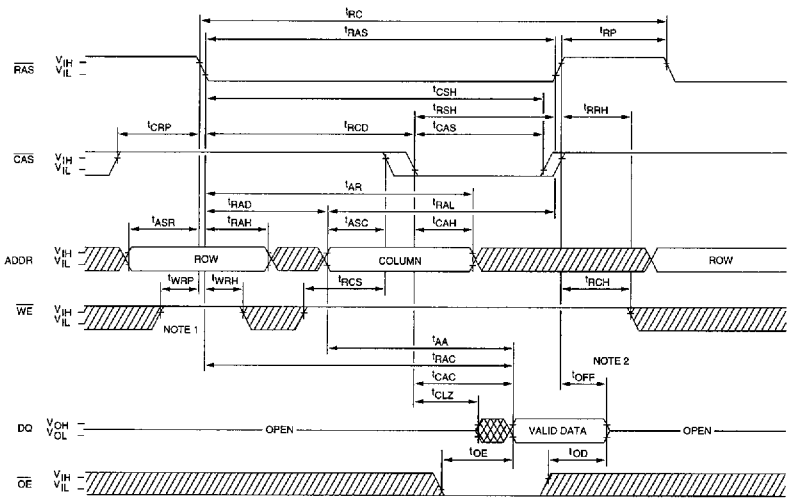
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +5V; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 2.5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCP.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. If the cycle is a READ-MODIFY-WRITE, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles.
23. Even if $\overline{OE}$ is HIGH, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. ^tWTS and ^tWTH are setup and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
26. The DQs open during READ cycles once ^tOD or ^tOFF occur.
27. Extended refresh current is reduced as ^tRAS is reduced from its maximum specification during the extended refresh cycle.
28. If the DRAM controller uses a burst refresh, a burst refresh of all rows must be executed upon exiting SELF REFRESH.
29. Column-address changed once each cycle.

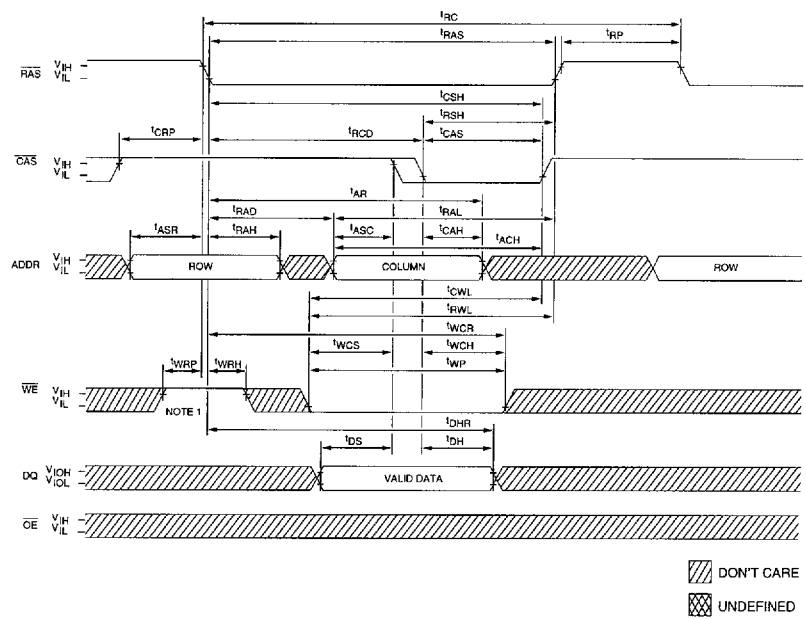
NEW

EDO DRAM

READ CYCLE

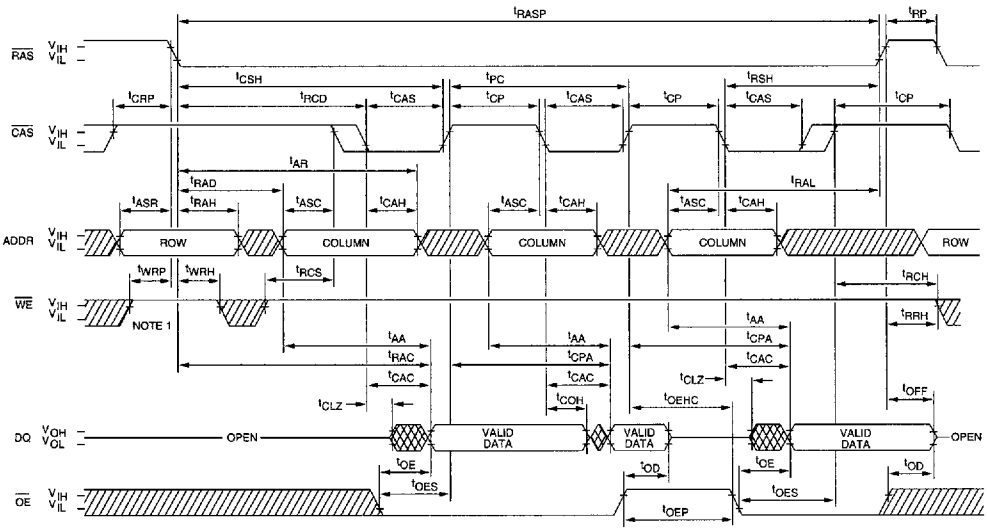


EARLY WRITE CYCLE

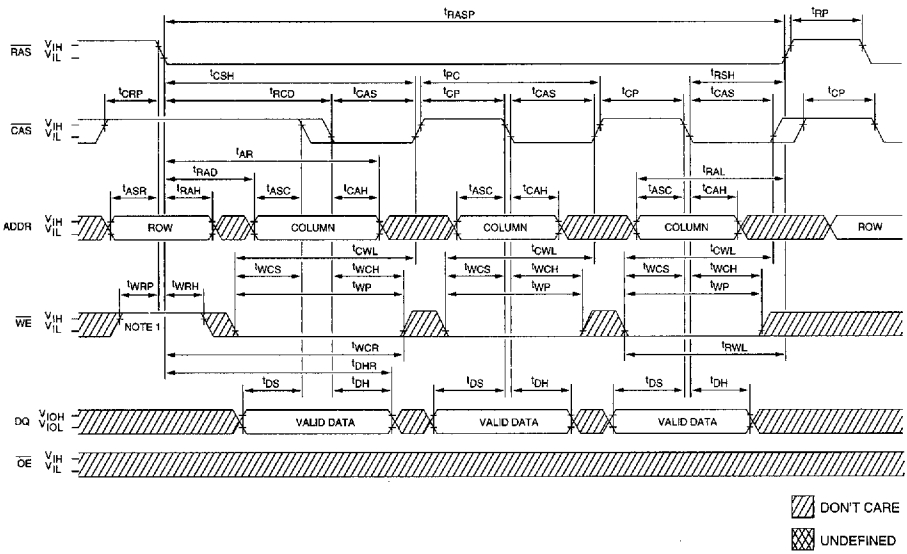


NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever occurs last.

EDO-PAGE-MODE READ CYCLE



EDO-PAGE-MODE EARLY-WRITE CYCLE

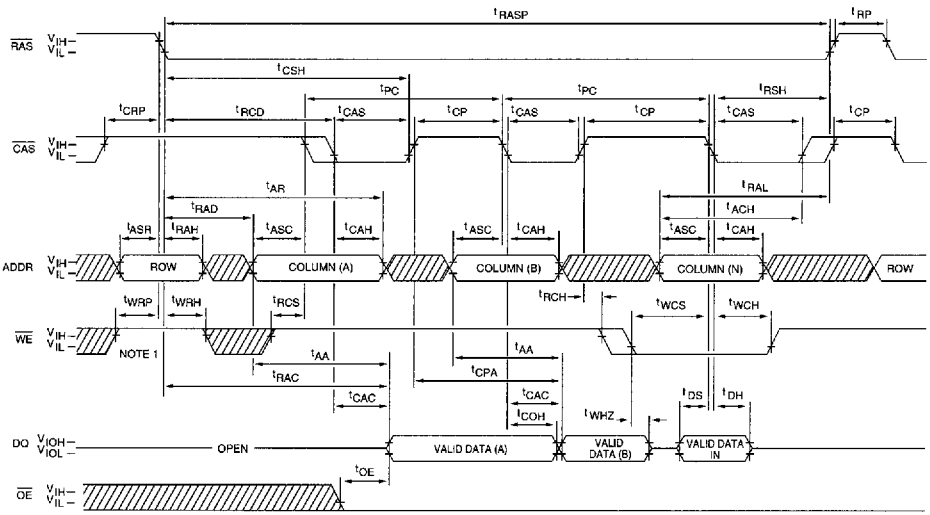


NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

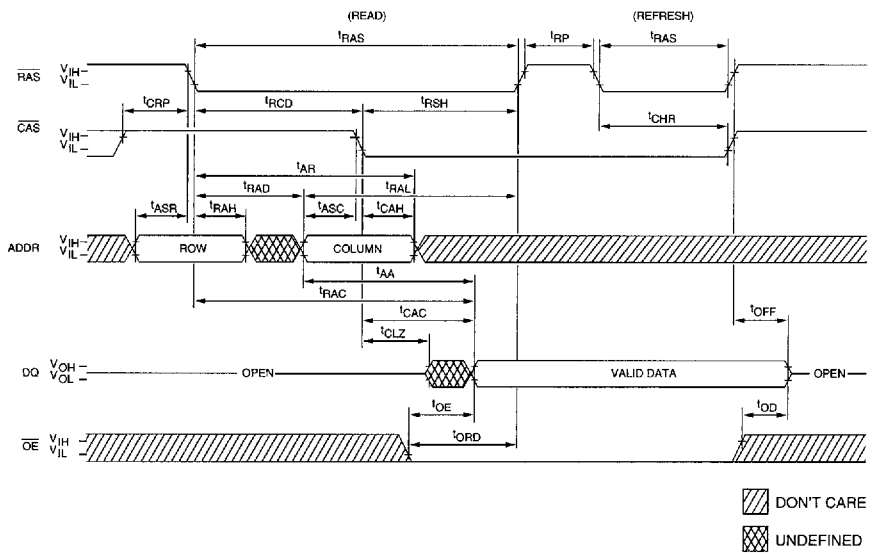
NEW

EDO DRAM

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



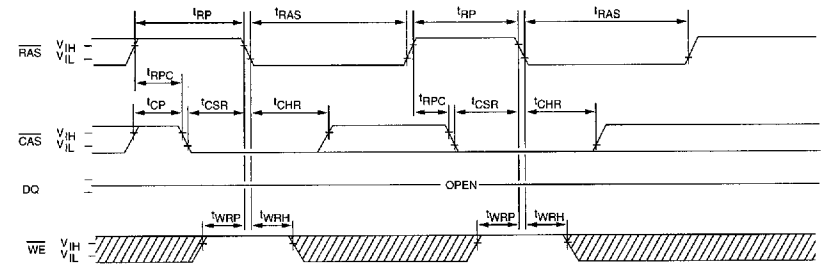
HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



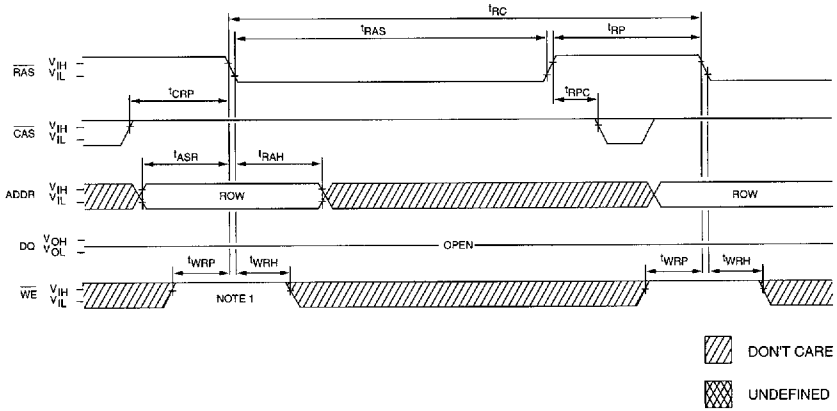
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

CBR REFRESH CYCLE

(Addresses and $\overline{OE}$ = DON'T CARE)



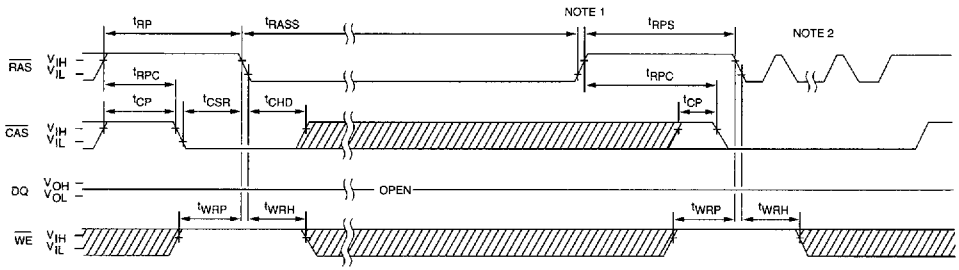
RAS-ONLY REFRESH CYCLE



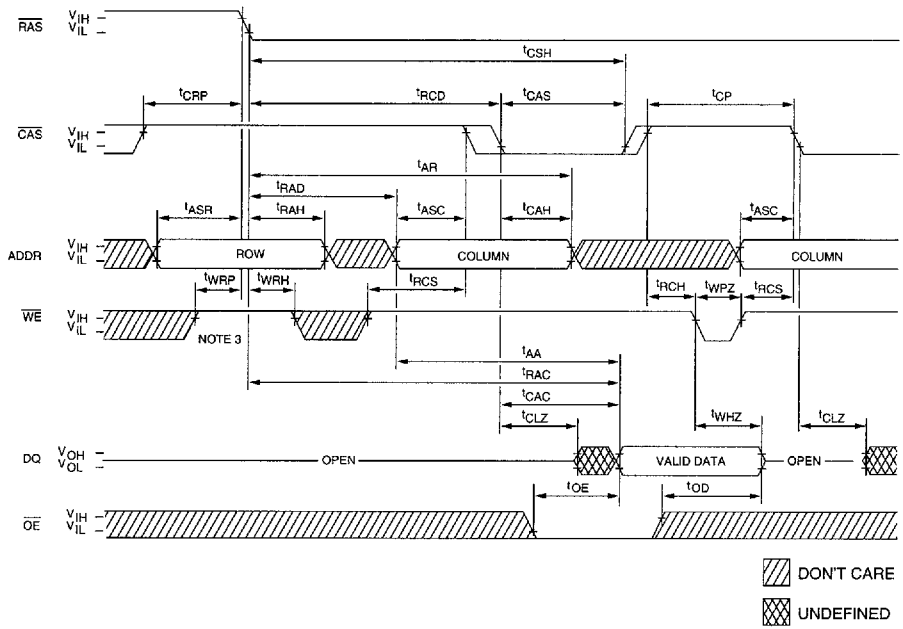
NOTE: 1. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

NEW EDO DRAM

SELF REFRESH CYCLE
(Addresses and $\overline{OE}$ = DON'T CARE)



READ CYCLE
(with $\overline{WE}$-controlled disable)



NOTE:
1. Once ^{t}RASS (MIN) is met and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once ^{t}RPS is satisfied, a complete burst of all rows should be executed.
3. Although $\overline{WE}$ is a "don't care" at $\overline{RAS}$ time during an access cycle (READ or WRITE), the system designer should implement $\overline{WE}$ HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.