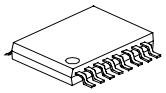
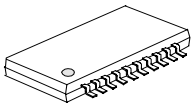
FET BIAS CONTROLLER WITH POLARISATION SWITCH AND TONE DETECTION



SSOP-16(150mil)



SSOP-20(150mil)

DESCRIPTION

The UTC L8115 is designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs, PMR, cellular telephones etc. with a minimum of external components.

With the addition of two capacitors and a resistor the devices provide drain voltage and current control for three external grounded source FETs, generating the regulated negative rail required for FET gate biasing whilst operating from a single supply. This negative bias, at -2.8 volts, can also be used to supply other external circuits.

The UTC L8115 includes bias circuits to drive up to three external FETs. A control input to the device selects either one of two FETs as operational, the third FET is permanently active. This feature is normally used as an LNB polarization switch. Also specific to Universal LNB applications is the 22kHz tone detection and logic output feature which is used to enable high and low band frequency switching.

Drain current setting of the UTC L8115 is user selectable over the range 0 to 15mA, this is achieved with addition of a single resistor. The UTC L8115 gives 2.2 volts drain whilst.

FEATURES

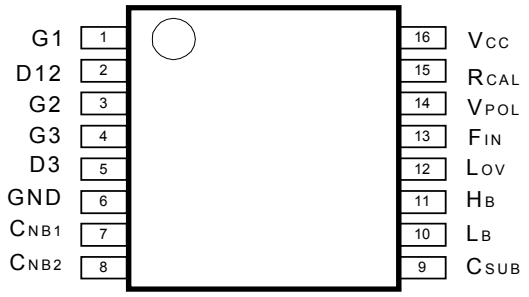
*Provides bias for GaAs and HEMT FETs.
*Drives up to three FETs.
*Dynamic FET protection.
*Drain current set by external resistor.
*Regulated negative rail generator requires only 2 external capacitors.
*Choice in drain voltage
*Wide supply voltage range
*Polarisation switch for LNBs
*22KHz tone detection for band switching.
*Tone detector ignores unwanted signals
*Support fr MIMIC, FET and Bipolar local oscillator devices

APPLICATIONS

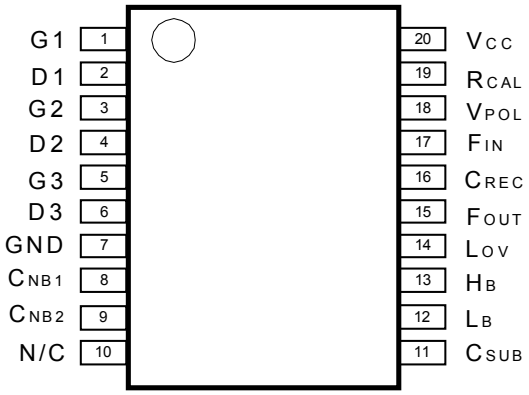
*Satellite receiver LNBs
*Private mobile radio(PMR)
*Cellular telephones

PIN CONFIGURATION

SSOP-16(150mil)



SSOP-20(150mil)



ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage		Vcc	-0.6 ~ 12	V
Supply Current		Icc	100	mA
Input Voltage		V_{IN}	25 Continuous	V
Drain Current (per FET)(set by R_{CAL})		I_D	0 ~ 15	mA
Power Dissipation(Ta=25℃)	SSOP-16(150mil)	P_D	500	mW
	SSOP-20(150mil)		500	mW
Operating Temperature		Topr	-40 ~ 80	℃
Storage Temperature		Tstg	-50 ~ 85	℃

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, Ta=25℃, Vcc=5V, I_D=10mA, R_{CAL}=33kΩ)

PARAMETER	SYMBOL	TEST CONDITONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	Vcc		5		10	V
Supply Current	Icc	I_{D1}= I_{D2} (or I_{D12})=I_{D3}=0		8.5	15	mA
		I_{D1}=0,I_{D2} (or I_{D12})= I_{D3}=10mA, V_{POL}=14V		28	35	mA
		I_{D2}=0,I_{D1} (or I_{D12})= I_{D3}=10mA, V_{POL}=15.5V		28	35	mA
		I_{D1} and I_{D3}=0, I_{LB}=10mA		18	25	mA
		I_{D1} and I_{D3}=0, I_{HB}=10mA		18	25	mA
Substrate Voltage	V_{SUB}	(Internally generated) I_{CSUB}=0	-3.05	-2.8	-2.55	V
		I_{CSUB}=-200 μA			-2.4	V
Output Noise						
Drain Voltage	E_{ND}	C_G=4.7nF,C_D=10nF			0.02	Vpkpk
Gate Voltage	E_{NG}	C_G=4.7nF,C_D=10nF			0.005	Vpkpk
Oscillator Frequency	fo		180	330	800	kHz

GATE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITONS	MIN.	TYP.	MAX.	UNIT
Output Current Range	I_{GO}		-30		2000	A
Output Voltage						
Gate 1 Off	V_{G1O}	I_{D1}=0mA, V_{POL}=14V, I_{GO1}=-10 μA	-2.5	-2.25	-2.0	V
Low	V_{G1L}	I_{D1}=12mA, V_{POL}=15.5V, I_{GO1}=-10 μA	-2.5	-2.25	-2.0	V
High	V_{G1H}	I_{D1}=8mA, V_{POL}=15.5V, I_{GO1}=0 μA	0.4	0.75	1.0	V
Output Voltage						
Gate 2 Off	V_{G2O}	I_{D2}=0mA, V_{POL}=15.5V, I_{GO2}=-10 μA	-2.5	-2.25	-2.0	V
Low	V_{G2L}	I_{D2}=12mA, V_{POL}=14V, I_{GO2}=-10 μA	-2.5	-2.25	-2.0	V
High	V_{G2H}	I_{D2}=8mA, V_{POL}=14V, I_{GO2}=0 μA	0.4	0.75	1.0	V
Output Voltage						
Gate 3 Low	V_{G3L}	I_{D3}=12mA, I_{GO3}=-10 μA	-3.0	-2.75	-2.0	V
High	V_{G3H}	I_{D3}=8mA, I_{GO3}=0 μA	0.4	0.75	1.0	V

DRAIN CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITONS	MIN.	TYP.	MAX.	UNIT
Current	I_D		8	10	12	mA
Current range	I_{Drng}	Set by R_{CAL}	0		15	mA
Current Change						
With Vcc	ΔI_{DV}	Vcc=5 ~ 10V		0.5		%/V
With Tj	ΔI_{DT}	Tj=-40 ~ +80℃		0.05		%/℃
Drain 1 Change: High	V_{D1}	I_{D1}=10mA,V_{POL}=15.5V	2.0	2.2	2.4	V
Drain 2 Change: High	V_{D2}	I_{D2}=10mA,V_{POL}=14V	2.0	2.2	2.4	V
Drain 3 Change: High	V_{D3}	I_{D3}=10mA,V_{POL}=15.5V	2.0	2.2	2.4	V
Voltage Change						
With Vcc	ΔV_{DV}	Vcc=5 ~ 10V		0.5		%/V
With Tj	ΔV_{DT}	Tj=-40 ~ +80℃		50		ppm
Leakage Current						
Drain 1	I_{L1} *	V_{D1}=0.5V,V_{POL}=14V			10	μA
Drain 2	I_{L2} *	V_{D2}=0.5V,V_{POL}=15.5V			10	μA

* FOR SSOP-20(150mil) package only.

TONE DETECTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITONS	MIN.	TYP.	MAX.	UNIT
Filter Amplifier Bias Voltage [5]	V_{OUT}	I_{FIN}=0	1.75	1.95	2.15	V
Input Impedance	Finz	V_{FIN}=100mV p/p		150		Ω
Amplifier Gain	AG	V_{FIN}=100mV p/p		30		V/mA
V Threshold [5]	FV_T		100	170	350	mVp/p
Output Stage Lov Volt.Range [6]	V_{Lov}	I_L=50mA(L_B or H_B)	-0.5		Vcc-1.8	V
Lov Bias Current	I_{LOV}	V_{LOV}=0	0.02	0.15	1.0	μA
L_B Output Low	V_{LBL}	V_{LOV}=0, I_L=0 Enabled [6] RIb-Csub=1MΩ	-3.05	-2.80	-2.55	V
		V_{LOV}=3V, I_L=0mA Enabled [6] RIb-Gnd=1MΩ	-0.01	0	0.1	V
L_B Output High	V_{LBH}	V_{LOV}=0, I_L=10mA Disabled [6]	-0.025	0	0.025	V
		V_{LOV}=3V ,I_L=50mA Disabled [6]	2.9	3.0	3.1	
H_B Output Low	V_{HBL}	V_{LOV}=0 ,I_L=0 Disabled [6] Rhb-Csub=1MΩ	-3.05	-2.80	-2.55	V
		V_{LOV}=3V, I_L=0mA Disabled [6] Rhb-Gnd=1MΩ	-0.01	0	0.1	V
H_B Output High	V_{HBH}	V_{LOV}=0, I_L=10mA Enabled [6]	-0.025	0	0.025	V
		V_{LOV}=3V, I_L=50mA Enabled [6]	2.9	3.0	3.1	

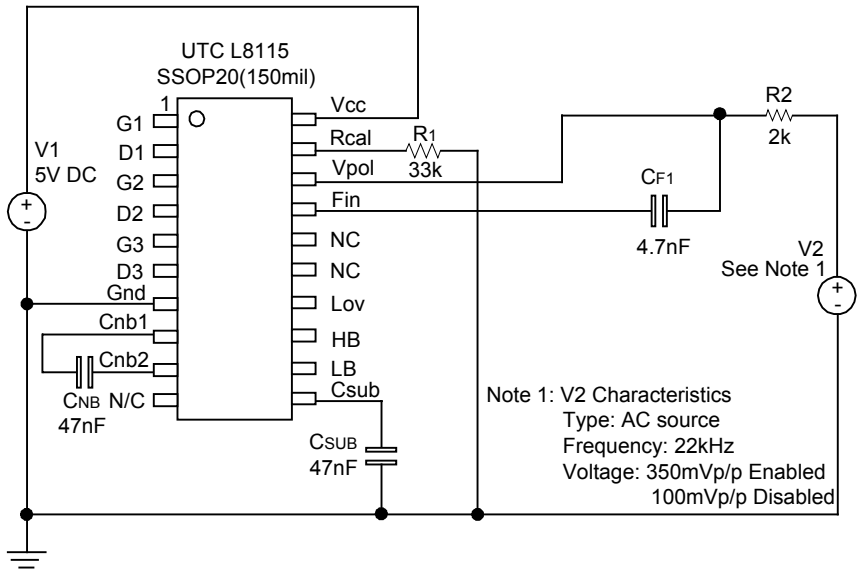
POLARITY SWITCH CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITONS	MIN.	TYP.	MAX.	UNIT
Input Current	I_{POL}	V_{POL}=25V (Applied via R_{POL}=2kΩ)	10	25	40	μA
Threshold Voltage	V_{TPOL}	V_{POL}=25V (Applied via R_{POL}=2kΩ)	14	14.75	15.5	V
Switching Speed	T_{SPOL}	V_{POL}=25V (Applied via R_{POL}=2kΩ)			100	ms

NOTES:

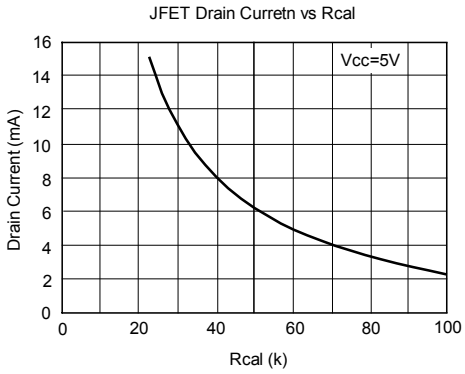
1. The negative bias voltages specified are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB}, of 47nF are required for this purpose.
2. The characteristics are measured using an external reference resistor R_{CAL} of value 33k wired from pins R_{CAL} to ground.
3. Noise voltage is not measured in production.
4. Noise voltage measurement is made with FETs and gate and drain capacitors in place on all outputs.C_G,4.7nF,are connected between gate output and ground,C_D,10nF,are connected between drain outputs and ground.
5. These parameters are linearly related to Vcc.
6. These parameters are measured using Test Circuit 1

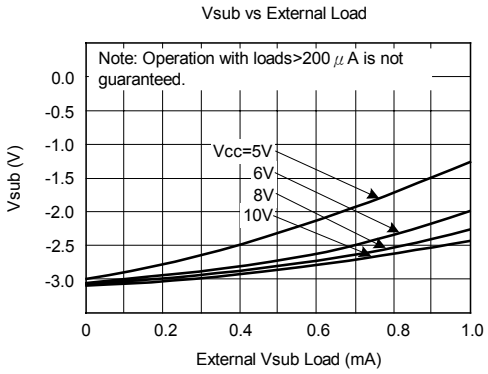
TEST CIRCUIT 1

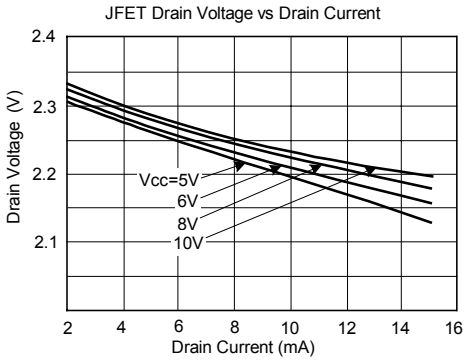


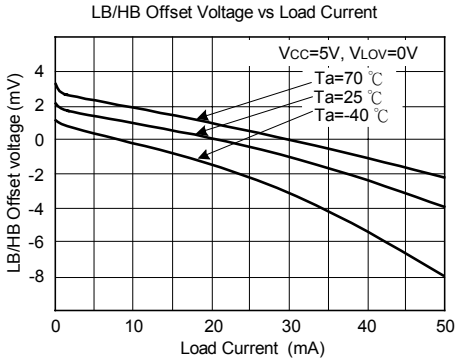
Note:Same circuit used for SSOP16(150mil) but with adjusted pinout.

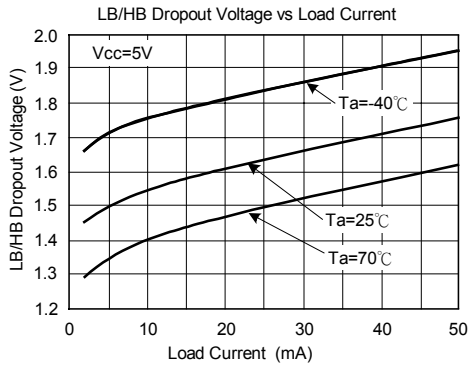
TYPCIAL CHARACTERISTICS



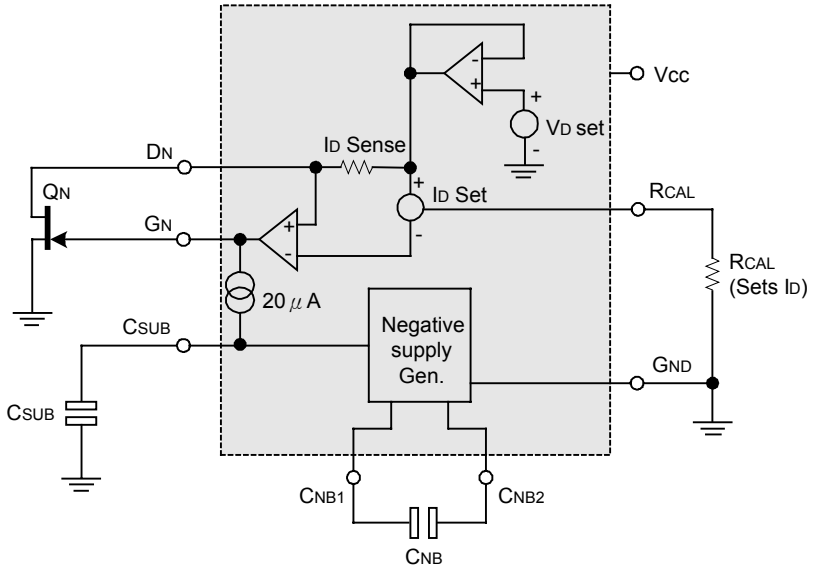








FUNCTIONAL DIAGRAM



FUNCTIONAL DESCRIPTION

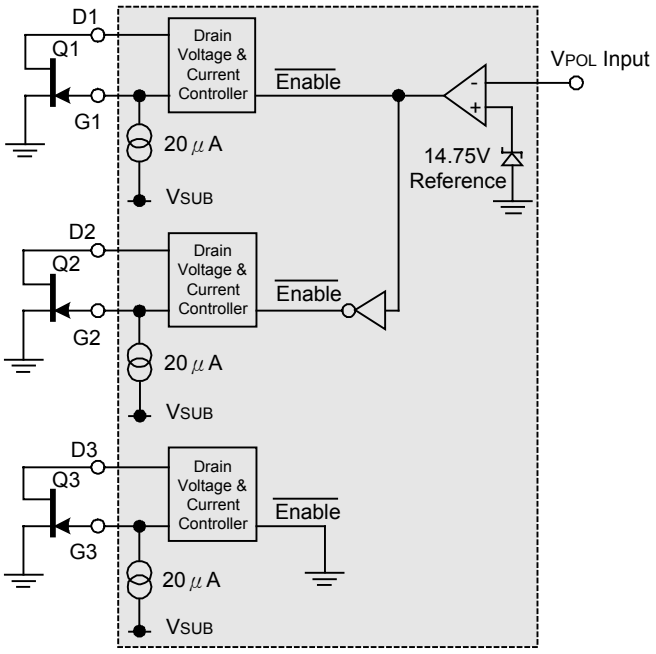
The UTC L8115 provides all the bias requirements for external FETs, including the generation of the negative supply required for gate biasing, from the single supply voltage.The diagram above shows a single stage from the UTC series. It contains 3 such stages. The negative rail generator is common to both devices.

The drain voltage of the external FET Q_N is set by the UTC L8115 to its normal operating voltage. This is determined by the on board V_D Set reference, the UTC L8115 this is nominally 2.2 volts whilst.

The drain current taken by the FET is monitored by the low value resistor I_D Sense. The amplifier driving the gateof the FET adjusts the gate voltage of Q_N so that the drain current taken matches the current called for by an external resistor R_{CAL}.

Since the FET is a depletion mode transistor, it is often necessary to drive its gate negative with respect to groundto obtain the required drain current. To provide this capability powered from a single positive supply, the deviceincludes a low current negative supply generator. This generator uses an internal oscillator and two external capacitors, C_{NB} and C_{SUB}.

The following schematic shows the function of the V_{POL} input. Only one of the two external FETs numberd Q1 and Q2 are powered at any one time,their selection is controlled by the input V_{POL}.This input is designed to be wired to the power input of the LNB via a high value(10k) resistor.With the input voltage of the LNB set at or below 14V,.FET Q2 will be enabled.With the input voltage at or above 15.5V,FET Q1 will be enabled.The disabled FET has its gate driven low and its drain terminal is switched open circuit. It is permissible to commect the drain pins D1 and D2 together if required by the application circuit;this is done internally in the SSOP-16(150mil) version.FET number Q3 is always active regardless of the voltage applied to V_{POL}.



For SSOP-20(150mil) Package

Control Input Switch Function

Input sense	Polarisation	Select
≤14 volts	Vertical	FET Q2
≥15.5 volts	Horizontal	FET Q1

For many LNB applications, tone detection for band switching is required. The UTC L8115 includes all the circuitry necessary to detect the presence of a 22kHz tone modulated on the supply input to the LNB. The main elements of the detector are an op-amp, a rectifier/smoother and a comparitor. The op-amp has a pre-set internal feedback resistor so that just a simple RC network wired to the input gives user defined gain and low frequency cut filter characteristics. The RC network components also serve two other purposes. The resistor provides overvoltage protection for the Vpol pin and the capacitor minimises tone interference of the Vpol threshold. The upper frequency roll-off of the op-amp has been set internally at above 100kHz to allow the amplifier to be used with other common tone switch frequencies.

The rectifier/smoother/comparitor function is provided by a complex propriety circuit that allows the UTC L8115 to reliably detect wanted tones whilst ignoring low frequency square wave switch box signals, DiSEqC™ bursts and supply switching transients common when using DiSEqC-2™ ready set-top boxes. This is all achieved without the need for any further external components. The threshold of the comparitor is supply dependent, hence the gain of the preceding op-amp must be adjusted in line with supply voltage. See the table below for recommended values for 22kHz detection, given for a range of supplies.

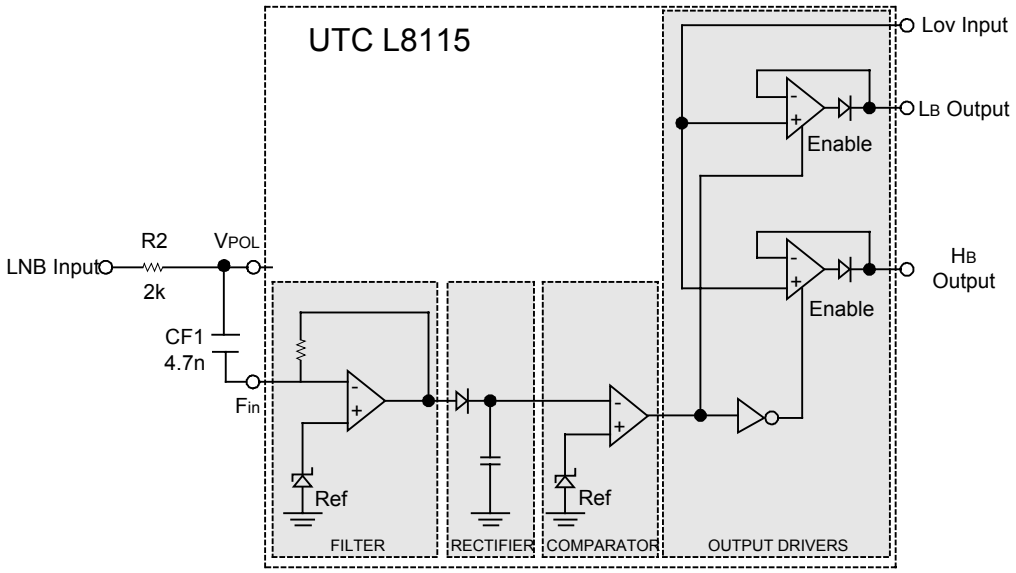


Table_1

Filter Components	Supply Voltage (Vcc)					
	5V	6V	7V	8V	9V	10V
Cf	4.7nF	4.7nF	4.7nF	10nF	10nF	10nF
Rvpol(R2)	2k	1.8k	1.5k	1.3k	1.1k	1.0k

Note:Optimised for F(tone)=22kHz

APPLICATIONS CIRCUIT

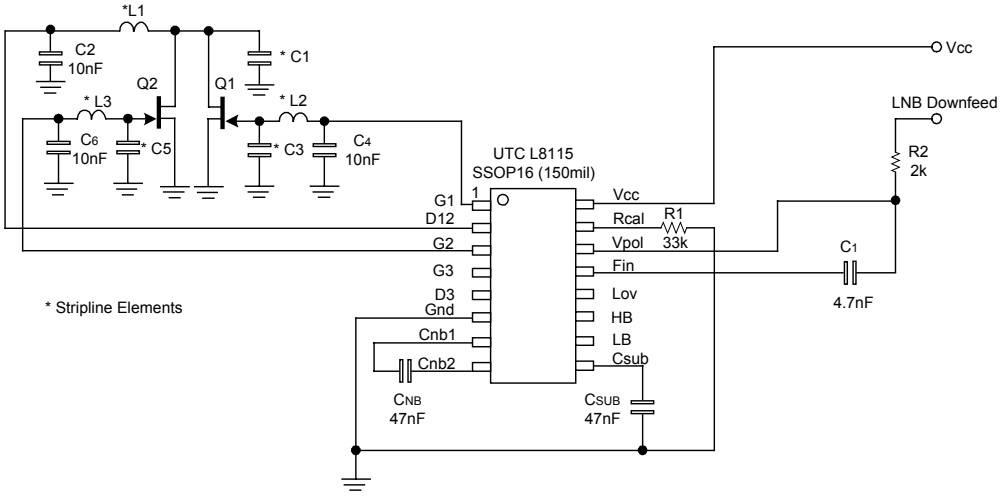
The diagrams below show partial application circuits for the UTC series showing all external components required for appropriate biasing. The bias circuits are unconditionally stable over the full temperature range with the associated FETs and gate and drain capacitors in circuit.

Capacitors C2 and C4 ensure that residual power supply and substrate generator noise is not allowed to affect other external circuits which may be sensitive to RF interference. They also serve to suppress any potential RF feedthrough between stages via the UTC device. These capacitors are required for all stages used. Values of 10nF and 4.7nF respectively are recommended however this is design dependent and any value between 1nF and 100nF could be used.

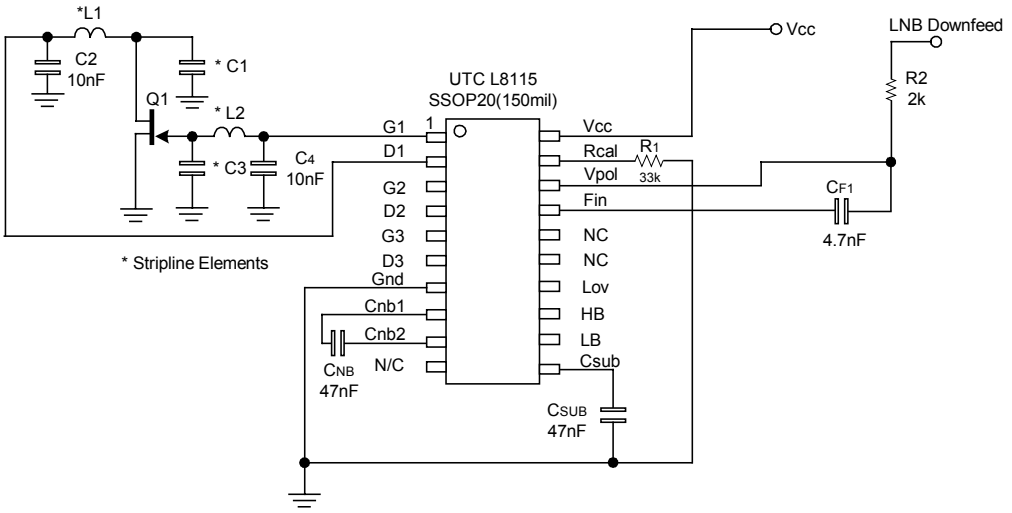
The capacitors C_{NB} and C_{SUB} are an integral part of the UTCs negative supply generator. The negative bias voltage is generated on-chip using an internal oscillator. The required value of capacitors C_{NB} and C_{SUB} is 47nF. This generator produces a low current supply of approximately -3 volts. Although this generator is intended purely to bias the external FETs, it can be used to power other external circuits via the C_{SUB} pin.

Resistor R_{CAL} sets the drain current at which all external FETs are operated. If any bias control circuit is not required, its related drain and gate connections may be left open circuit without affecting the operation of the remaining bias circuits.

The UTC L8115 has been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range -3V to 1V under any conditions, including powerup and powerdown transients. All the bias stages include drain currents limits which work independently in each stage. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current.



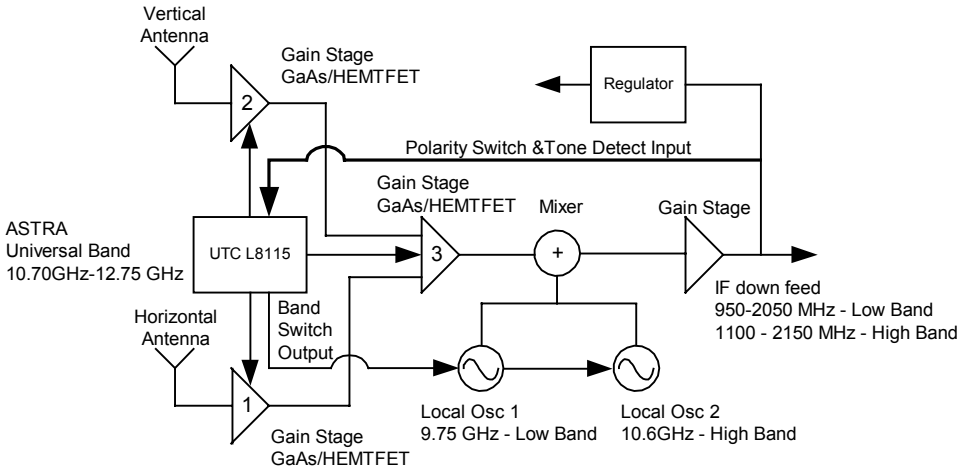
SSOP16(150mil) Applications circuit



SSOP20(150mil) Applications circuit

The following block diagram shows the main section of an LNB designed for use with the Astra series of satellites. The UTC L8115 is the core bias and control element of this circuit. The UTC provides the negative rail, FET bias control, polarisation switch control, tone detection and band switching with the minimum of external components. Compared to other discrete component solutions the UTC circuit reduces component count and overall size required.

Single Universal LNB Block Diagram



Tone detection and band switching is provided on the UTC L8115 devices. The following diagrams describes how this feature operates in an LNB and the external components required. The presence or absence of a 22kHz tone applied to pin FIN enables one of two outputs, LB and HB. A tone present enables HB and tone absent enables

LB. The LB and HB outputs are designed to be compatible with both MMIC and discrete (bipolar or FET) local oscillator applications, selected by pin LOV. Referring to Figure 1 wiring pin LOV to ground will force LB and HB to switch between -2.6V (disabled) and 0V (enabled). Referring to Figures 2 and 3 wiring pin LOV to a positive voltage source (e.g. a potential divider across VCC and ground set to the required oscillator supply voltage, VOSC) will force the LB and HB outputs to provide the required oscillator supply, VOSC, when enabled and 0V when disabled.

Tone Detection Function

LOV	FIN	LB	HB	LB	HB
GND	22kHz	Disabled	Enabled	-3 volts	GND
	-	Enabled	Disabled	GND	-3 volts
VOSC	22kHz	Disabled	Enabled	Note 1	Vosc
	-	Enabled	Disabled	Vosc	Note 1

Note 1: 0 volts in typical LNB applications but ependent on extenal circuits.

APPLICATIONS LOCAL OSCILLATOR CIRCUITS

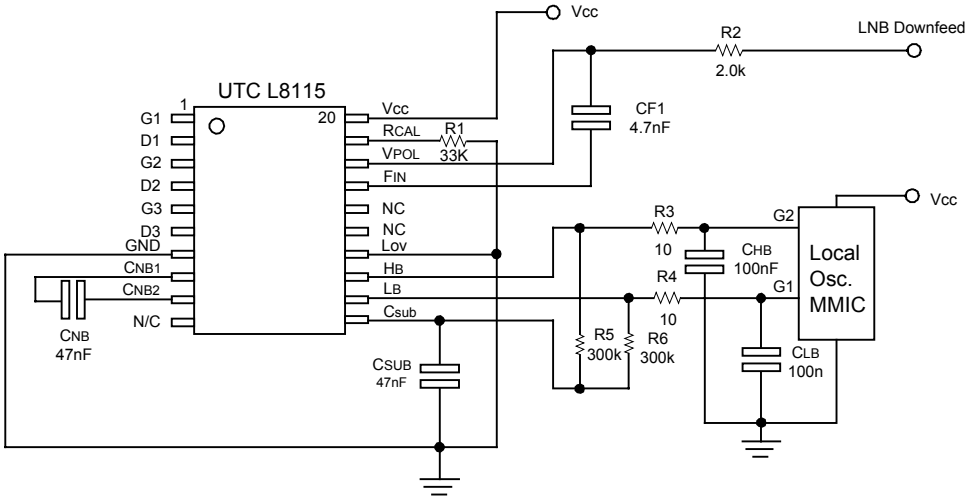


Figure 1

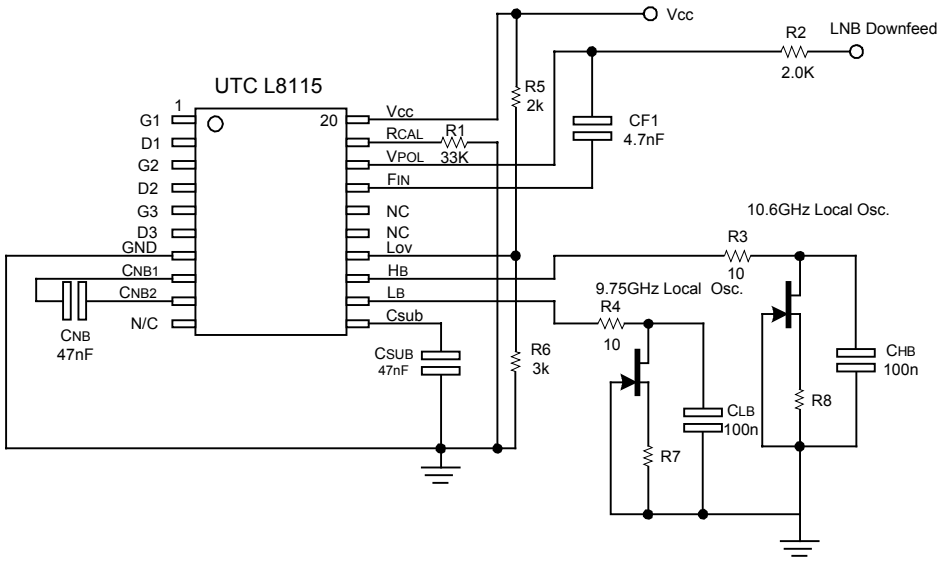


Figure 2

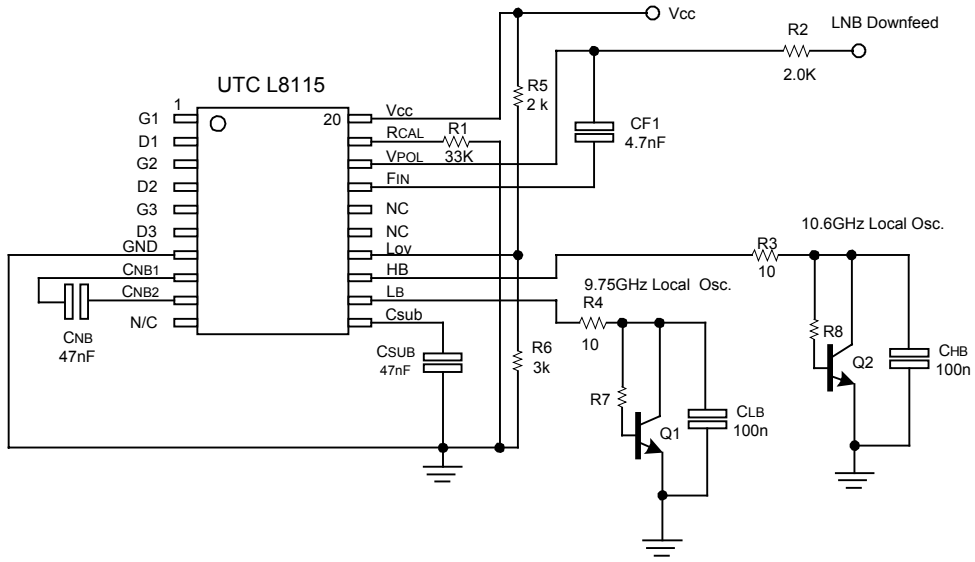


Figure 3