PM7341, PM8316

S/UNI-IMA-84, TEMUX-84

S/UNI-IMA-84/TEMUX-84 DEVELOPMENT KIT

PRELIMINARY

ISSUE 2: JUNE 2001

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
2	June 2001	Updated Schematics Added Board Modifications section Modified Software Interface section Inclusion of Bill of Materials Inclusion of Layout Inclusion of VHDL code Updated SEEP register values Minor grammatical and formatting changes
1	December 2000	Document Created.

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1 INTRODUCTION

The S/UNI-IMA-84/TEMUX-84 Development Kit is intended for software development of several PMC-Sierra devices including:

- SPECTRA-155
- TEMUX-84
- S/UNI-IMA-84
- S/UNI-DUPLEX

1.1 Purpose

The S/UNI-IMA-84/TEMUX-84 Development Kit is intended to assist engineers in board design and software development using PMC-Sierra's PM7341 S/UNI-IMA-84, PM8316 TEMUX-84, PM5342 SPECTRA-155 and PM7350 S/UNI-DUPLEX.

The S/UNI-IMA-84/TEMUX-84 Development Kit can also be used to generate a high speed Low Voltage Differential Signal (LVDS) serial link for connection to other PMC-Sierra devices with an LVDS interface.

1.2 Scope

This document describes the design of the S/UNI-IMA-84/TEMUX-84 Development Kit. A description for each of the functional blocks of the design is given followed by the detailed design, including physical and mechanical descriptions, implementation descriptions, layout, bill of materials and CPLD code.

1.3 Applications

1.3.1 ATM Edge Switch IMA and UNI Port Card

An optimized solution comprising the PM7341 S/UNI-IMA-84 and PM8316 TEMUX-84 devices enables a new generation of high-density port cards for terminating up to an OC-3s worth of IMA circuits (84 T1 links). The following Figure shows the S/UNI-IMA-84 connected to a TEMUX-84, SDRAM and an ATM Layer Device.

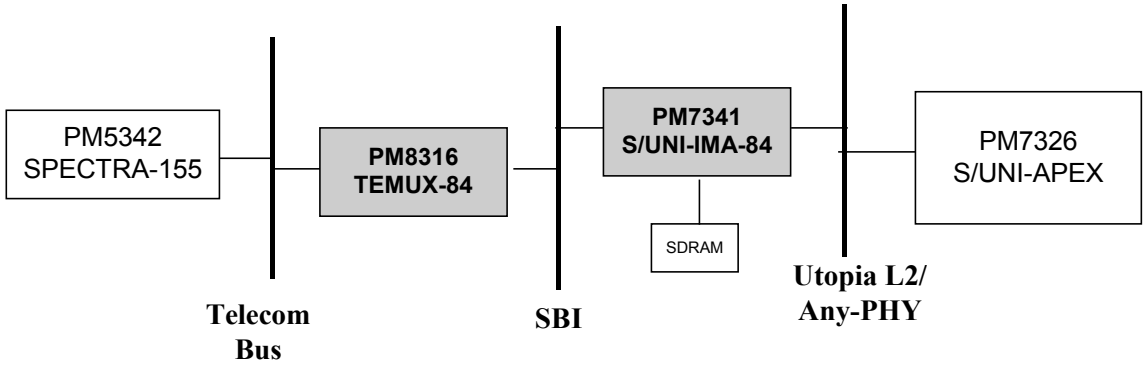

Figure 1 ATM Edge Switch IMA and UNI Port Card Example

1.1.1 ATM Multiservice Switch, Any Service Any Port Card

The following Figure shows an ATM Multiservice Switch Any Service, Any Port card comprising the PM7341 S/UNI-IMA-84, PM7385 FREEDM-84A672, Frame Relay to ATM Interworking Functions, PM73122 AAL1gator-32, PM8316 TEMUX-84, PM5342 SPECTRA-155 and a DS3 LIU. Through software configuration of the devices, any port can be configured to support IMA, User-to-Network Interfaces (UNI), Frame Relay or Circuit Emulation Service.

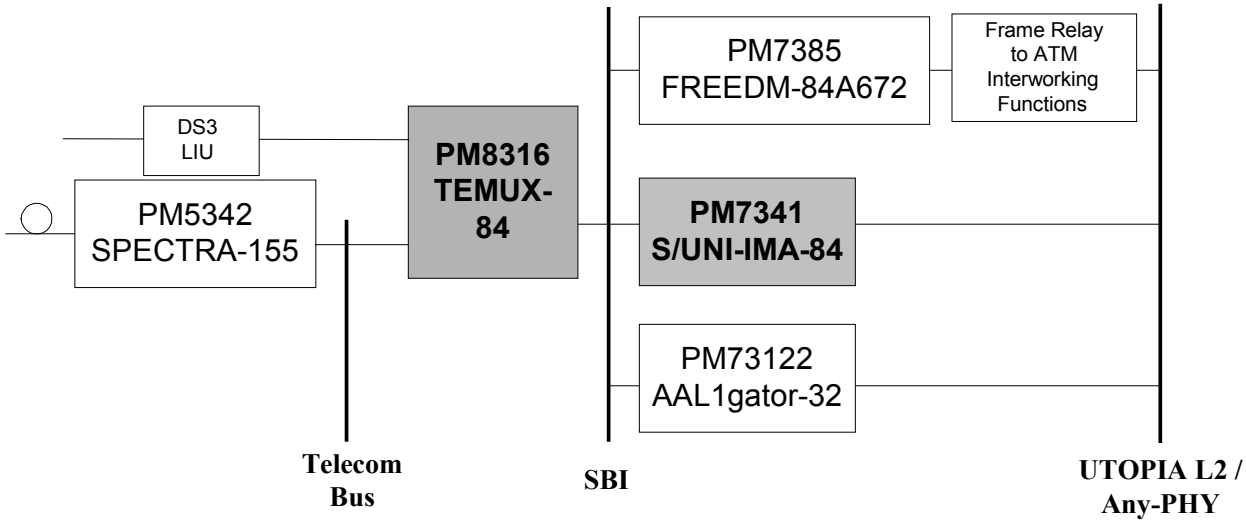

Figure 2 ATM Multiservice Switch, Any Service Any Port Card Example

2 FEATURES

This Reference Design provides the following features:

- Provides full access to the SPECTRA-155, TEMUX-84, S/UNI-IMA-84, S/UNI-DUPLEX registers.
- 33 MHz CompactPCI (CPCI) interface.
- On board hot swap controller with power sequencing.
- 3.3 Volt CMOS Telecom bus allowing communication between the SPECTRA-155 and the TEMUX-84.
- 19.44 MHz SBI bus allowing communication between the TEMUX-84 and the S/UNI-IMA-84.
- UTOPIA Level 2 bus allowing communication between the S/UNI-IMA-84 and the S/UNI-DUPLEX.
- Two LVDS serial links provided for applications that need 1:1 protection such as connection to the DSLAM Core Card (part of the DSLAM Reference Design) for connection to WAN up-link.
- Front panel status LED's which display line status and power supply status.

3 FUNCTIONAL DESCRIPTION

3.1 Data Flow

The S/UNI-IMA-84/TEMUX-84 Development Kit is connected over a CompactPCI bus to a host processor and external memory. Figure 3 illustrates the general data flow.

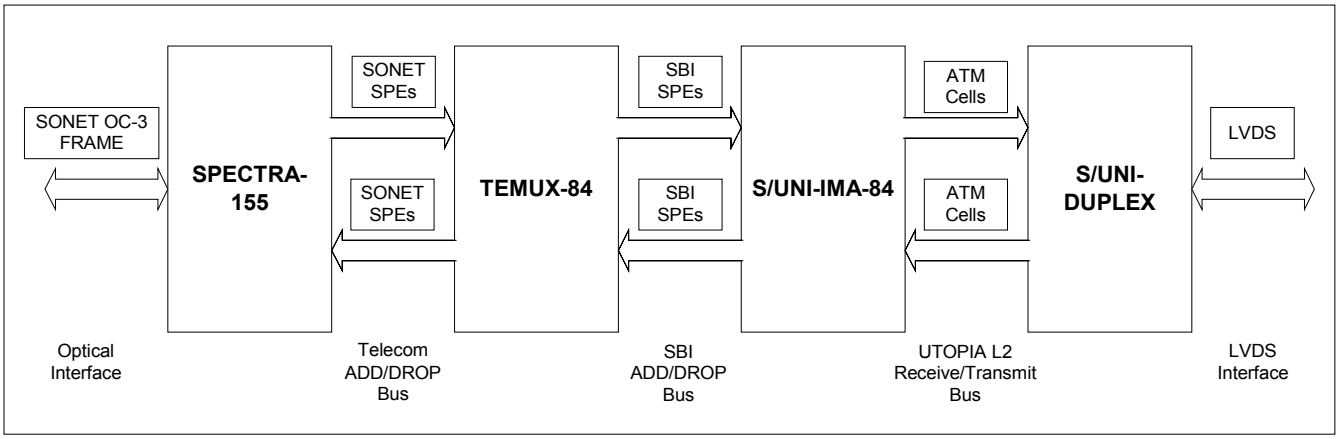

Figure 3 S/UNI-IMA-84/TEMUX-84 Development Kit Data Flow

3.1.1 Transmit Direction

In the transmit direction, the S/UNI-DUPLEX receives data via the LVDS interface. The S/UNI-DUPLEX demultiplexes these ATM cells and routes them to the appropriate virtual PHY of the S/UNI-IMA-84 via the UTOPIA L2 bus.

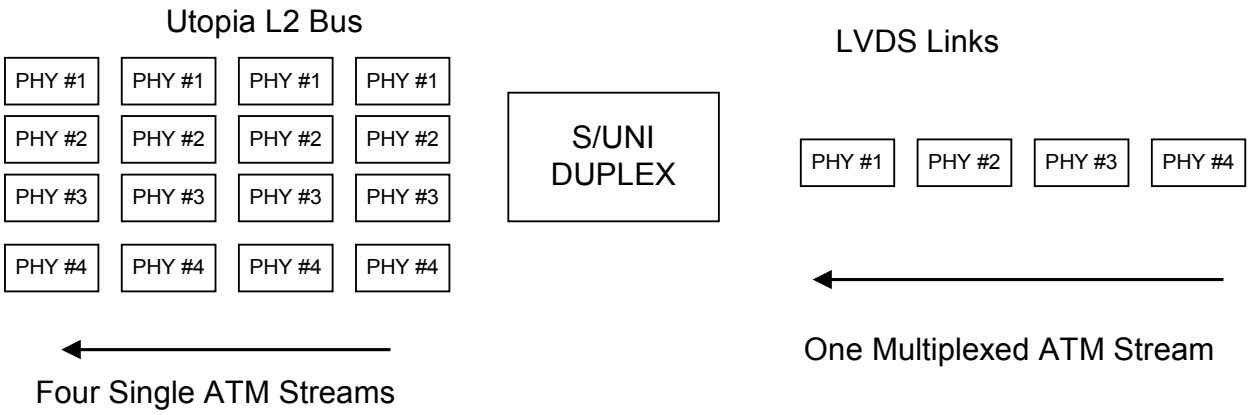

Figure 4 S/UNI-DUPLEX Demultiplexing ATM Streams

The S/UNI-IMA-84 performs the IMA protocol on the data recovered from the UTOPIA L2 bus. The IMA protocol consists of taking a cell stream destined to a group and distributing the cells in a round-robin fashion to the links within a group, adding IMA Control Protocol (ICP) cells, filler cells and stuff cells as needed. The ICP cells convey state information to the far end and are used to format an IMA frame. The IMA frame is used as a mechanism to synchronize the links at the far end. Cell rate decoupling is performed at the IMA sub-layer via filler cells. Filler cells are used instead of physical layer cells for cell rate decoupling, thus a continuous stream of cells is sent to the TC layer.

By distributing the ATM cell stream to multiple physical links in a round-robin fashion, an IMA Group appears to the ATM layer devices like a PHY layer device with a maximum capacity which is determined by the number of links per group the S/UNI-IMA-84 is configured to support (e.g. nxT1, nxE1, nxG.SHDSL). The S/UNI-IMA-84 supports up to 42 simultaneous IMA groups and each IMA group can support 1 to 32 links with the constraint of a maximum of 84 total links. However, because the S/UNI-IMA-84 is configured in UTOPIA L2 mode (as opposed to Any-PHY) and because UTOPIA L2 only supports 31 PHYs, only up to a maximum of 31 virtual PHYs can be addressed within the S/UNI-IMA-84.

An IMA Group is referred to as a virtual PHY because the ATM layer can address multiple virtual PHYs within one physical PHY device, the S/UNI-IMA-84. In this design, an IMA link refers to the individual T1 line, down which a portion of the Group's ATM traffic travels.

An IMA layer device on the other end of the physical links will reassemble the ATM cells arriving from the various physical links into a single ATM stream, which it will pass to the ATM layer.

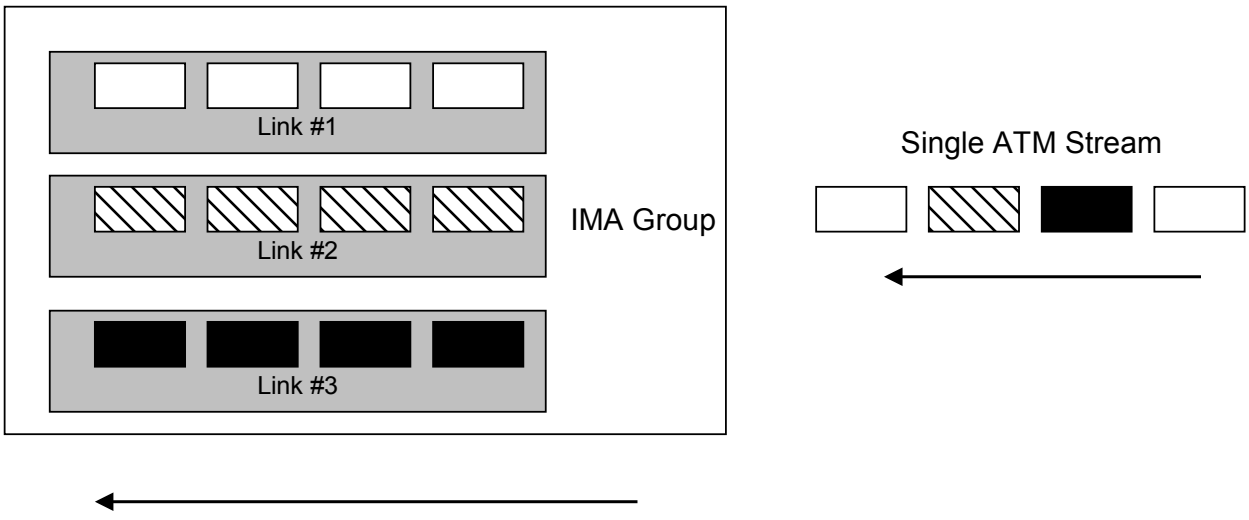

Figure 5 IMA Protocol

In the TC sub-layer, the HEC is calculated and inserted into the cell headers. The cell stream is then mapped into the DS1 payload with zeros inserted for the framing and overhead bits.

After a serial to parallel conversion is performed on the 84 links, the data is then conveyed across the SBI ADD bus to the TEMUX-84.

The EXSBI (Extract Scaleable Bandwidth Interconnect) block of the TEMUX-84 device demaps up to 84 1.544Mb/s links, 63 2.048Mb/s links or three 44.736Mb/s links from the SBI ADD bus. Timing for the links can be slaved to the arrival rate of data or from link rate adjustments provided by the TEMUX-84. In this design, the TEMUX-84 is configured in master mode. The TEMUX-84 can also send link rate adjustment requests to the S/UNI-IMA-84 using the AJUST_REQ signal. This signal indicates whether the S/UNI-IMA-84 should send one additional or one fewer byte of data during the next 500 μs interval.

Each T1 transmitter frames to SF or ESF DS1 formats, or framing can be optionally disabled. The TEMUX-84 supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion and zero-code suppression on a per-DS0 basis. PRBS generation or detection is supported on a framed and unframed T1 basis.

The SPE's from the TEMUX-84 are transmitted to the SPECTRA-155 devices via the TELECOM ADD Bus.

Each TPIP (Transmit Pointer Interpreter) block within the SPECTRA-155 takes the SPEs from the TELECOM ADD Bus and interprets the H1, H2 pointers, indicates the J1 byte location, and detects alarm conditions. The TTAL (Transmit Telecombus Aligner) block then takes the STS-1 SPE from the TPIP, and aligns it to the frame of the transmit stream. The TPOP (Transmit Path O/H Processor) block then performs path overhead processing. Following this, both Line and Section Overhead processing occurs before the complete SONET STS-3 SPE is transmitted serially over transmit line interface.

The transmitted signal is then converted to optical format by the front panel Optical Interface unit.

3.1.2 Receive Direction

The S/UNI-IMA-84/TEMUX-84 Development Kit receives SONET/SDH OC-3 (155.52 Mbits\s) frames through the front panel optical interface. The optical interface converts the optical signals into STS-3 (155.52 Mbits\s) electrical signals for processing by the SPECTRA-155.

The SPECTRA-155 receives SONET/SDH frames via a bit serial interface, recovers clock and data, and terminates the SONET/SDH section (regenerator section), line (multiplexer section), and path. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section and line bit interleaved parity (BIP) (B1, B2), accumulating error counts at each level for performance monitoring purposes. B2 errors are also monitored to detect signal fail and signal degrade threshold crossing alarms (for use with Automatic Protection Switching). Line remote error indications (M1) are also accumulated.

In addition, the SPECTRA-155 interprets the received payload pointers (H1, H2), detects path alarm conditions, detects and accumulates path BIPs (B3). The SPECTRA-155 also monitors and accumulates path Remote Error Indications (REIs), accumulates and compares the 16 or 64 byte path trace (J1) message against an expected result, and extracts the Synchronous Payload Envelope (virtual container).

Figure 6 below depicts the format of an incoming SONET STS-3 Frame using floating SPE structures. The SPE's are located using the H1 and H2 pointer bytes.

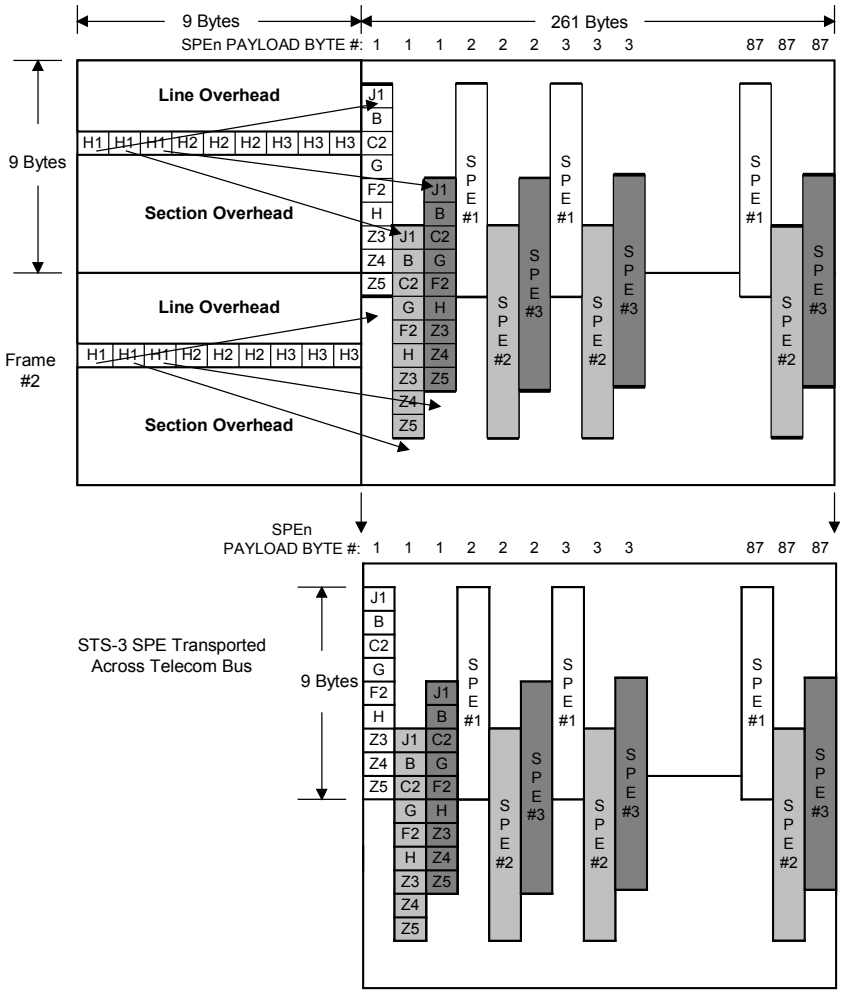

Figure 6 SONET OC-3 Frame Processing by the SPECTRA-155

The extracted SPE is placed on the Telecom DROP bus. The DPL (DROP Bus Payload Active) and DC1J1V1 (DROP Bus Composite Timing) signals indicate the location of the path overhead and the tributaries within the SPE.

The TEMUX-84 device receives data placed on the TELECOM DROP Bus. The TEMUX-84 is configured to use a Telecom Bus (SONET\SDH) Line Side Interface and the SBI Bus System Side Interface.

The SONET/SDH line side interface provides STS-1 SPE processing and generation. The payload processor aligns and monitors the performance of SONET virtual tributaries (VT1.5s). Maintenance functions per tributary include loss of pointer detection, AIS alarm, tributary path signal label mismatch, and tributary path signal label unstable alarms. Optionally, interrupts can be generated due to the assertion and removal of any of the above alarms. Counts

are accumulated for tributary path BIP-2 errors on a block or bit basis and for FEBE indications. The synchronous payload envelope generator generates all tributary pointers and calculates and inserts tributary path BIP-2. The generator also inserts FEBE, RDI and enhanced RDI in the V5 byte. Software can force AIS insertion on a per tributary basis.

The TEMUX-84 SONET/SDH VT Payload Processor demaps up to 84 T1s from the three STS-1 SPEs (AU3 or TUG3). The bit asynchronous demapper performs majority vote C-bit decoding to detect stuff requests for T1, E1 and DS3 asynchronous mappings. The VT1.5/VT2/TU-11/TU-12 mapper uses an elastic store and a jitter attenuator to minimize jitter introduced via bit stuffing.

Figure 7 depicts how the individual STS-1 SPE's (carried within the STS-3 SPE) transmitted across the Telecom Drop Bus are processed by the TEMUX-84. The TEMUX-84 is configured to process three STS-1 SPEs and it utilizes the tributary pointers to locate the beginning of each VT1.5. Figure 7 also shows how each VT1.5 is mapped into the STS-1 SPE.

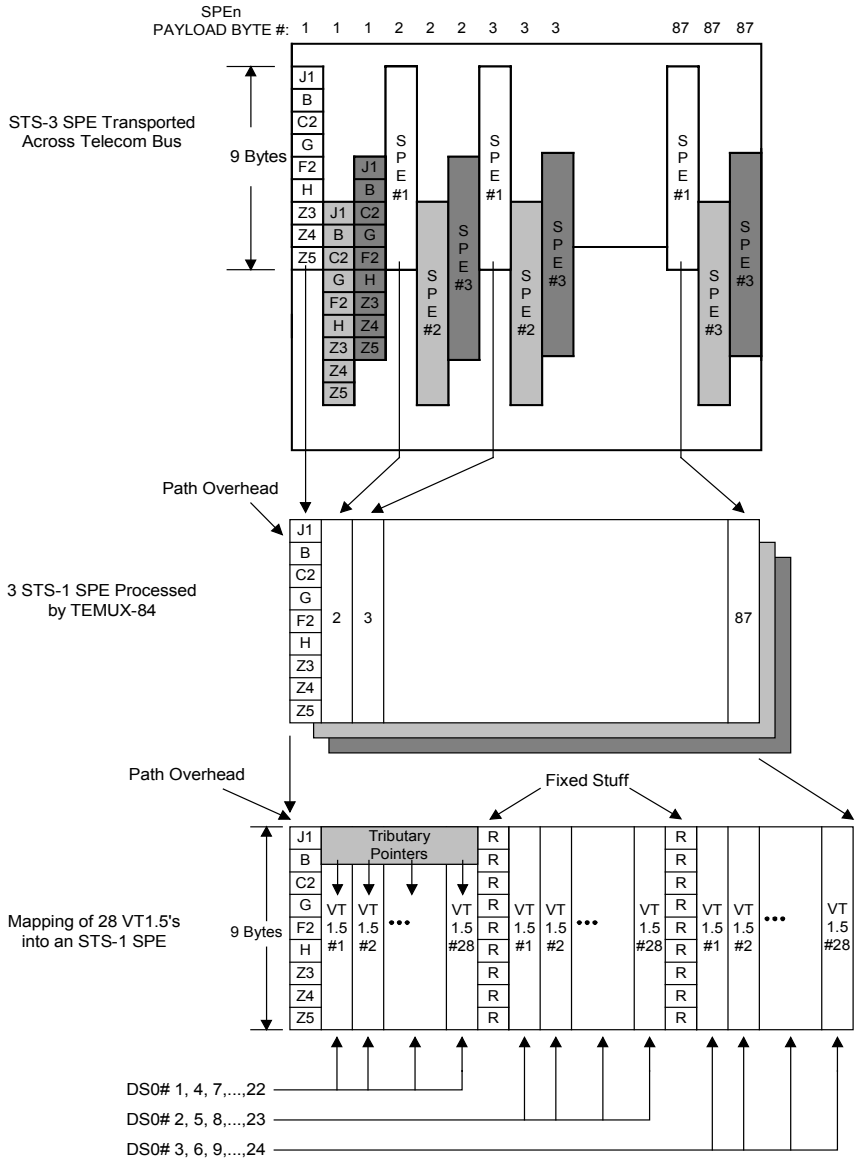

Figure 7 VT1.5 Demapping by the TEMUX-84

The S/UNI-IMA-84 implements the Transmission Convergence (TC) layer function and Inverse Multiplexing for ATM (IMA) protocol for DS1/E1 links.

The TC layer searches for cell delineation as per the procedures outlined in ITU-T Recommendation I.432.1. To find the cell delineations, the TC layer computes the HEC value for all bits received. Once cell delineation is obtained, the payload is optionally descrambled and the cells are passed to the IMA sub-layer. The TC layer provides counts of errored headers as well as OCD and LCD error interrupts.

The IMA sub-layer performs IMA frame delineation and stuff cell removal. IMA delineation consists of reassembling a single ATM stream, running at some multiple of the T1 rate, out of the ATM cells arriving over the multiple physical links. Based upon the ICP cell information, the S/UNI-IMA-84 determines the differential delay between the links within a group and applies the link and group state machine logic to coordinate the activation and deactivation of the groups and links with the far end. The recovered ATM cells are transmitted across a Utopia L2 interface running at 25 MHz to the S/UNI-DUPLEX.

The S/UNI-DUPLEX implements the first stage of multiplexing by routing traffic from the IMA's virtual PHYs and transmitting the traffic simultaneously over two high speed serial 4 wire LVDS providing 1:1 protection for possible interface to a core card for connection to a WAN up-link.

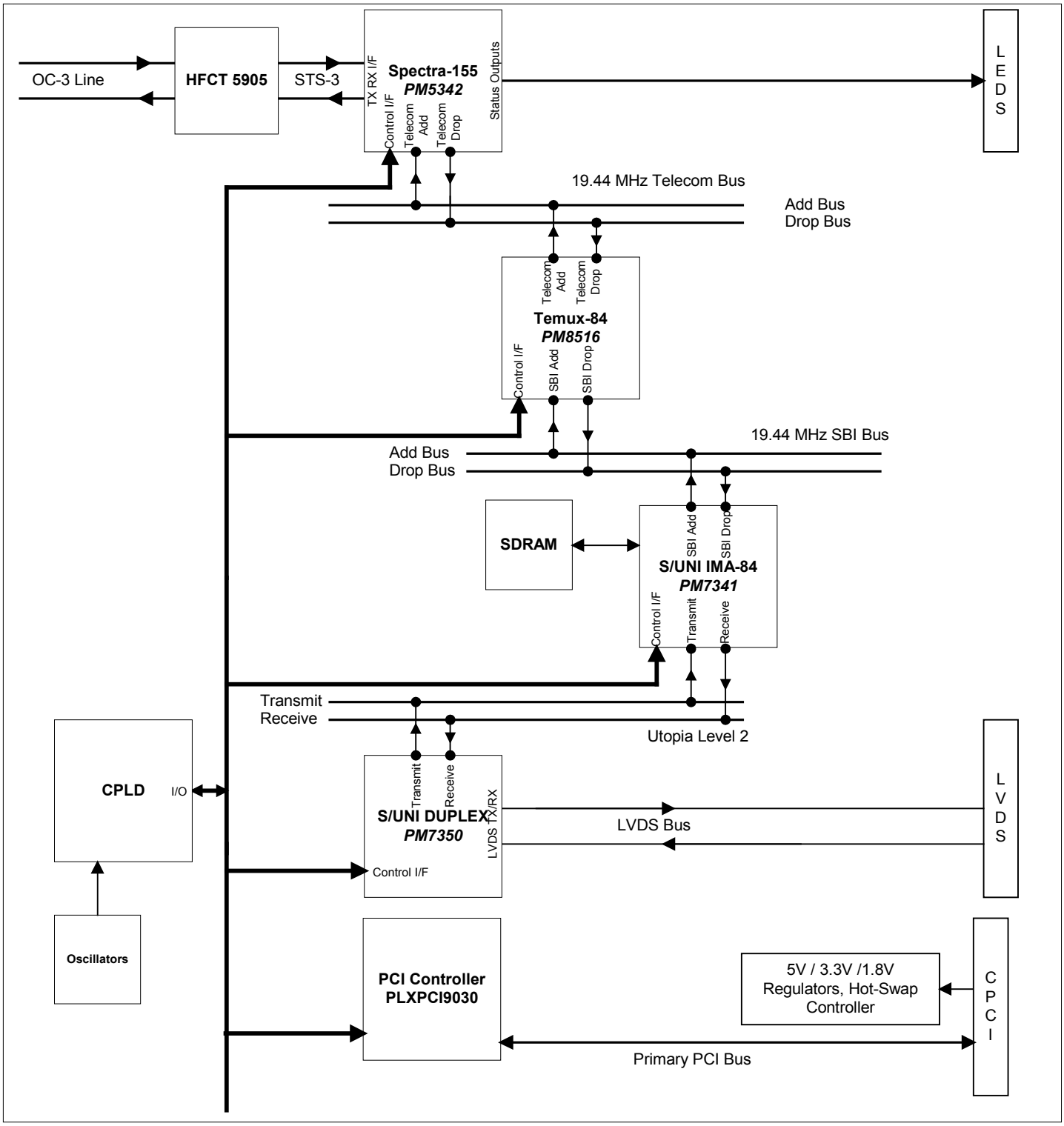

Figure 8 Block Diagram of S/UNI-IMA-84/ TEMUX-84 Development Kit

4 BLOCK DESCRIPTION

The following sections describe the function of each hardware block shown in Figure 8.

4.1 Optics

Conversion between the optical OC-3 signal and the electrical STS-3 signal is accomplished using the HP HFCT-5905 optical transceiver.

4.2 PM5342 SPECTRA-155

The PM5342 SONET/SDH PAYLOAD EXTRACTOR/ALIGNER (SPECTRA-155) terminates the transport and path overhead of STS-1 (STM-0/AU3) and STS-3/3c (STM-1/AU3/AU4) streams at 51.84 Mbit/s and 155.52 Mbit/s respectively. The SPECTRA-155 implements significant functions for a SONET/SDH compliant line interface.

The SPECTRA-155 is implemented in low power, +5 Volt, CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 256-pin SBGA package.

4.3 PM8316 TEMUX-84

The TEMUX-84 is a high density T1/E1 framer with integrated VT/TU Mappers and M13 Multiplexers. PM8316 provides framing and multiplexing for 84 T1 channels or 63 E1 channels into three channelized DS-3's or alternatively maps the T1/E1 channels directly into a SONET/SDH OC-3.

The TEMUX-84 is configured for a Telecom Bus Line Side Interface, and a Scaleable Bandwidth Interconnect (SBI) Bus System Side Interface. The Telecom bus is used to transfer SONET Synchronous Payload Envelopes (SPE) between the SPECTRA-155 and the TEMUX-84. The SBI bus is used to interface to a link layer device, in this case the S/UNI-IMA-84.

4.4 PM7341 S/UNI-IMA-84

The PM7341 S/UNI-IMA-84 is a monolithic integrated circuit that implements the Inverse Multiplexing for ATM protocol over up to 84 T1 links or 63 E1 links when using the high density SBI interface or 32 independent T1/E1 links using the clock and data interface. The S/UNI-IMA-84 can support up to 42 simultaneous IMA groups and each IMA group can support 1 to 32 links with a maximum of 84 links in total. Each group can consist of either T1 or E1 links. Alternatively, the

S/UNI-IMA-84 can be used for cell delineation of up to 84 T1 links, 63 E1 links or 3 DS3 links.

4.4.1 SDRAM

Two configurations of external SDRAM are supported, 16Mbit (1Mbit x 16) and 64 Mbit (4Mbit x 16), both of which are single chip devices.

4.5 PM7350 S/UNI-DUPLEX

The PM7350 S/UNI-DUPLEX is a monolithic integrated circuit, typically used with its sister device, the S/UNI-VORTEX, to implement a point-to-point serial backplane interconnect architecture. The primary role of the S/UNI-DUPLEX is to interface to up to 32 devices (typically framers or PHYs) and transfer 52-56 byte data cells in serial format to/from a backplane. Devices interface to the S/UNI-DUPLEX via an 8 or 16-bit SCI-PHY/UTOPIA/Any-PHY bus, or optionally via a 16-port clock and data interface.

Each S/UNI-DUPLEX can connect to two 100 to 200 Mb/s Low Voltage Differential Signal (LVDS) serial links. A microprocessor port provides access to internal configuration and monitoring registers. The microprocessor port may also be used to insert and extract cells in support of an embedded microprocessor communication channel.

4.6 Bus Interfaces

4.6.1 Telecom Bus Interface

The Telecom bus is used to transfer SONET Synchronous Payload Envelopes (SPE) between the SPECTRA-155 and the TEMUX-84 devices. The connectivity is as shown in Figure 9.

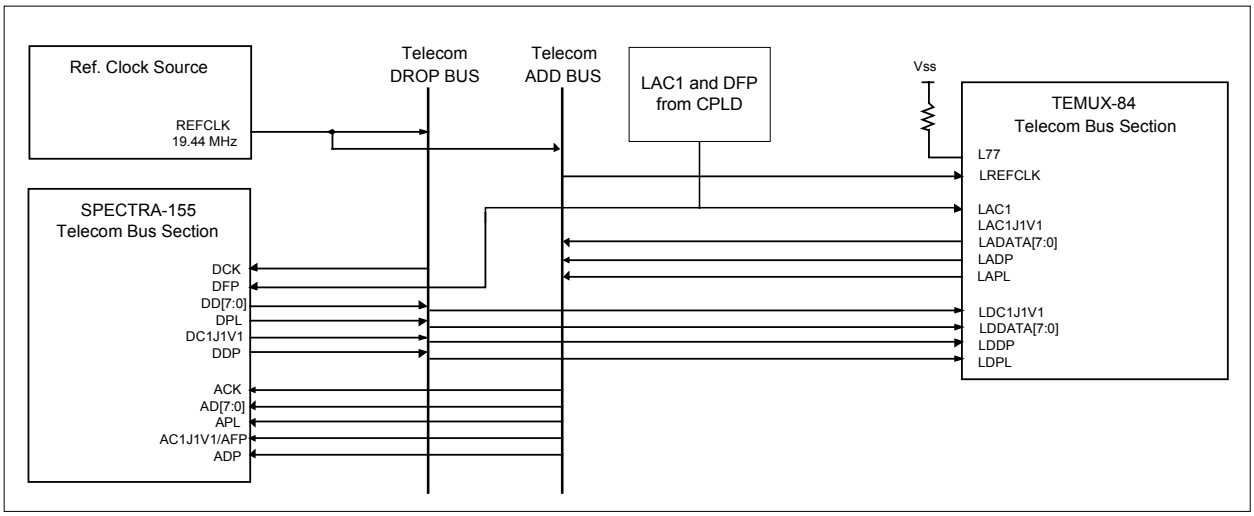

Figure 9 Telecom Bus Interface

In the receive direction, the SONET Payload is presented to the Telecom DROP bus to be received by the TEMUX-84. The TEMUX-84 will terminate the SONET Payload, demultiplex and remap the VT1.5 data into T1 data that will be sent to the S/UNI-IMA-84.

In the transmit direction, the TEMUX-84 drives the Telecom ADD bus. The transmitted SPE is then received and processed by the SPECTRA-155 device.

The TEMUX-84 utilizes the LAC1 signal to identify the frame and multiframe boundaries on the Add data bus. The signal is generated in the CPLD by dividing a 19.44 MHz clock by 9720. The SPECTRA-155 (DFP) also uses this frame pulse.

4.6.2 SBI Bus Interface

The TEMUX-84 device features a Scaleable Bandwidth Interconnect (SBI) bus to interface to link layer devices like the S/UNI-IMA-84. The SBI bus connectivity between TEMUX-84 and the S/UNI-IMA-84 is shown in Figure 10.

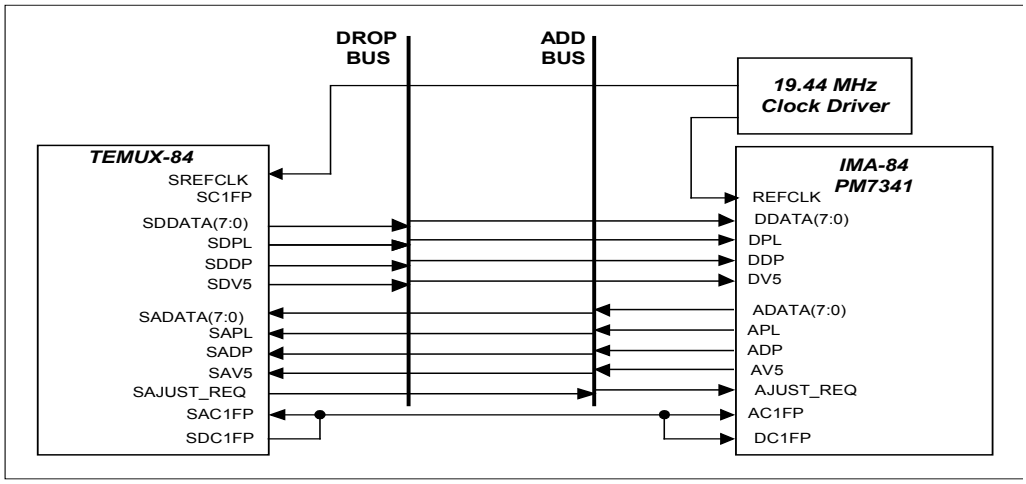

Figure 10 SBI Bus Interface

In the receive direction, the TEMUX-84 will transmit a SPE composed of T1/E1's or DS3's to the S/UNI-IMA-84 via the SBI DROP bus.

In the transmit direction, the S/UNI-IMA-84 will transmit SPE's to the TEMUX-84 device via the SBI ADD Bus.

The SBI bus utilizes the C1FP signal to indicate SBI Bus multiframe alignment, which occurs every 500 μs. The signal is provided by the TEMUX-84.

4.6.3 UTOPIA Level 2 Bus Interface

The UTOPIA Level 2 bus is used to transfer ATM cells between the S/UNI-IMA-84 and the S/UNI-DUPLEX. The S/UNI-DUPLEX serves as the bus master and continuously polls the S/UNI-IMA-84 for transmit (receive) data. Note that for this kit, the UTOPIA Level 2 bus shall run on an external 25 MHz oscillator; however the S/UNI-DUPLEX and the S/UNI-IMA-84 can support a maximum UL2 bus rate of 52 MHz. The UTOPIA L2 interface is software selectable to be 8 or 16 bits wide. This kit is designed for a 16-bit wide UTOPIA L2 bus. The architecture is as shown in Figure 11.

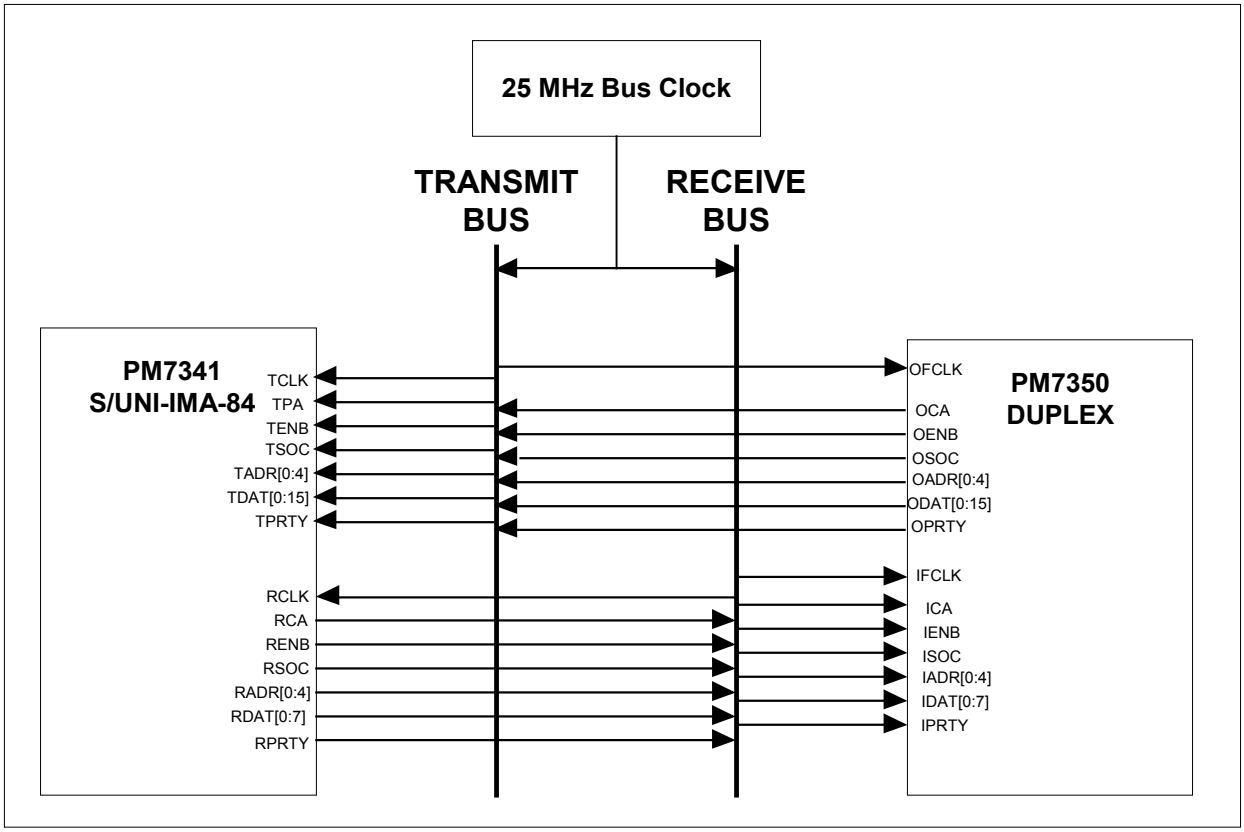

Figure 11 UTOPIA Level 2 Bus Interface

4.7 CompactPCI Bridge

The S/UNI-IMA-84/TEMUX-84 Development Kit does not have an onboard microprocessor and so the PCI bus host processor card interfaces with this development kit via a CPCI bridge device, which only utilizes a read/write (non-burst) register sequence and interrupt service.

The hot swap compatible PLX PCI 9030 (PCI 9030) Bus Target is employed as the CPCI bus interface.

The PCI 9030 has a 32 long word (lword) write FIFO and 16 lword read FIFO allowing the CPCI bus to burst data to and from the external microprocessor and the PMC-Sierra devices. The Local bus interface of the PCI 9030 is generic and very flexible, supporting 8, 16, and 32-bit transfers operating in multiplexed or non-multiplexed modes as big or little endian at a clock rate asynchronous to the PCI bus up to 60MHz. The Local bus is partitioned into 4 distinct user-definable address spaces that can be configured independently. Each Local address

space can be configured to optionally support burst mode transfers and pre-fetching. The timing of each address space is specifiable via a set of programmable wait states as well as supporting a ready signal used to insert additional wait states.

In this development kit, the host processor will access the Local devices via the PCI 9030 CPCI Bridge configured in non-multiplexed 16-bit address and 16-bit data bus mode. The Local bus is clocked at 33MHz by looping the buffered PCI clock output (BCLKO) available from the PCI 9030 back to the Local bus clock input.

The PCI 9030 is designed to operate with either a 33 or 66 MHz PCI bus in a +3.3 V signaling environment, but is also +5 V tolerant on its PCI interface.

4.8 SEEP

The NM93CS56 Serial EEPROM from Fairchild Semiconductor is used to store configuration information for the PCI 9030 Bridge. This specific SEEP (or equivalent) is required by PCI 9030 because it supports sequential read operations.

The SEEP is 1Kbit deep, 256 bits of which are occupied by the PCI 9030 configuration data, leaving 768 bits unused. The SEEP clock is 250 kHz, which is derived from the PCI clock of 33 MHz internally divided by 132.

4.8.1 Card ID Number

The Applications specific Card number is stored in the serial EEPROM. The Card ID assignment is shown in Table 1 below.

Table 1 PCI Card ID Codes

Device	Vendor ID	Device ID	Subsystem Vendor ID	Subsystem ID
Unconfigured PCI 9030	10B5h	9030h	11F8h (PMC-Sierra)	2356h S/UNI-IMA-84/TEMUX-84 Development kit Issue 1

The 11F8 hex is PMC-Sierra's registered vendor ID. Subsystem ID 2356 hex is unregistered ID for the S/UNI-IMA-84/TEMUX-84 Development kit Issue 1.

4.8.2 Serial EEPROM Load Registers

The PCI 9030 can be initialized to a large extent by reading data from its serial EEPROM port during initialization. Reading the data from the serial EEPROM is equivalent to directly writing to the 9030's configuration registers via the CPU.

The S/UNI-IMA-84/TEMUX-84 Development kit includes an EEPROM for this purpose. Table 2 illustrates the **preliminary** serial EEPROM Load Registers' contents.

Refer to the PCI 9030 datasheet for detailed information on the format of the configuration data stored in the SEEP.

Table 2 PCI 9030 Serial EPROM Load Registers

SEEP Offset	Description	PCI 9030 Register Bits Affected	Setting
0h	Device ID	PCIIDR[31:16]	9030h
2h	Vendor ID	PCIIDR[15:0]	10B5h
4h	PCI Status	PCISR[15:0]	0290h
6h	PCI Command	PCIICR[	0000h
Ah	Class Code	PCICCR[23:8]	0001h
8h	Class Code / Revision	PCICCR[7:0] / PCIREV[7:0]	0680h
Ch	Subsystem ID	PCISID[15:0]	2356h
Eh	Subsystem Vendor ID	PCISVID[15:0]	11F8h
10h	MSW New Capability Pointer	Reserved	XXXXh
12h	LSW New Capability Pointer	CAP_PTR[7:0]	XX40h
14h	(Maximum Latency and Minimum Grant are not loadable)	Reserved	XXXXh
16h	Interrupt Pin (Interrupt Line Routing is not loadable)	PCIIPR[7:0] / PCIILR[7:0]	0100h
18h	MSW of Power Management Capabilities	PMC[14:11, 5, 3:0]	4801h
1Ah	LSW of Power Management Next Capability Pointer / Power Management Capability ID	PMNEXT[7:0] / PMCAPID[7:0]	4801h
1Ch	MSW of Power Management Data / PMCSR Bridge Support Extension	Reserved	XXXXh
1Eh	LSW of Power Management Control / Status	PMCSR[14:8]	0000h
20h	MSW of Hot Swap Control / Status	Reserved	XXXXh
22h	LSW of Hot Swap Next Capability Pointer / Hot Swap Control	HS_NEXT[7:0] / HS_CNTL[7:0]	4C06h
24h	PCI Vital Product Data Address	Reserved	0000h

SEEP Offset	Description	PCI 9030 Register Bits Affected	Setting
26h	PCI Vital Product Next Capability Pointer / PCI Vital Product Data Control	PVPD_NEXT[7:0] / PVPDCNTL[7:0]	0003h
28h	MSW of Range for PCI-to-Local Address Space 0	LAS0RR[31:16]	0FF0h
2Ah	LSW of Range for PCI-to-Local Address Space 0	LAS0RR[15:0]	0000h
2Ch	MSW of Range for PCI-to-Local Address Space 1	LAS1RR[31:16]	0000h
2Eh	LSW of Range for PCI-to-Local Address Space 1	LAS1RR[15:0]	0000h
30h	MSW of Range for PCI-to-Local Address Space 2	LAS2RR[31:16]	0000h
32h	LSW of Range for PCI-to-Local Address Space 2	LAS2RR[15:0]	0000h
34h	MSW of Range for PCI-to-Local Address Space 3	LAS3RR[31:16]	0000h
36h	LSW of Range for PCI-to-Local Address Space 3	LAS3RR[15:0]	0000h
38h	MSW of Range for PCI-to-Local Expansion ROM	EROMRR[31:16]	FFFFh
3Ah	LSW of Range for PCI-to-Local Expansion ROM	EROMRR[15:0]	0000h
3Ch	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[31:16]	0000h
3Eh	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0	LAS0BA[15:0]	0001h
40h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[31:16]	0000h
42h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1	LAS1BA[15:0]	0000h
44h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 2	LAS2BA[31:16]	0000h
46h	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 2	LAS2BA[15:0]	0000h
48h	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 3	LAS3BA[31:16]	0000h
4Ah	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 3	LAS3BA[15:0]	0000h
4Ch	MSW of Local Base Address (Remap) for Expansion ROM	EROMBA[31:16]	0010h
4Eh	LSW of Local Base Address (Remap) for Expansion ROM	EROMBA[15:0]	0000h
50h	MSW of Bus Region Descriptors for Local Address Space 0	LAS0BRD1[31:16]	5481h
52h	LSW of Bus Region Descriptors for Local Address Space 0	LAS0BRD1[15:0]	0080h

SEEP Offset	Description	PCI 9030 Register Bits Affected	Setting
54h	MSW of Bus Region Descriptors for Local Address Space 1	LAS1BRD1[31:16]	0000h
56h	LSW of Bus Region Descriptors for Local Address Space 1	LAS1BRD1[15:0]	0000h
58h	MSW of Bus Region Descriptors for Local Address Space 2	LAS2BRD1[31:16]	0000h
5Ah	LSW of Bus Region Descriptors for Local Address Space 2	LAS2BRD1[15:0]	0000h
5Ch	MSW of Bus Region Descriptors for Local Address Space 3	LAS3BRD1[31:16]	0000h
5Eh	LSW of Bus Region Descriptors for Local Address Space 3	LAS3BRD1[15:0]	0000h
60h	MSW of Bus Region Descriptors for Expansion ROM	EROMBRD[31:16]	0000h
62h	LSW of Bus Region Descriptors for Expansion ROM	EROMBRD[15:0]	0000h
64h	MSW of Chip Select (CS) 0 Base and Range	CS0BASE[31:16]	0002h
66h	LSW of Chip Select (CS) 0 Base and Range	CS0BASE[15:0]	0001h
68h	MSW of Chip Select (CS) 1 Base and Range	CS1BASE[31:16]	0006h
6Ah	LSW of Chip Select (CS) 1 Base and Range	CS1BASE[15:0]	0001h
6Ch	MSW of Chip Select (CS) 2 Base and Range	CS2BASE[31:16]	000Ah
6Eh	LSW of Chip Select (CS) 2 Base and Range	CS2BASE[15:0]	0001h
70h	MSW of Chip Select (CS) 3 Base and Range	CS3BASE[31:16]	000Eh
72h	LSW of Chip Select (CS) 3 Base and Range	CS3BASE[15:0]	0001h
74h	Serial EEPROM Write-Protected Address Boundary	PROT_AREA[7:0]	0030h
76h	LSW of Interrupt Control / Status Register	INTCSR[15:0]	0000h
78h	MSW of PCI Target Response, Serial EEPROM, and Initialization Control	CNTRL[31:16]	0078h
7Ah	LSW of PCI Target Response, Serial EEPROM, and Initialization Control	CNTRL[15:0]	0000h
7Ch	MSW of General Purpose I/O Control	GPIOC[31:16]	0000h
7Eh	LSW of General Purpose I/O Control	GPIOC[15:0]	0240h
80h	MSW of Hidden Power Management Data Select (refer to Section 7.2.1 of PCI 9030 Data sheet)	PMDATA[7:0] hidden, D_0 and D_{3hot} Power Dissipated	0000h
82h	LSW of Hidden Power Management Data Select (refer to Section 7.2.1 of PCI 9030 Data sheet)	PMDATA[7:0] hidden, D_0 and D_{3hot} Power Consumed	0000h

SEEP Offset	Description	PCI 9030 Register Bits Affected	Setting
84h	MSW of Hidden Power Management Data Scale (refer to Section 7.2.1 of PCI 9030 Data Sheet)	Reserved	0000h
86h	LSW of Hidden Power Management Data Scale (refer to Section 7.2.1 of PCI 9030 Data Sheet)	PMCSR[14:13] hidden, Bits[7:0] are used as follows: [7:6] D_{3hot} Power Dissipated [5:4] D_0 Power Dissipated [3:2] D_{3hot} Power Consumed [1:0] D_0 Power Consumed	0000h
87-100h	Blank		

4.9 CPLD

A Xilinx XC9536XL CPLD provides the miscellaneous logic required for the board, and framing pulses that is required by the SPECTRA-155 as shown in Figure 12. The timing requirements for the design were such to allow the slowest speed grade of XC9536XL available (-10) to be used. Faster pin-compatible devices are available should future requirements have tighter timing constraints. Pin compatible devices with more internal logic resources are also available. The logic for the CPLD is specified exclusively in a single VHDL source file. The VHDL code is available in APPENDIX D: VHDL Code for CPLD. 16 of the 34 I/O pins available are used. 14 of the remaining I/O pins are accessible via headers.

The CPLD is programmed via its JTAG port. The JTAG port is accessible through the debug header. This interface allows for the possibility of remote upgrades of the CPLD configuration.

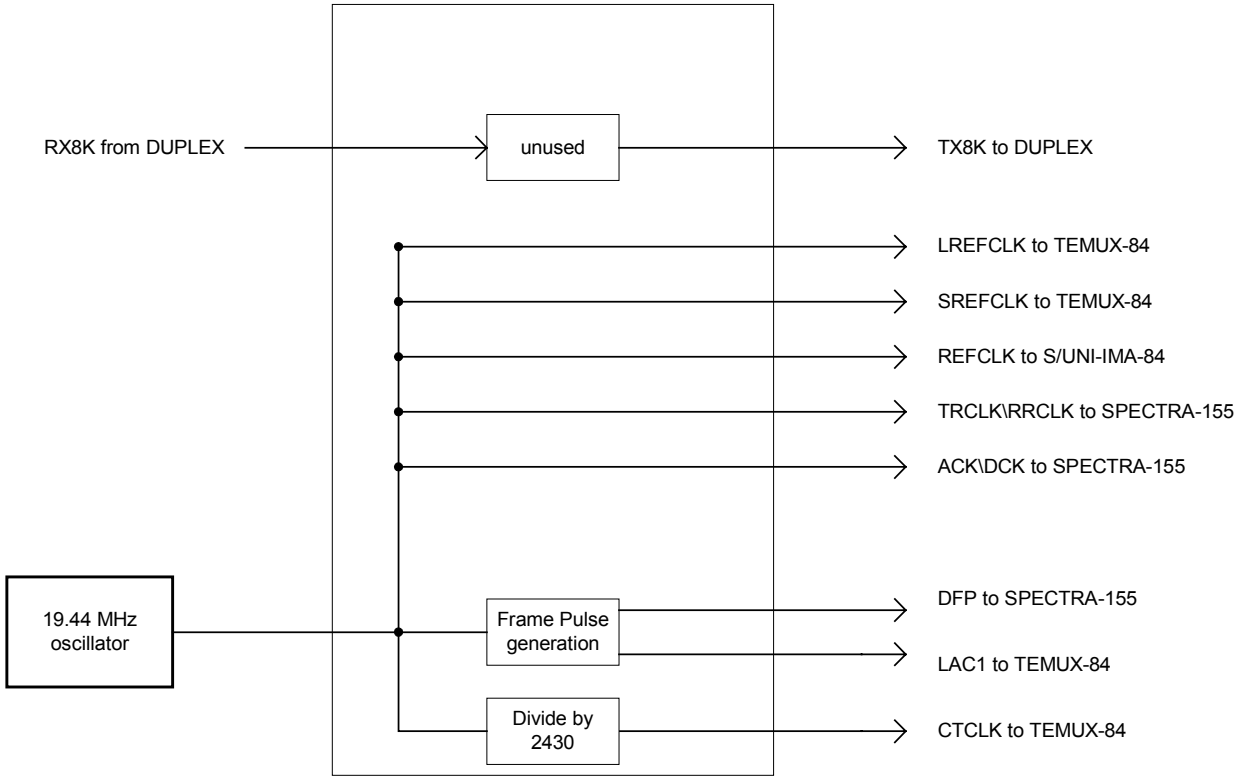

Figure 12 CPLD Logic Block Diagram

4.9.1 Local Bus Glue Logic

Some additional logic is required to glue the interrupt bits from the four PMC-Sierra devices to the PCI bridge Local bus. The four interrupts from devices are decoded to two interrupt bits to the PCI bridge. All four interrupt bits are also sent to General Purpose I/O pins of the PCI bridge.

4.10 Full Hot Swap Capability

Hot swap functionality allows the orderly insertion and removal of boards without adversely affecting system operation. The S/UNI-IMA-84/TEMUX-84 development kit is a Full Hot Swap board. Full Hot Swap boards have the minimum Hot Swap features plus the additional resources for software connection control. The following Full Hot Swap resources are provided to software executing on the external microprocessor:

- An ENUM# signal, which is an open collector (open drain) bussed signal, to signal a change in status for the board.

- A switch, actuated with the lower ejector handle, indicates the beginning of the extraction process or end of the insertion process.
- An LED to indicate the status of the software connection process.
- A set of four control and status bits on each board which allows the system host's software to determine the source of the ENUM# signal and control the LED.

This development kit employs a hot swap compatible CPCI bridge, PCI 9030, and a hot swap controller, the Linear Technology LTC1422. The CPCI connector is assembled with three different length pins, as required by the hot swap specification [PICMG 2.1 R1.0]. Supporting circuitry is also carefully designed to not impair the hot swap ability.

Please refer to the PCI 9030 data sheet and the CompactPCI® Hot Swap Specification, R1.0 for further details regarding these resources.

4.10.1 Power Supply with Hot Swap Controller

The power supply for the S/UNI-IMA-84/TEMUX-84 Development Kit is as shown in Figure 13. Integral to the circuit is the use of the LTC1422 Hot Swap Controller.

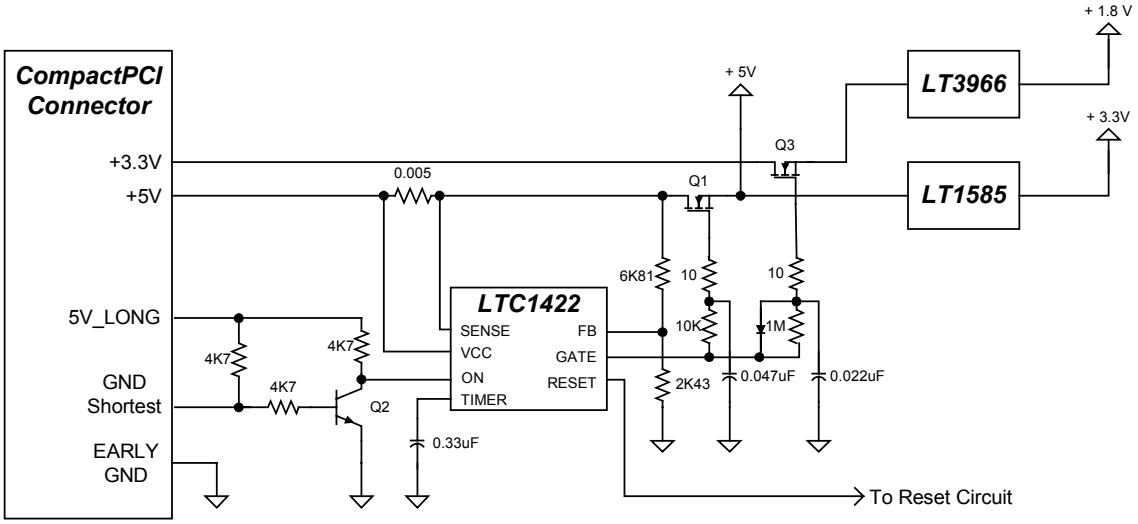

Figure 13 Power Supply with integrated hot swap circuitry

The S/UNI-IMA-84/TEMUX-84 Development Kit contains components that operate at 1.8V, 3.3V and 5V, referenced to ground. The 5V supply is provided

to the board through the CompactPCI connector. The 1.8V and 3.3V supplies are generated on the board via DC-DC voltage regulators.

It is required that 5V power is provided before both 1.8V and 3.3V power to avoid device latchup. Please refer to the respective data sheets of each device for further details regarding device power-up.

The first mating pins are 5V_LONG and Early GND. When these pins initially mate, Q2 saturates and the ON pin of the LTC1422 is held low. The LT1422 has yet to receive power, which keeps both MOSFETs open (off).

When the shortest pins mate with the backplane, GND_Shortest connecting to the base of Q2 causes Q2 to turn off and the ON pin then becomes logic high. The LTC1422 then begins to slowly ramp up the gate voltage for Q1 & Q3, causing the MOSFETS to gradually turn on, limiting the inrush current to the board to a safe level. This, in turn, causes the gate voltages on Q1 and Q3 to rise, turning the transistors on. Because the resistor and capacitor network used for Q3 is different than Q1, Q3 powers up with a 20 ms delay.

Once Q1 and Q3 turn on, the LP3966 is used to generate the +1.8V supply from the CompactPCI +3.3V line, while the LT1585 generates +3.3V from the CompactPCI +5V line. The board +5V supply is generated directly from the CompactPCI +5V line. The LP3966 is capable of supplying 3A, while the LT1585 can supply 4.6A.

Should the voltage across the 0.005 Ω resistor exceed 50 mV for more than 10 μs, an internal circuit breaker will trip, pulling the GATE output voltage to ground.

4.10.2 Ejector Handle and LED

The ejector handle has a built-in microswitch, which toggles when the ejector changes position. A blue LED signals the card's readiness for removal. When the ejector handle switch is opened the PCI9030 asserts *ENUM#* to inform the host CPU that the card is about to be removed. When the blue LED is turned on, the card may be safely removed.

4.11 CPCI Bridge Hardware Interfaces

4.11.1 CPCI System Bus Interface

The host processor located on an external board will access the PMC-Sierra devices located on-board through a CPCI connector. The serial EEPROM (SEEP) is used to store configuration information for the PCI 9030 bridge.

The system bus interface is a straightforward pin-to-pin connection between both the CPCI connector to the PCI 9030 and the SEEP to the PCI 9030. The system bus pins consist of interface control, address/data control and error reporting. For further functional description of each pin, please refer to any standard book covering PCI technology as well as the PCI 9030 and SEEP datasheet.

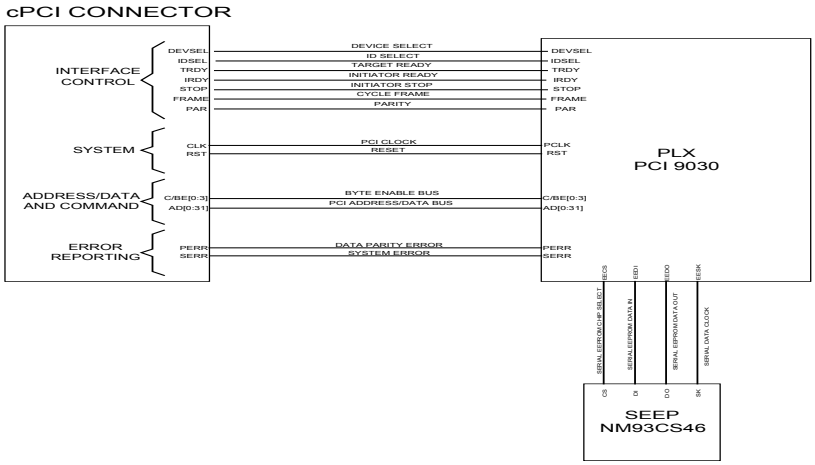

Figure 14 CPCI System Bus Interface Block Diagram

4.11.2 PCI 9030-Local Bus Interface

The PCI 9030 serves as a master device on the Local bus. Upon control from the external processor on the System side bus, the PCI 9030 sends the address and data out to the Local bus, while its control information is sent to the CPLD, which handles all decode logic and timing requirements for each PMC-Sierra device.

The PCI 9030 is configured to operate the Local Bus in non-multiplexed mode. Access to each PMC-Sierra device by the PCI 9030 is very similar in operation, with the difference between each access being the number of address and data

interface pins that each PMC-Sierra device microprocessor block contains, and the set-up and hold timing parameters.

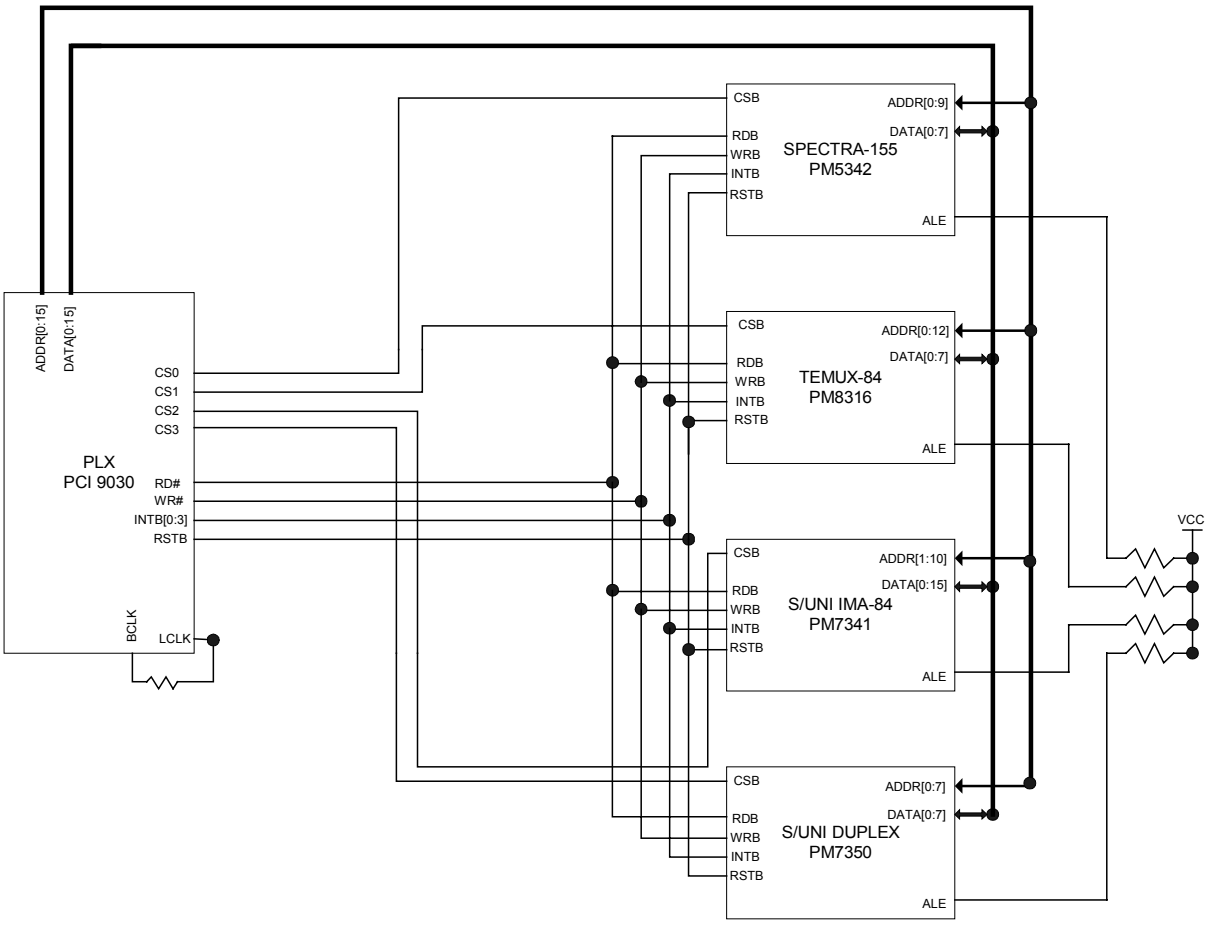

Figure 15 PCI 9030 Local Bus Interface Block Diagram

4.12 Oscillators

A 19.44 MHz ± 20ppm oscillator is required on the card to drive the Telecom bus and SBI bus. The CPLD will use this clock source to generate the 2 kHz synchronization pulse and other framing pulses.

A 37.056 MHz ± 32ppm oscillator is required on the card to drive the digital phase locked loop on the TEMUX-84 that performs jitter attenuation on the T1 recovered clocks.

A 49.152 MHz ± 32ppm oscillator is required on the card to drive the digital phase locked loop on the TEMUX-84 that performs jitter attenuation on the E1 recovered clocks.

A 51.84 oscillator is required on the card to generate a gapped DS3 clock for the TEMUX-84.

A 55 MHz oscillator is required on the card to drive the system clock of the S/UNI-IMA-84 for use with the external SDRAM device.

A 25 MHz oscillator is required on the card to drive the UTOPIA Level 2 bus.

5 ANALYSIS

5.1 INTERFACE TIMING

In the timing analysis figures of the section, a gray waveform indicates uncertainty, and a black waveform indicates an input that is not valid since more than one device may be driving the signal at that time. All times are measured in nanoseconds (ns).

5.1.1 SPECTRA-155 – TEMUX-84 Telecom DROP Bus

The Telecom DROP Bus is the ingress interface between SPECTRA-155 data and control outputs and TEMUX-84 data and control inputs. On the DROP bus, DCK provides timing to the SPECTRA-155 and LREFCLK provides timing to the TEMUX-84. These clocks need to be synchronized for correct operation of the bus. The Telecom bus is synchronized to a 19.44 MHz clock source. The AC1J1V1 signal is sampled on the rising edge of LREFCLK and indicates frame, payload and tributary multiframe boundaries. See Figure 16 below for a diagram of the Telecom drop bus timing.

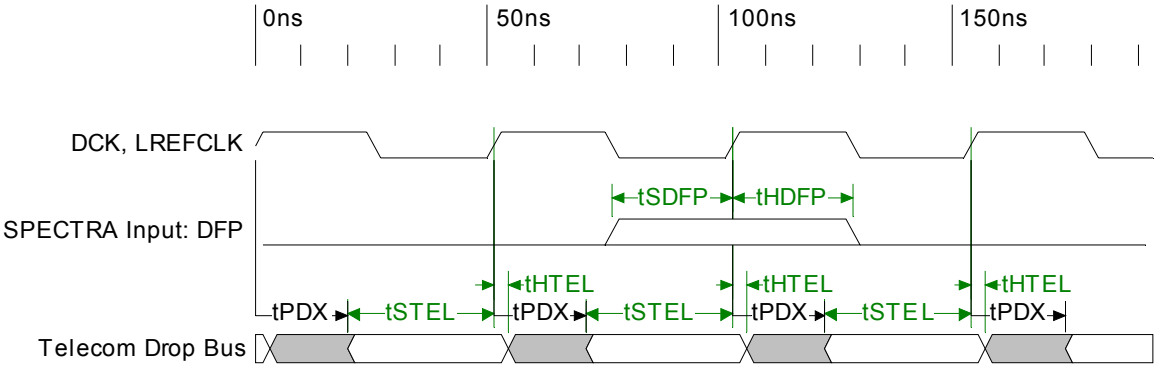

Figure 16 Telecom DROP Bus Timing Diagram

In reference to Figure 16, the sequence of events for one Telecom DROP bus clock cycle is as follows:

1. The SPECTRA-155 updates DD[7:0], DDP, DPL, and DC1J1V1 on the rising edge of DCK after a propagation delay, tP Dx.

2. On the next rising edge, the TEMUX-84 samples LDDATA[7:0], LDDP, LDPL, and LDC1J1V1 on the rising edge of LREFCLK. The TEMUX-84 inputs require a set-up time of tS TEL and a hold time of tH TEL relative to the rising edge of LREFCLK.

3. On the same rising edge of DCK, the SPECTRA-155 samples DFP. DFP requires a set-up time of tS DFP and a hold time of tH DFP.

The output propagation delays involved in Figure 16 are shown in the following table:

Table 3 Telecom Drop Bus Propagation Delays

Name	Device	Description	Min	Max
tP DX	SPECTRA-155	DCK High to Dx Valid	3	20

The input constraints involved in Figure 16 are shown in the following table:

Table 4 Telecom Drop Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS DFP	SPECTRA-155	DFP Set-up Time	5	25.72	20.72
tH DFP	SPECTRA-155	DFP Hold Time	1	25.72	24.72
tS TEL	TEMUX-84	Telecom Bus Set-up Time	5	31.44	26.44
tH TEL	TEMUX-84	Telecom Bus Hold Time	1	3	2

5.1.2 SPECTRA-155 – TEMUX-84 Telecom ADD Bus

The Telecom ADD Bus is the egress interface between SPECTRA data and control inputs and TEMUX data and control outputs. See Figure 17 below for a diagram of the Telecom ADD bus timing.

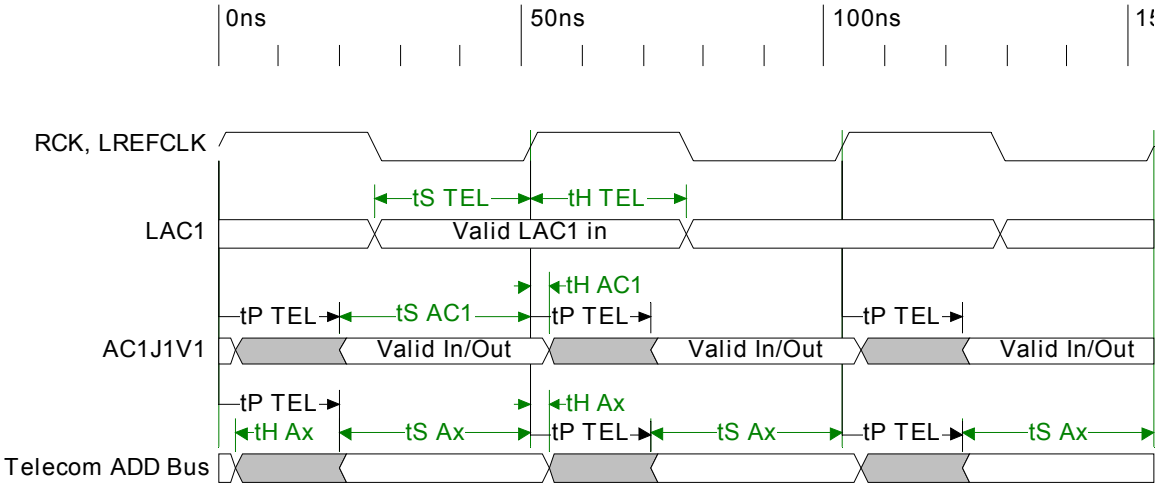

Figure 17 Telecom ADD Bus Timing Diagram

In reference to Figure 17, the sequence of events for one Telecom ADD bus clock cycle is as follows:

1. The TEMUX-84 updates LADATA[7:0], LADP, and LAPL on the falling edge of LREFCLK after a propagation delay, tP TEL.

2. On the next rising edge, SPECTRA samples AD[7:0], ADP, and APL on the rising edge of ACK. These SPECTRA inputs require a set-up time of tS Ax and a hold time of tH Ax relative to the rising edge of ACK.

3. On the same rising edge of LREFCLK, the TEMUX-84 samples LAC1. LAC1 requires a set-up time of tS TEL and a hold time of tH TEL.

The output propagation delays involved in Figure 17 are shown in the following table:

Table 5 Telecom Add Bus Propagation Delays

Name	Device	Description	Min	Max
tP TELOE	TEMUX-84	LREFCLK to Tristateable Outputs going Valid from Tristate	0	13
tZ TEL	TEMUX-84	LREFCLK to Tristateable Outputs going Tristate	3	20
tP TEL	TEMUX-84	LREFCLK to Output Valid	3	20

The input constraints involved in Figure 17 are shown in the following table:

Table 6 Telecom Add Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS TEL	SPECTRA-155	Telecom Bus Set-up Time	5	25.72	20.72
tH TEL	SPECTRA-155	Telecom Bus Hold Time	1	25.72	24.72
tS Ax	SPECTRA-155	Ax Set-up Time	5	31.44	26.44
tH Ax	SPECTRA-155	Ax Hold Time	1	3	2
tS AC1	TEMUX-84	AC1J1V1 Set-up Time	5	31.44	26.44
tH AC1	TEMUX-84	AC1J1V1 Hold Time	1	3	2

5.1.3 TEMUX-84 – S/UNI-IMA-84 SBI ADD Bus Interface

The SBI ADD Bus is the egress interface between S/UNI-IMA-84 data and control outputs and TEMUX-84 data and control inputs. On the ADD bus, SREFCLK provides timing to the TEMUX-84 and REFCLK provides timing to the S/UNI-IMA-84. These clocks need to be synchronized for correct operation of the bus.

The C1FP frame pulse indicates SBI bus multiframe alignment, which occurs every 500 µs. Therefore, this signal is pulsed every 9720 SREFCLKs. In this reference design, C1FP is generated from the SDC1FP pin of the TEMUX-84.

In reference to Figure 18, the S/UNI-IMA-84 outputs are ADATA[7:0], ADP, APL, AC1FP, and AV5. The corresponding TEMUX-84 inputs are SADATA[7:0], SADP, SAPL, SAC1FP, and SAV5. Please see the Pin Description and Functional Timing sections of the device datasheets for the functional description of these signals.

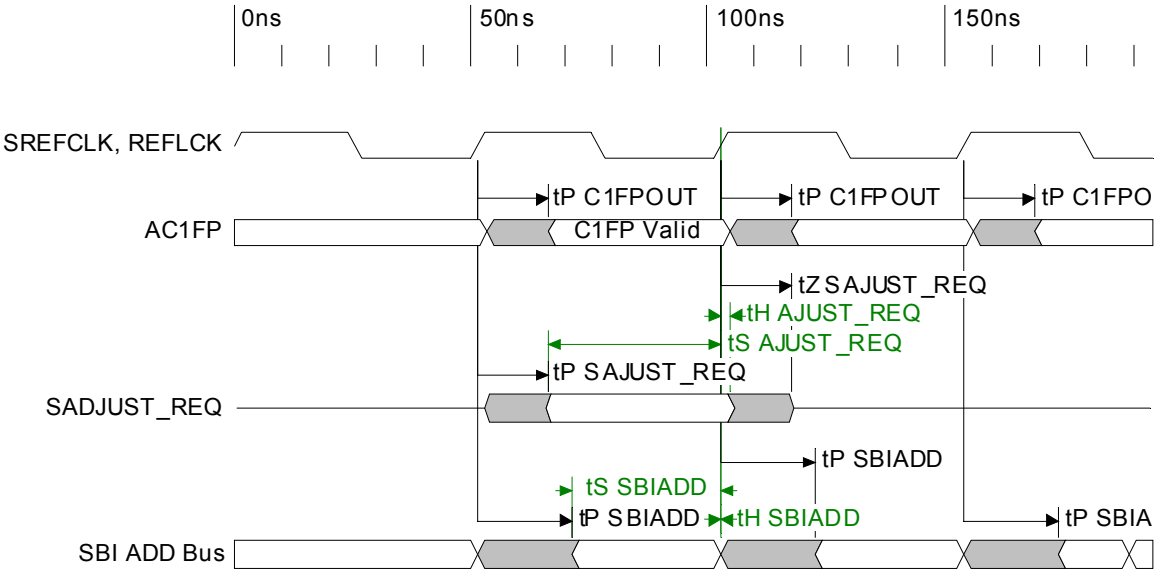

Figure 18 SBI ADD Bus Timing Analysis

In reference to Figure 18, the sequence of events for one SBI ADD bus clock cycle is as follows:

1. S/UNI-IMA-84 updates ADATA[7:0], ADP, APL, and AV5 on the rising edge of REFCLK after a propagation delay, tP SBIADD.

2. On the same rising edge, TEMUX-84 updates C1FPOUT after a propagation delay, tP SDC1FP.

3. The AJUST_REQ signal is asserted by the TEMUX-84 to control the data rate of the S/UNI-IMA-84.

4. On the next rising edge of SREFCLK, TEMUX-84 samples SADATA[7:0], SADP, SAPL, and SAV5. These TEMUX-84 inputs require a set-up time of tS SBIADD and a hold time of tH SBIADD relative to the rising edge of SREFCLK.

5. On the same edge, the S/UNI-IMA-84 samples the SAJUST_REQ signal. The SAJUST_REQ signal requires a setup time of tSAJUST and a hold time of tHSAJUST

The output propagation delays involved in Figure 18 are shown in the following table:

Table 7 SBI Add Bus Propagation Delays

Name	Device	Description	Min	Max
tP SBIADD	S/UNI-IMA-84	REFCLK to SBI ADD Bus Outputs Valid	0	20
tP SAJUST_REQ	TEMUX-84	SREFCLK to SAJUST_REQ Valid	2	15
tZ SAJUST_REQ	TEMUX-84	SREFCLK to SAJUST_REQ Tri-state	2	15

The input constraints involved in Figure 18 are shown in the following table:

Table 8 SBI Add Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AJUST	S/UNI-IMA-84	SAJUST_REQ Set-up Time to SREFCLK	4	36.44	32.44
tH AJUST	S/UNI-IMA-84	SAJUST_REQ Hold Time to SREFCLK	0	2	2
tS SBIADD	TEMUX-84	SBI ADD Bus Inputs Set-up Time to SREFCLK	4	31.44	27.44
tH SBIADD	TEMUX-84	SBI ADD Bus Inputs Hold Time from SREFCLK	0	0	0

5.1.4 TEMUX-84 – S/UNI-IMA-84 SBI DROP Bus Interface

The SBI DROP Bus is the ingress interface between TEMUX-84 data and control outputs and S/UNI-IMA-84 data and control inputs. On the DROP bus, SREFCLK provides timing to the TEMUX-84 and REFCLK provides timing to the

S/UNI-IMA-84. These clocks need to be synchronized for correct operation of the bus.

The C1FP frame pulse indicates SBI bus multiframe alignment, which occurs every 500 µs. Therefore, this signal is pulsed every 9720 SREFCLKs. In this reference design, C1FP is generated from the SDC1FP pin of the TEMUX-84.

In reference to Figure 19, theTEMUX-84 outputs are SDDATA[7:0], SDDP, SDPL, and SDV5. The corresponding S/UNI-IMA-84 inputs are DDATA[7:0], DDP, DPL, and DV5. Please see the Pin Description and Functional Timing sections of the device datasheets for the functional description of these signals.

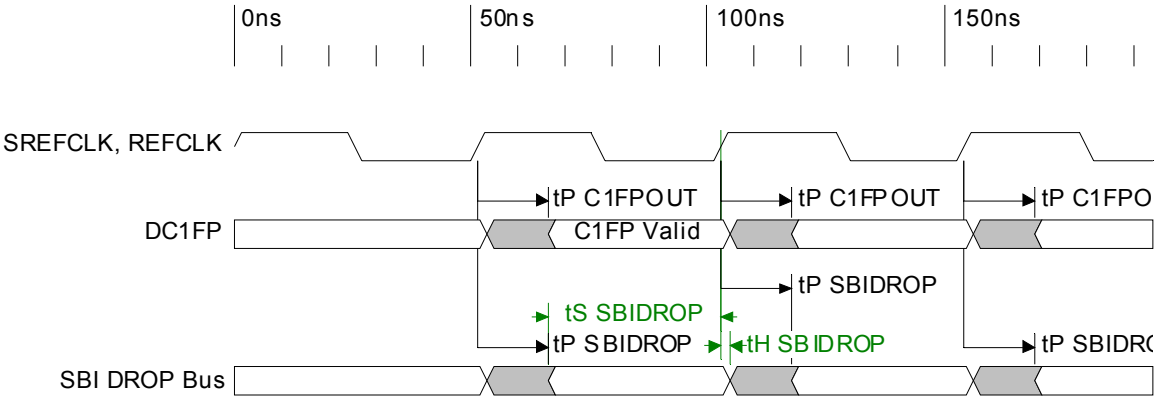

Figure 19 SBI DROP Bus Timing Analysis

In reference to Figure 19, the sequence of events for one SBI DROP bus clock cycle is as follows:

1. On the rising edge of REFCLK, TEMUX-84 updates SDDATA[7:0], SDDP, SDPL, and SDV5 after a propagation delay, tP SBIDROP.

2. On the same edge, TEMUX-84 updates C1FP after a propagation delay, tP SDC1FP.

3. On the next rising edge of SREFCLK, S/UNI-IMA-84 samples DDATA[7:0], DDP, DPL, and DV5. These S/UNI-IMA-84 inputs require a set-up time of tS SBIDROP and a hold time of tH SBIDROP relative to the rising edge of SREFCLK.

The output propagation delays involved in Figure 19 are shown in the following table:

Table 9 SBI DROP Bus Propagation Delays

Name	Device	Description	Min	Max

Name	Device	Description	Min	Max
tP SBIDROP	TEMUX-84	REFCLK to SBI DROP Bus Outputs Valid	0	20
tP SDC1FP	TEMUX-84	SREFCLK to C1FP Valid	2	15

The input constraints involved in Figure 19 are shown in the following table:

Table 10 SBI DROP Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS SBIDROP	S/UNI-IMA-84	SBI DROP Bus Inputs Set-up Time to SREFCLK	4	31.44	27.44
tH SBIDROP	S/UNI-IMA-84	SBI DROP Bus Inputs Hold Time from SREFCLK	0	0	0

5.1.5 S/UNI-IMA-84 – S/UNI-DUPLEX UTOPIA Level 2 TRANSMIT Bus Interface

The UTOPIA Level 2 is used as the standard for communication between the PHY to ATM layer device in this development kit. The PHY device being the S/UNI-IMA-84 and the ATM layer device being the S/UNI-DUPLEX. In the egress direction the S/UNI-DUPLEX will present the ATM cells, which will be mapped into multiple links by the S/UNI-IMA-84. Conversely, in the ingress direction the S/UNI-IMA-84 will extract the ATM cells from their respective links and present the ATM cells to the S/UNI-DUPLEX to be processed.

This bus interface is configured to be a byte-wide interface with synchronous timing provided by an external 19.44MHz oscillator to each device's respective reference bus clock pins.

The UTOPIA L2 Transmit Bus is the egress interface between S/UNI-IMA-84 data and control inputs and S/UNI-DUPLEX data and control outputs. As a bus master, the S/UNI-DUPLEX will continuously poll the Transmit Cell Available (TCA) status line of the S/UNI-IMA-84 for which it has a downstream cell buffered. When the S/UNI-IMA-84 has room (ie. TCA is asserted), the S/UNI-DUPLEX sends the next buffered cell to the PHY over the UTOPIA L2 bus.

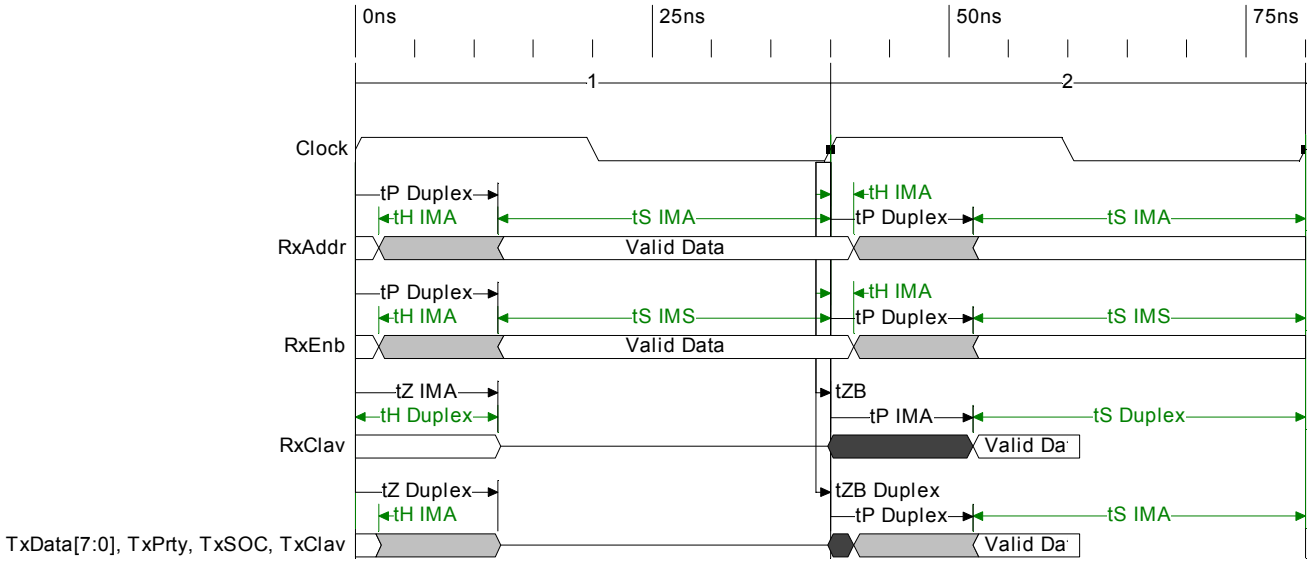

Figure 20 UTOPIA L2 Bus Transmit Timing Diagram

In reference to Figure 20, the sequence of events for one UTOPIA Level 2 bus cycle is as follows:

1. On the rising edge of RxClk, signals RxAddr and RxEnb are updated by the S/UNI-DUPLEX after the propagation delay tP Duplex.

2. On the next rising edge of RxClk, the S/UNI-IMA-84 reads the data from the signals RxAddr and RxEnb. The S/UNI-IMA-84 requires that the data be valid during the setup time tS IMA and the hold time tH IMA. In addition, the S/UNI-IMA-84 can update RxClav after a propagation delay tP IMA.

3. Also on the same edge, the S/UNI-DUPLEX may update RxData[7:0], RxPrty, and RxSOC after a propagation delay tP Duplex.

4. On the next rising edge of RxClk, the S/UNI-IMA-84 reads the data from the signals RxData[7:0], RxPrty, RxSOC, and RxClav. The S/UNI-IMA-84 requires that the data be valid during the setup time tS IMA and the hold time tH IMA. In addition, the S/UNI-IMA-84 can update RxClav after a propagation delay tP IMA.

The output propagation delays involved in Figure 20 are shown in the following table:

Table 11 UTOPIA L2 Transmit Bus Propagation Delays

Name	Device	Description	Min	Max
tP Duplex	S/UNI-Duplex	Clock high to data valid	2	12
tZ Duplex	S/UNI-IMA-84	Clock high to output high impedence	2	12
tP Ima	S/UNI-IMA-84	Clock high to data valid		12
tZ Ima	S/UNI-IMA-84	Clock high to output high impedence		12
tZB	S/UNI-IMA-84	Clock high to output driven	0	

The input constraints involved in Figure 20 are shown in the following table:

Table 12 UTOPIA L2 Transmit Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS IMA	S/UNI-IMA-84	IMA Setup Time	4	18.3	14.3
tH IMA	S/UNI-IMA-84	IMA Hold Time	0	2	2
tS Duplex	S/UNI-Duplex	DUPLEX Setup Time	3	16.3	13.3
tH Duplex	S/UNI-Duplex	DUPLEX Hold Time	1	12	11

5.1.6 S/UNI-IMA-84 – S/UNI-DUPLEX UTOPIA Level 2 RECEIVE Bus Interface

The UTOPIA L2 Receive Bus is the ingress interface between the S/UNI-IMA-84 data and control outputs and the S/UNI-DUPLEX data and control inputs. As a bus master, the S/UNI-DUPLEX will continuously poll the Receive Cell Available (RCA) status line of the S/UNI-IMA-84, reading the cells from the S/UNI-IMA-84 as they become available. Once a cell is brought into the S/UNI-DUPLEX, the cell is tagged (via a prepend byte) with the appropriate PHY ID (0:31), and sent out simultaneously to the LVDS links.

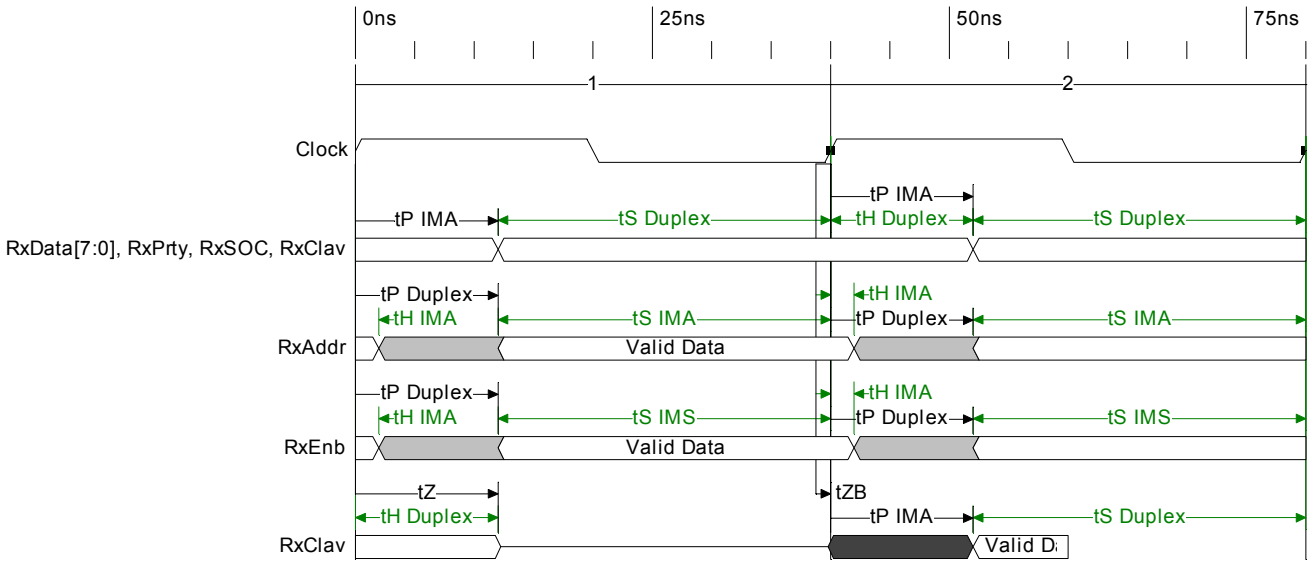

Figure 21 UTOPIA L2 Bus Receive Timing Diagram

In reference to Figure 21, the sequence of events for one UTOPIA Level 2 bus cycle is as follows:

1. On the rising edge of RxClk, signals RxAddr and RxEnb are updated by the S/UNI-DUPLEX after the propagation delay tP Duplex.

2. On the next rising edge of RxClk, the S/UNI-IMA-84 reads the data from the signals RxAddr and RxEnb. The S/UNI-IMA-84 requires that the data be valid during the setup time tS IMA and the hold time tH IMA.

3. Also on the same edge, the S/UNI-IMA-84 may update RxData[7:0], RxPrty, RxSOC, and RxClav after a propagation delay tP IMA.

4. On the next rising edge of RxClk, the S/UNI-DUPLEX reads the data from the signals RxData[7:0], RxPrty, RxSOC, and RxClav.

The output propagation delays involved in Figure 21 are shown in the following table:

Table 13 UTOPIA L2 Receive Bus Propagation Delays

Name	Device	Description	Min	Max
tP Duplex	S/UNI-Duplex	Clock high to data valid	2	12
tP Ima	S/UNI-IMA-84	Clock high to data valid		12
tZ	S/UNI-IMA-84	Clock high to output high impedance		12
tZB	S/UNI-IMA-84	Clock high to output driven	0	

The input constraints involved in Figure 21 are shown in the following table:

Table 14 UTOPIA L2 Transmit Bus Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS IMA	S/UNI-IMA-84	IMA Setup Time	4	18.3	14.3
tH IMA	S/UNI-IMA-84	IMA Hold Time	0	2	2
ts Duplex	S/UNI-Duplex	DUPLEX Setup Time	3	16.3	13.3
tH IMA	S/UNI-IMA-84	DUPLEX Hold Time	1	12	11

5.1.7 PCI 9030 Timing Diagrams

Timing specifications for the PCI 9030 that are specific to the microprocessor interface for the S/UNI-IMA-84/TEMUX-84 Development Kit is reproduced here.

Table 15 PCI 9030 AC Timing (Local Inputs) Electrical Characteristics

Symbol	Signal Name	tSETUP	tHOLD	Units
LAD[0:31]	Address/Data Bus	5.0	1.0	Ns
LD[0:31]	Data Bus	5.0	1.0	Ns
READY#	Local Ready Input	7.0	1.0	Ns

Table 16 PCI 9030 AC Timing (Local Outputs) Electrical Characteristics

Symbol	Signal Name	tLOUT	Units
ADS#	Address Strobe	10.0	Ns
CS[0:3]	Chip Select	10.0	Ns
LA[2:27]	Address Bus	10.0	Ns
LD[0:31]	Data Bus	10.0	Ns
RD#	Read Strobe	10.0	Ns
WR#	Write Strobe	10.0	Ns

Maximum output propagation delays are measured with a 50pF load on the outputs.

The following sections describe the timing analysis performed for both read and write accesses to each PMC-Sierra device.

Note that all timing margin requirements are met in the timing diagrams for each microprocessor read and write to PMC-Sierra devices.

5.1.7.1 TEMUX-84 READ Operation

The host processor can access the registers on the TEMUX-84 device via the PCI 9030 Target Interface Device. The read access of the TEMUX-84 is shown below.

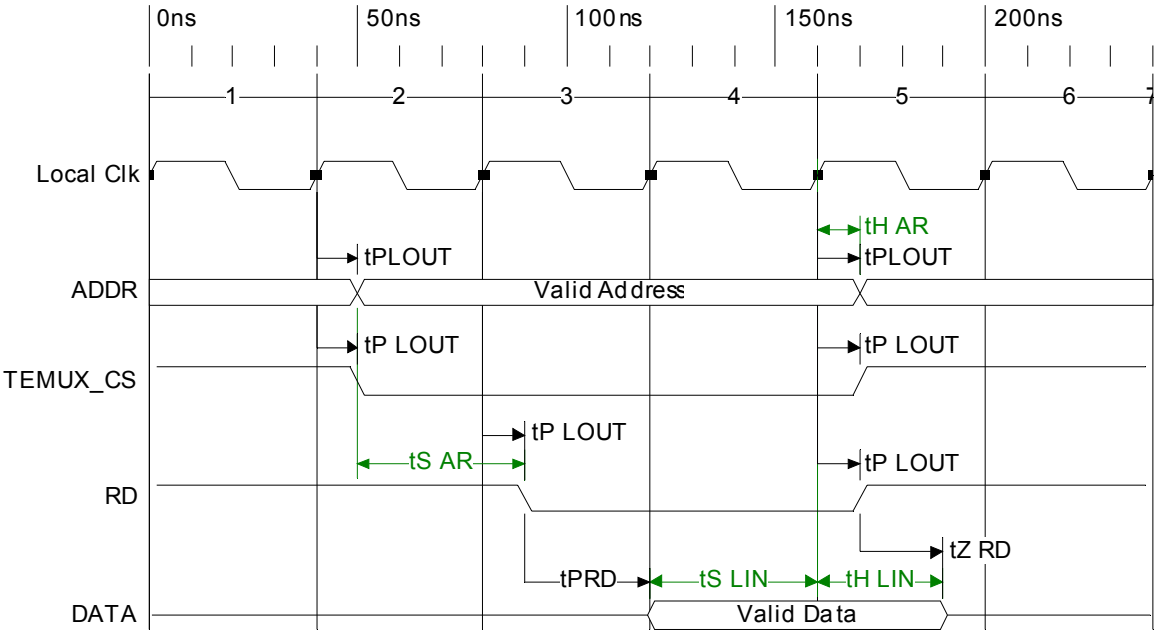

Figure 22 TEMUX-84 read cycle timing

In reference to Figure 22, the sequence of events for the PCI 9030 to read data from any TEMUX-84 is as follows:

1. On the rising edge of clock cycle 2, the PCI 9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

2. On the rising edge of clock cycle 3, the PCI 9030 asserts the RD signal after a propagation delay of tP LOUT. The cycle in which the RD signal is asserted is set by the Read Strobe Delay bits in the LAS1BRD register of the PCI 9030. For this interface, the value is 1.

3. After the propagation delay tP RD, the TEMUX-84 puts valid data on the data bus. At the start of cycle 5, The PCI 9030 reads the data from the data bus. The PCI 9030 inputs require a setup time of tS LIN and a hold time of tH LIN. Note that the PCI 9030 waits 1 cycle for the data to be placed on the data bus, this delay is set by the NRAD bits in LAS1BRD.

4. Also at the start of cycle 5, the PCI 9030 de-asserts the RD, TEMUX_CS, and address lines after the propagation delay, tP LOUT. The de-assertion of the RD signal causes the TEMUX-84 data bus to tristate after a propagation delay tZ RD.

The output propagation delays involved in Figure 22 are shown in the following table:

Table 17 PCI 9030 to TEMUX-84 Read Propagation Delays

Name	Device	Description	Min	Max
tP LOUT	PCI 9030	Local Clock edge to Local output delay	-	10
tP RD	TEMUX-84	RD to valid data delay	-	30
tZ RD	TEMUX-84	RD negated to data tristate delay	-	20

The input constraints involved in Figure 22 are shown in the following table:

Table 18 PCI 9030 to TEMUX-84 Read Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AR	TEMUX-84	Address to valid read setup	10	40	30
tH AR	TEMUX-84	Address to valid read hold	5	10	5
tS LIN	PCI 9030	Input setup time	5	40	35
tH LIN	PCI 9030	Input hold time	1	30	29

5.1.7.2 TEMUX-84 WRITE Operation

The write access of the TEMUX-84 is shown below.

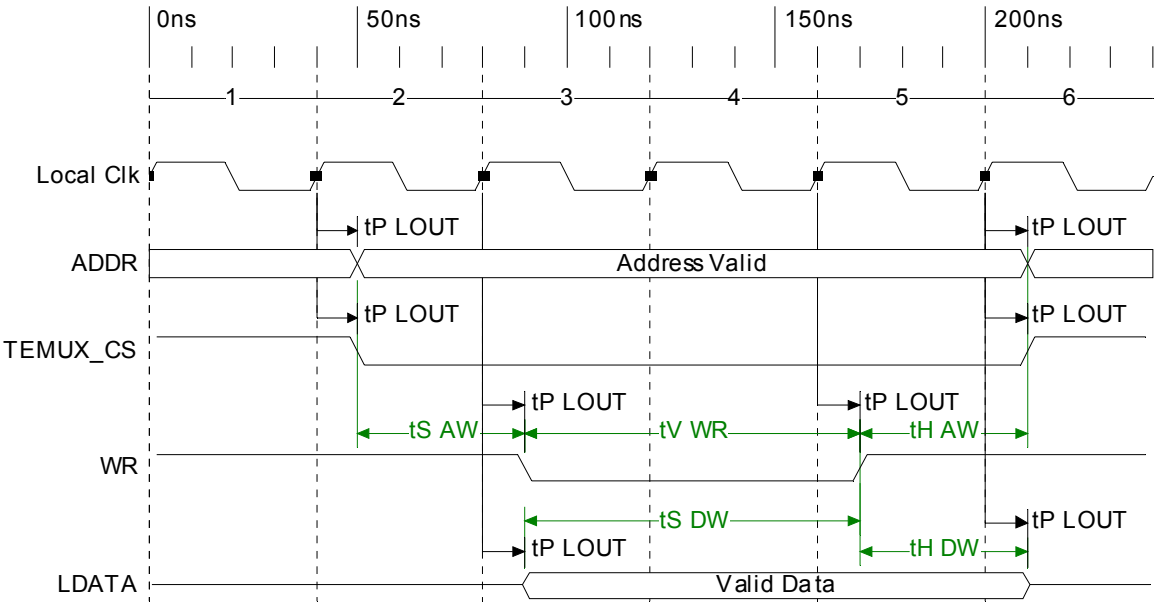

Figure 23 TEMUX-84 write cycle timing

In reference to Figure 23, the sequence of events for the PCI 9030 to write data to the TEMUX-84 is as follows:

1. On the rising edge of clock cycle 2, the PCI 9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

2. On the rising edge of clock cycle 3, the PCI 9030 puts valid data on the data bus and asserts the WR signal after a propagation delay of tP LOUT. The cycle in which the WR signal is asserted is set by the Write Strobe Delay bits in the LAS1BRD register of the PCI 9030. For this interface, the value is 1. This delay is required to satisfy tS AW, the address to write setup time.

3. The TEMUX-84 inputs require the data to be present for a setup time of tS DW. To satisfy these requirements, the PCI 9030 waits 1 cycle with valid data on the data bus. The NWDD bits in LAS1BRD set the wait delay. This wait delay also satisfies tV WR, the Valid Write Pulse width.

4. On the rising edge of clock cycle 5, the PCI 9030 deasserts the WR signal after a propagation delay of tP LOUT. This causes the TEMUX-84 to latch the data from the bus. The data must remain present on the bus for an additional tH DW. This is accomplished by setting the Write Cycle Hold bits in LAS1BRD to 1. The write cycle hold causes DATA, TEMUX_CS, and ADDR to stay active until the rising edge of cycle 6, when they deassert after tP LOUT.

The output propagation delays involved in Figure 23 are shown in the following table:

Table 19 PCI 9030 to TEMUX-84 Write Propagation Delays

Name	Device	Description	Min	Max
tP LOUT	PCI 9030	Local Clock edge to Local output delay	-	10

The input constraints involved in Figure 23 are shown in the following table:

Table 20 PCI 9030 to TEMUX-84 Write Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AW	TEMUX-84	Address to valid write set-up	10	40	30
tV WR	TEMUX-84	Valid write pulse width	40	80	40
tH AW	TEMUX-84	Address to valid write hold	5	40	35
tS DW	TEMUX-84	Data to valid write set-up	20	80	60
tH DW	TEMUX-84	Data to valid write hold	5	40	35

5.1.7.3 S/UNI-DUPLEX READ Operation

The host processor can access the registers on the S/UNI-DUPLEX device via the PCI 9030 Target Interface Device. The read access of the S/UNI-DUPLEX is shown below.

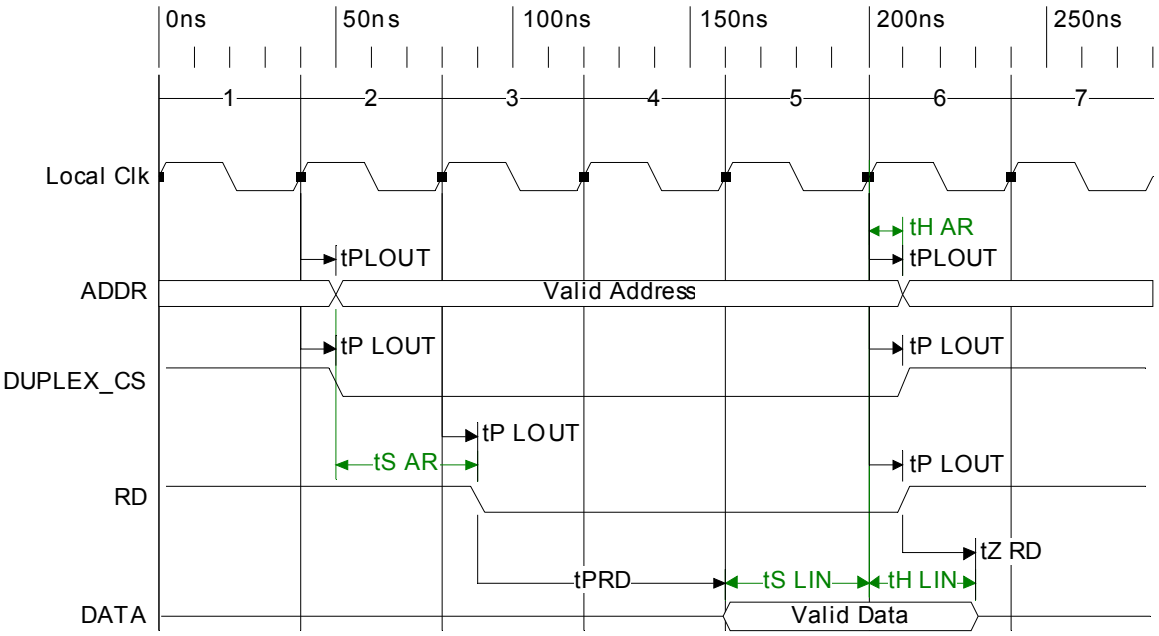

Figure 24 S/UNI-DUPLEX READ Timing Diagram

In reference to Figure 24, the sequence of events for the PCI 9030 to read data from any S/UNI-DUPLEX is as follows:

5. On the rising edge of clock cycle 2, the PCI 9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

6. On the rising edge of clock cycle 3, the PCI 9030 asserts the RD signal after a propagation delay of tP LOUT. The cycle in which the RD signal is asserted is set by the Read Strobe Delay bits in the LAS1BRD register of the PCI 9030. For this interface, the value is 1.

7. After the propagation delay tP RD, the S/UNI-DUPLEX puts valid data on the data bus. At the start of cycle 6, The PCI 9030 reads the data from the data bus. The PCI 9030 inputs require a setup time of tS LIN and a hold time of

tH LIN. Note that the PCI 9030 waits 2 cycles for the data to be placed on the data bus, this delay is set by the NRAD bits in LAS1BRD.

8. Also at the start of cycle 6, the PCI 9030 de-asserts the RD, DUPLEX _CS, and address lines after the propagation delay, tP LOUT. The de-assertion of the RD signal causes the S/UNI-DUPLEX data bus to tristate after a propagation delay tZ RD.

The output propagation delays involved in Figure 24 are shown in the following table:

Table 21 PCI 9030 to S/UNI-DUPLEX Read Propagation Delays

Name	Device	Description	Min	Max
tP LOUT	PCI 9030	Local Clock edge to Local output delay	-	10
tP RD	S/UNI-DUPLEX	RD to valid data delay	-	70
tZ RD	S/UNI-DUPLEX	RD negated to data tristate delay	-	20

The input constraints involved in Figure 24 are shown in the following table:

Table 22 PCI 9030 to S/UNI-DUPLEX Read Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AR	S/UNI-DUPLEX	Address to valid read setup	10	40	30
tH AR	S/UNI-DUPLEX	Address to valid read hold	5	10	5
tS LIN	PCI 9030	Input setup time	5	40	35
tH LIN	PCI 9030	Input hold time	1	30	29

5.1.7.4 S/UNI-DUPLEX WRITE Operation

The write access of the S/UNI-DUPLEX is shown below.

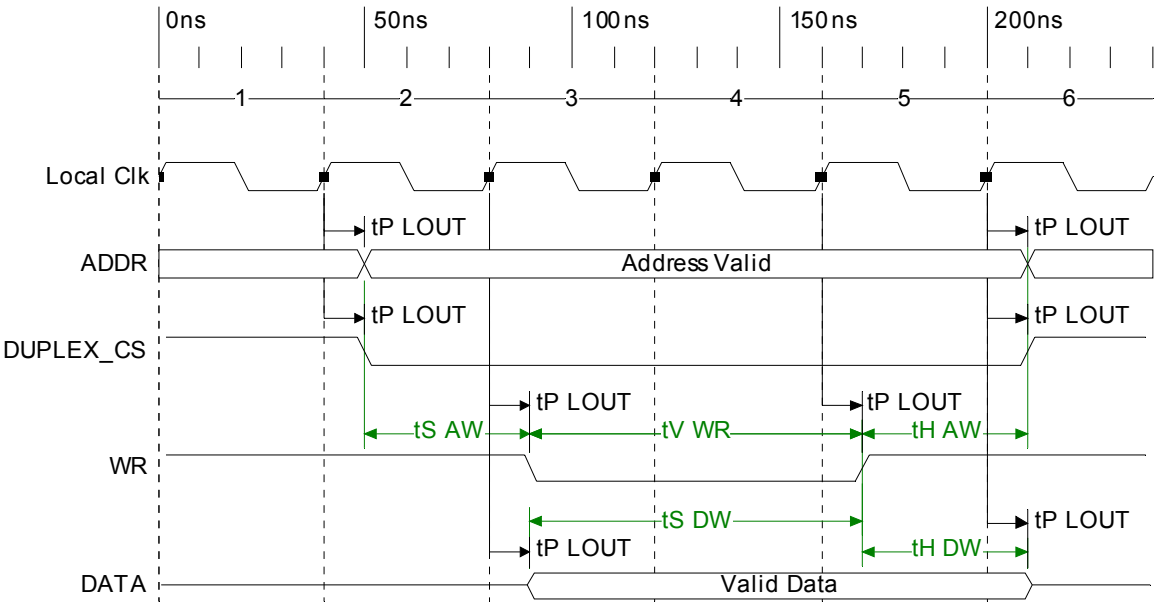

Figure 25 S/UNI-DUPLEX WRITE Timing Diagram

In reference to Figure 25, the sequence of events for the PCI 9030 to write data to the S/UNI-DUPLEX is as follows:

5. On the rising edge of clock cycle 2, the PCI 9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

6. On the rising edge of clock cycle 3, the PCI 9030 puts valid data on the data bus and asserts the WR signal after a propagation delay of tP LOUT. The cycle in which the WR signal is asserted is set by the Write Strobe Delay bits in the LAS1BRD register of the PCI 9030. For this interface, the value is 1. This delay is required to satisfy tS AW, the address to write setup time.

7. The S/UNI-DUPLEX inputs require the data to be present for a setup time of tS DW. To satisfy these requirements, the PCI 9030 waits 2 cycles with valid data on the data bus. The NWDD bits in LAS1BRD set the wait delay. This wait delay also satisfies tV WR, the Valid Write Pulse width.

8. On the rising edge of clock cycle 5, the PCI 9030 deasserts the WR signal after a propagation delay of tP LOUT. This causes the S/UNI-DUPLEX to latch the data from the bus. The data must remain present on the bus for an additional tH DW. This is accomplished by setting the Write Cycle Hold bits in LAS1BRD to 1. The write cycle hold causes DATA, DUPLEX _CS, and ADDR to stay active until the rising edge of cycle 6, when they deassert after tP LOUT.

The output propagation delays involved in Figure 23 are shown in the following table:

Table 23 PCI 9030 to S/UNI-DUPLEX Write Propagation Delays

Name	Device	Description	Min	Max
tP LOUT	PCI 9030	Local Clock edge to Local output delay	-	10

The input constraints involved in Figure 23 are shown in the following table:

Table 24 PCI 9030 to S/UNI-DUPLEX Write Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AW	S/UNI-DUPLEX	Address to valid write set-up	10	40	30
tV WR	S/UNI-DUPLEX	Valid write pulse width	40	80	40
tH AW	S/UNI-DUPLEX	Address to valid write hold	5	40	35
tS DW	S/UNI-DUPLEX	Data to valid write set-up	20	80	60
tH DW	S/UNI-DUPLEX	Data to valid write hold	5	40	35

5.1.7.5 S/UNI-IMA-84 READ/WRITE Operation

PCI 9030 read/write access to the S/UNI-IMA-84 device is identical to that of read/write access to the S/UNI-DUPLEX device in terms of the timing requirements. The difference between these two operations for each device is the size of the address and data bus with which each device communicates with the PCI 9030. S/UNI-IMA-84 contains a 10-bit address bus and a 16-bit data bus, while the S/UNI-DUPLEX contains an 8-bit address and 8-bit data bus.

5.1.7.6 SPECTRA-155 READ Operation

PCI 9030 read access to the SPECTRA-155 device is similar to that of read access to the TEMUX-84. However, there are a few important differences. First, the data propagation delay is longer, requiring a maximum of 80 ns, as opposed to 40 ns for the TEMUX-84. Also, the address set up time requirement; T_{SAR} is 25 ns, as opposed to 10 ns. To facilitate these differences, PCI 9030 chip select CS2 is used to generate chip selects for the SPECTRA-155. Using CS2 allows 2 wait states to be inserted for both read and write operations.

A timing diagram for PCI 9030 read access to the SPECTRA-155 is presented in Figure 26. Note that all set-up and hold time requirements are met.

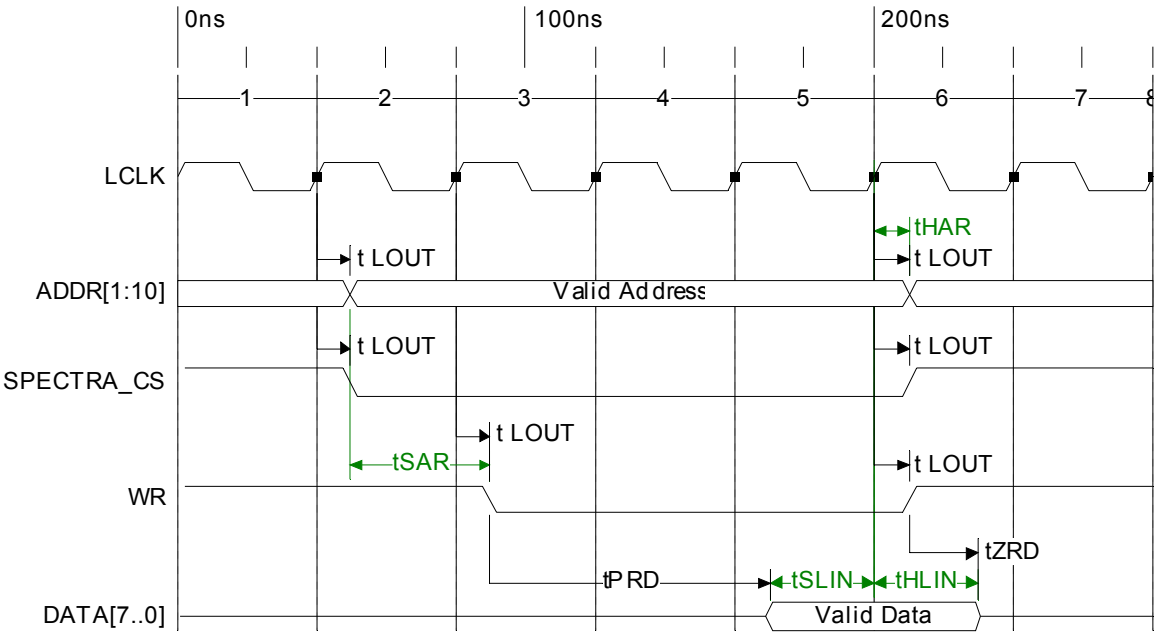

Figure 26 SPECTRA-155 read cycle timing

In reference to Figure 26, the sequence of events for the PCI 9030 to read data from the SPECTRA-622 is as follows:

1. On the rising edge of clock cycle 2, the PCI 9030 outputs the required address and the appropriate chip select after a propagation delay of tPLOUT.

2. On the rising edge of clock cycle 3, the PCI 9030 asserts the RD signal after a propagation delay of tPLOUT. The cycle in which the RD signal is asserted

is set by the Read Strobe Delay bits in the LAS0BRD register of the PCI 9030. For this interface, the value is 1.

3. After the propagation delay tPRD, the SPECTRA-155 puts valid data on the data bus. At the start of cycle 6, The PCI 9030 reads the data from the data bus. The PCI 9030 inputs require a setup time of tSLIN and a hold time of tHLIN. Note that the PCI 9030 waits 5 cycles for the data to be placed on the data bus; the NRAD bits in LAS0BRD set this delay.

4. Also at the start of cycle 6, the PCI 9030 de-asserts the RD, CS, and address lines after the propagation delay, tPLOUT. The de-assertion of the RD signal causes the SPECTRA-155 data bus to tristate after a propagation delay tZRD.

The output propagation delays involved in Figure 26 are shown in the following table:

Table 25 PCI 9030 to SPECTRA-155 Read Propagation Delays

Name	Device	Description	Min	Max
tLOUT	PCI 9030	Local Clock edge to Local output delay	N/A	10
tPRD	SPECTRA-155	RD to valid data delay	N/A	80
TZRD	SPECTRA-155	RD negated to data tristate delay	N/A	20

The input constraints involved in Figure 26 are shown in the following table:

Table 26 PCI 9030 to SPECTRA-155 Read Timing Constraints

Name	Device	Description	Min	Actual	Margin
tSAR	SPECTRA-155	Address to valid read setup	25	40	15
tHAR	SPECTRA-155	Address to valid read hold	5	10	5
tSLIN	PCI 9030	Input setup time	5	30	25
tHLIN	PCI 9030	Input hold time	1	30	29

5.1.7.7 SPECTRA-155 WRITE Operation

The PCI 9030 write interface to the SPECTRA-155 device is similar in operation to write access to the TEMUX-84, with the exception that CS2B is used rather that CS3B (as noted in section 6.1.5.6).

Figure 27 presents the SPECTRA-155 write cycle timing diagram.

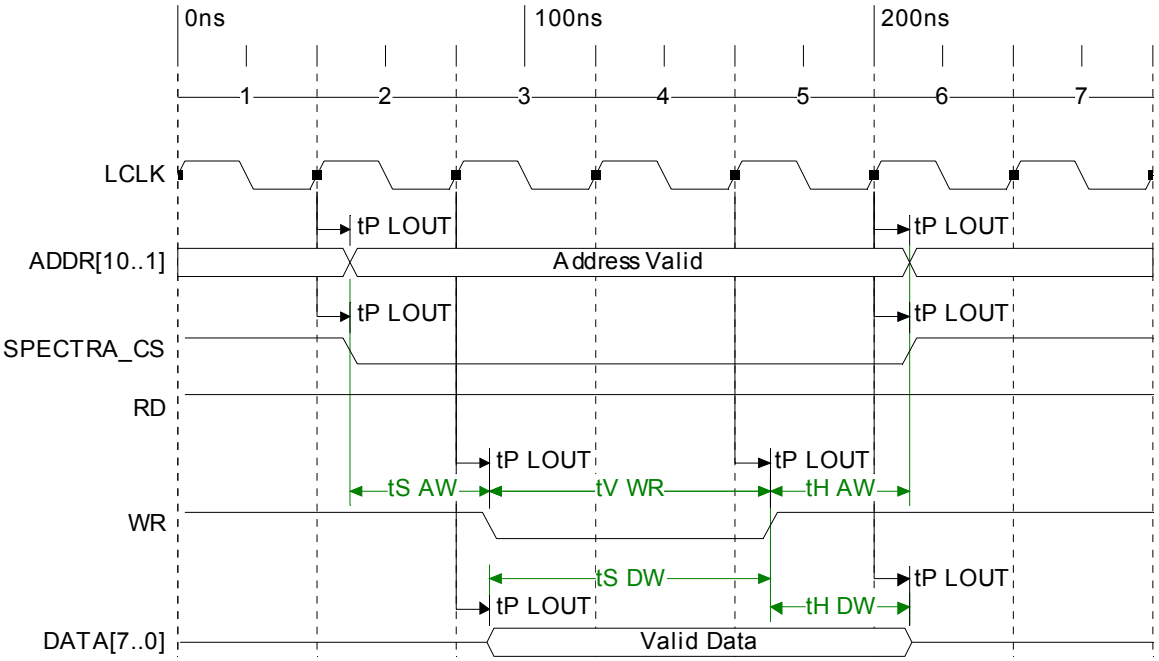

Figure 27 SPECTRA-155 write cycle timing

In reference to Figure 27, the sequence of events for the PCI 9030 to write data to the SPECTRA-155 is as follows:

1. On the rising edge of clock cycle 2, the PCI 9030 outputs the required address and the appropriate chip select after a propagation delay of tP LOUT.

2. On the rising edge of clock cycle 3, the PCI 9030 puts valid data on the data bus and asserts the WR signal after a propagation delay of tP LOUT. The cycle in which the WR signal is asserted is set by the Write Strobe Delay bits in the LAS0BRD register of the PCI 9030. For this interface, the value is 1. This delay is required to satisfy tS AW, the address to write setup time.

3. The SPECTRA-155 inputs require the data to be present for a setup time of tS DW and a hold time of tH DW. To satisfy these requirements, the PCI 9030 waits 2 cycles with valid data on the data bus. The NWDD bits in LAS0BRD set the wait delay. This wait delay also satisfies tV WR, the Valid Write Pulse width.

4. On the rising edge of clock cycle 5, the PCI 9030 deasserts the WR signal after a propagation delay of tP LOUT. This causes the SPECTRA-155 to latch the data from the bus. The data must remain present on the bus for an additional tH DW. This is accomplished by setting the Write Cycle Hold bits

in LAS0BRD to 1. The write cycle hold causes DATA, SPECTRA_CS, and ADDR to stay active until the rising edge of cycle 6, when they deassert after tP LOUT.

The output propagation delay involved in Figure 27 are shown in the following table:

Table 27 PCI 9030 to SPECTRA-622 Write Propagation Delays

Name	Device	Description	Min	Max
tP LOUT	PCI 9030	Local Clock edge to Local output delay	-	10

The input constraints involved in Figure 27 are shown in the following table:

Table 28 PCI 9030 to SPECTRA-622 Write Timing Constraints

Name	Device	Description	Min	Actual	Margin
tS AW	SPECTRA-155	Address to valid write set-up	25	40	15
tV WR	SPECTRA-155	Valid write pulse width	40	80	40
tH AW	SPECTRA-155	Address to valid write hold	5	40	35
tS DW	SPECTRA-155	Data to valid write set-up	20	80	60
tH DW	SPECTRA-155	Data to valid write hold	5	40	35

5.2 SIGNAL INTEGRITY SIMULATIONS

5.2.1 Pre-Layout

The following sections contain pre-layout signal integrity simulations for the Telecom, SBI, UTOPIA L2 and PCI 9030 bus interfaces of the S/UNI-IMA-84/TEMUX-84 Development Kit. The simulations were performed using the SPECTRA-155, TEMUX-84, S/UNI-IMA-84 and S/UNI-DUPLEX IBIS models.

5.2.2 Telecom Bus

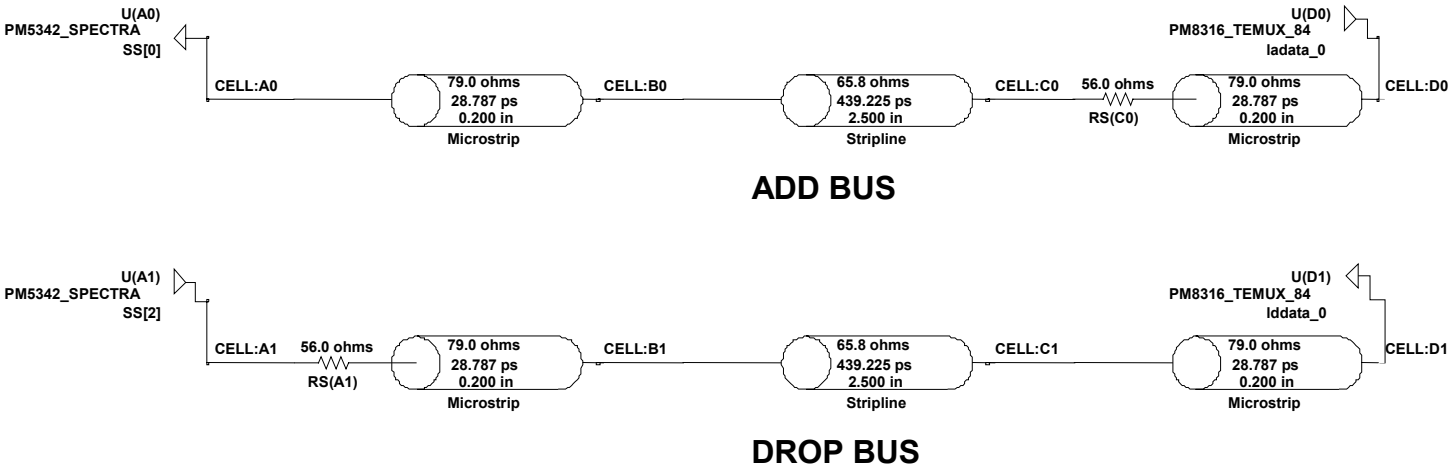

Figure 28 Telecom Bus Simulation Schematic

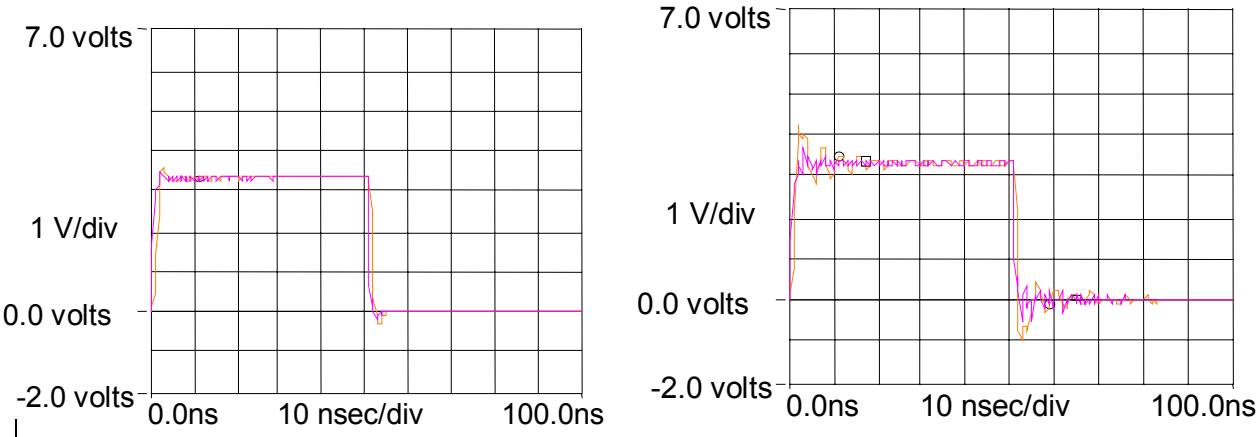

Figure 29 Telecom DROP Bus Simulation Results

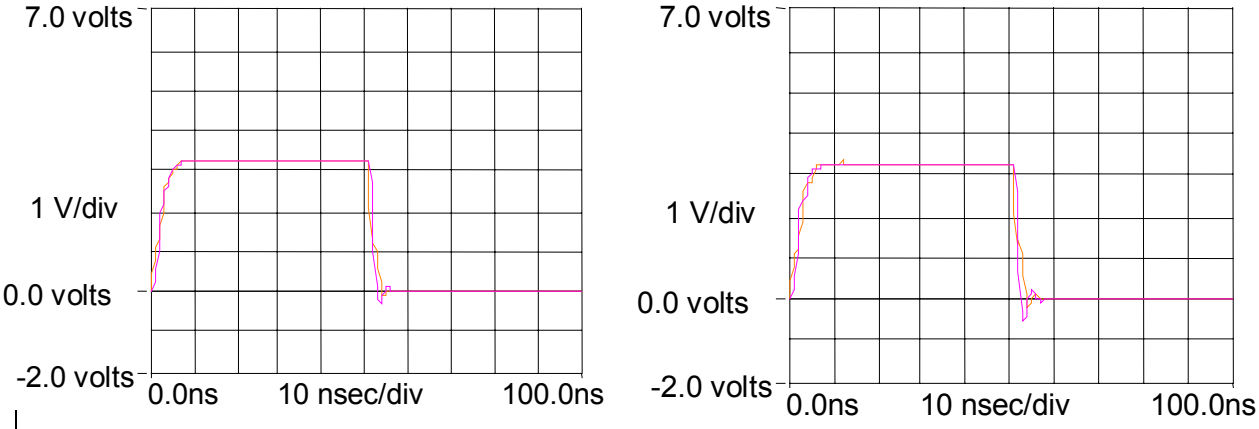

Figure 30 Telecom ADD Bus Simulation Results

Simulation results for 0 Ω and 56 Ω termination values for the ADD and DROP buses are presented in the above figures. It is clear that with 0 Ω terminations (right) more overshoot, undershoot, and ringing occurs than with the 56 Ω terminations.

5.2.3 SBI Bus

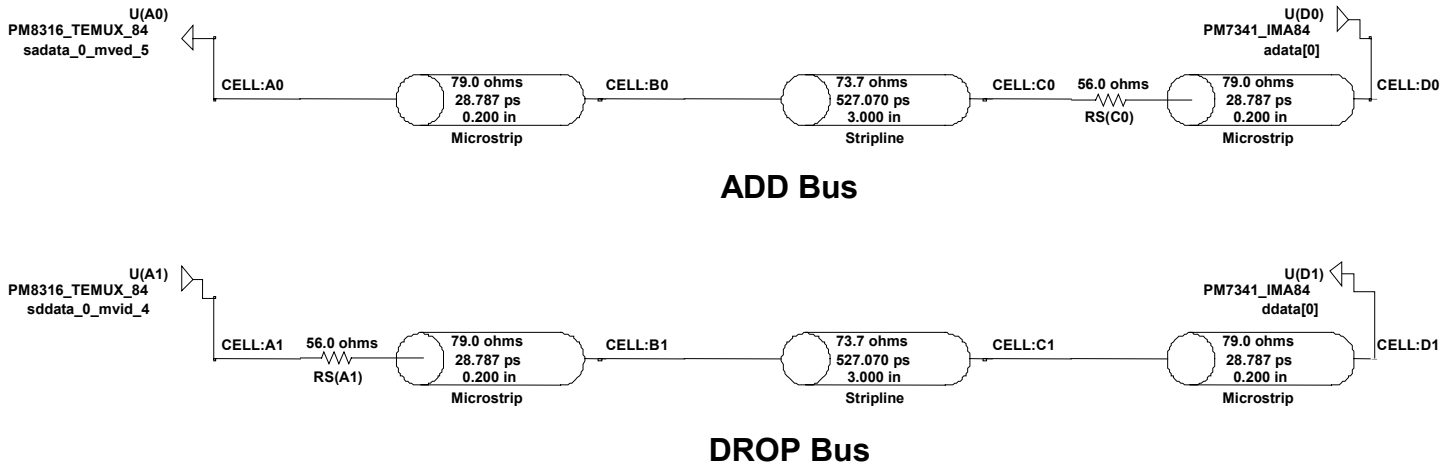

Figure 31 SBI Bus Simulation Schematic

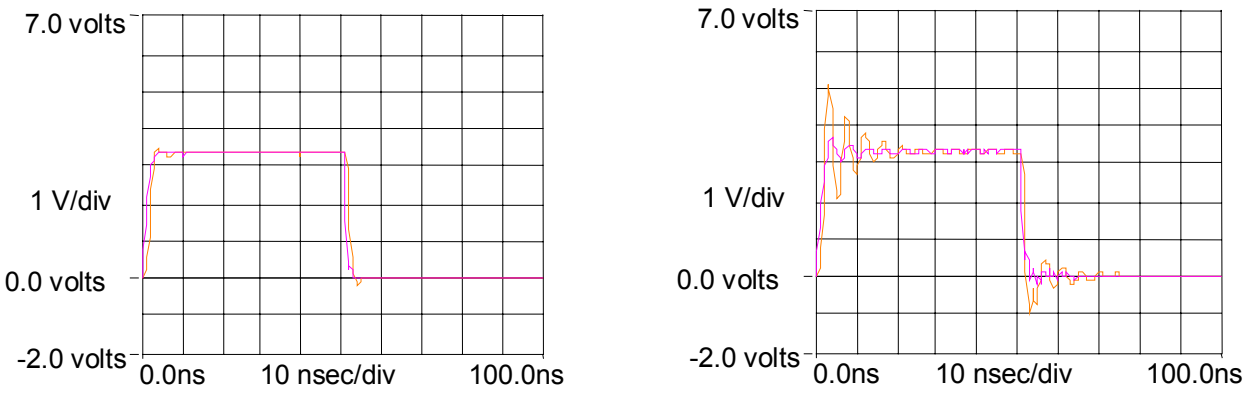

Figure 32 SBI ADD Bus Simulation Results

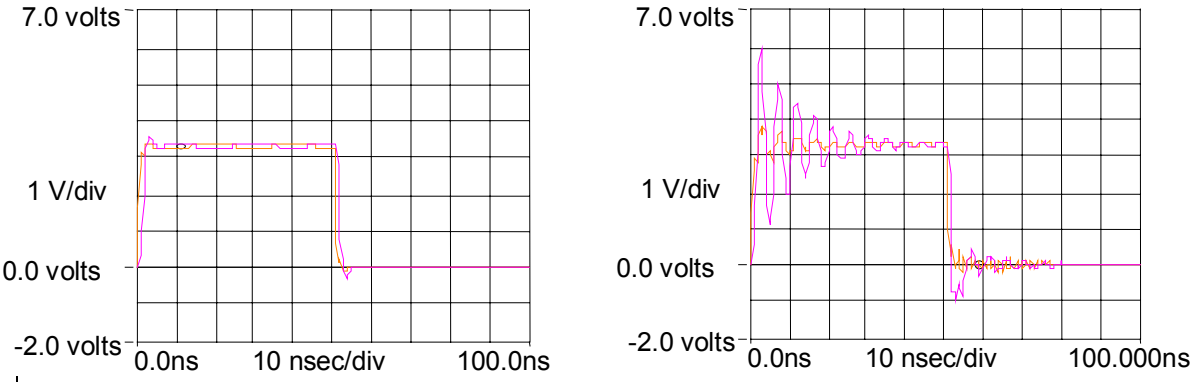

Figure 33 SBI DROP Bus Simulation Results

Simulation results for 0 Ω and 56 Ω termination values for the ADD and DROP buses are presented in the above figures. It is clear that with 0 Ω terminations (right) more overshoot, undershoot, and ringing occurs than with the 56 Ω terminations.

5.2.4 UTOPIA L2 Bus

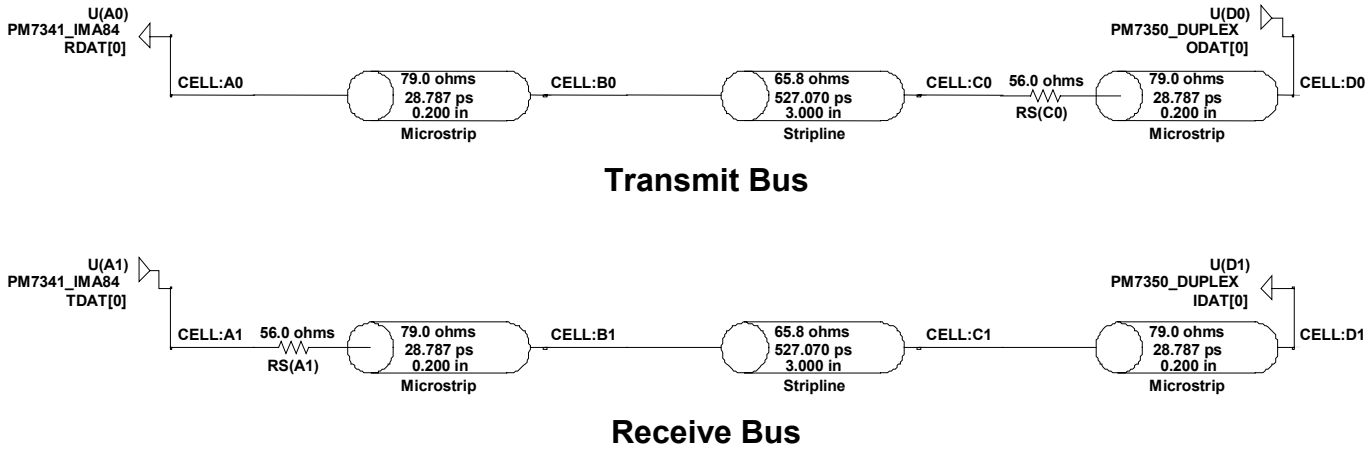

Figure 34 UTOPIA L2 Bus Simulation Schematic

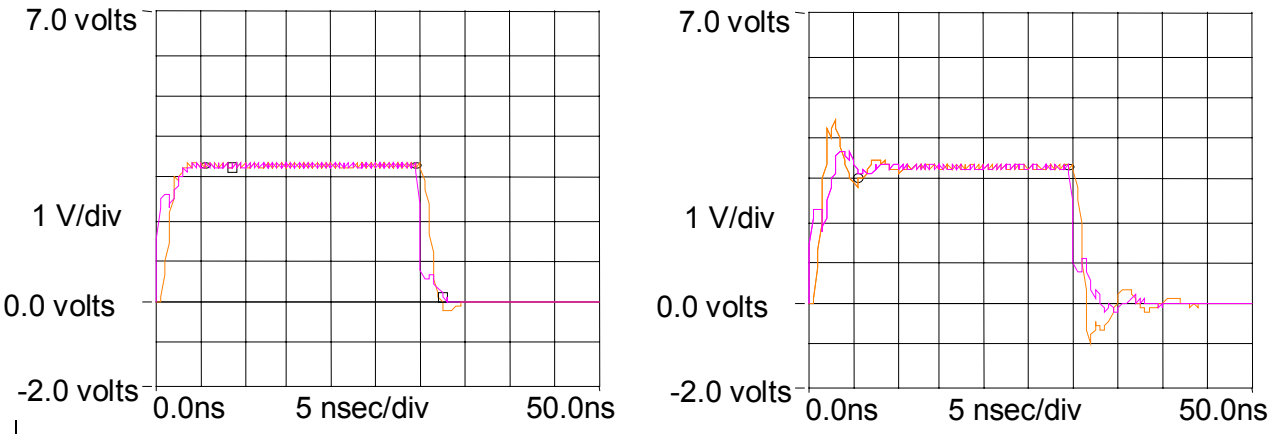

Figure 35 UTOPIA L2 RECEIVE Bus Simulation Results

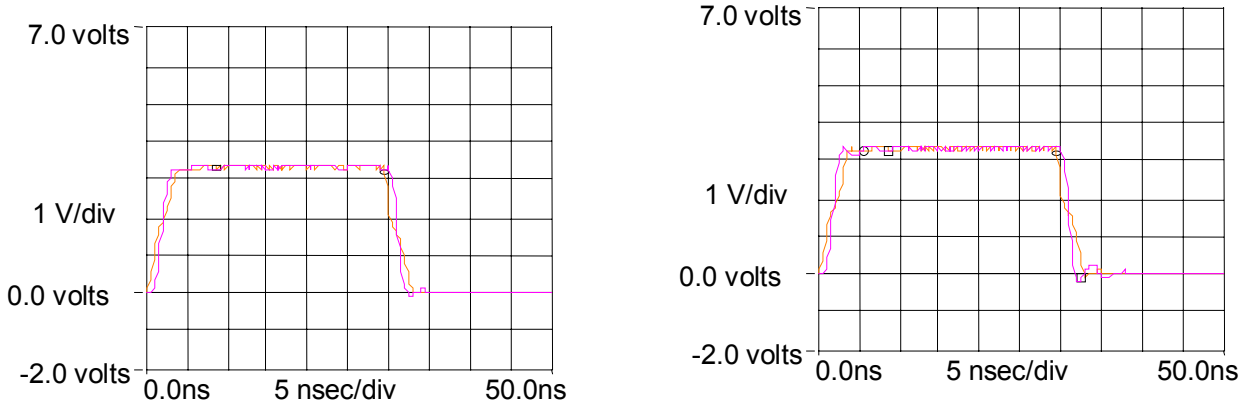

Figure 36 UTOPIA L2 TRANSMIT Bus Simulation Results

Simulation results for 0 Ω and 56 Ω termination values for the RECEIVE and TRANSMIT buses are presented in the above figures. It is clear that with 0 Ω terminations (right) more overshoot, undershoot, and ringing occurs than with the 56 Ω terminations.

5.2.5 PCI 9030 Interface

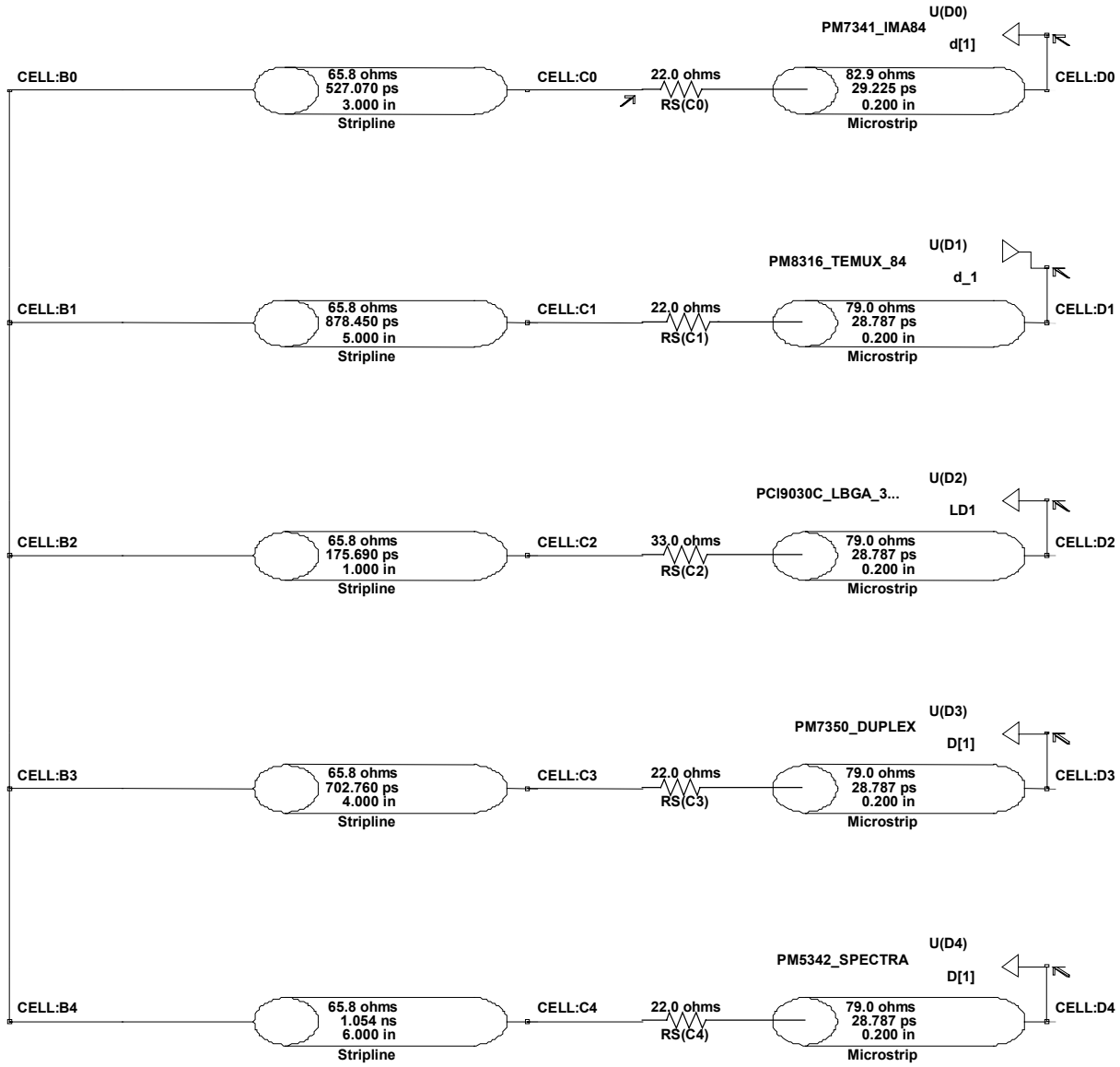

Figure 37 PCI 9030 Simulation Schematic

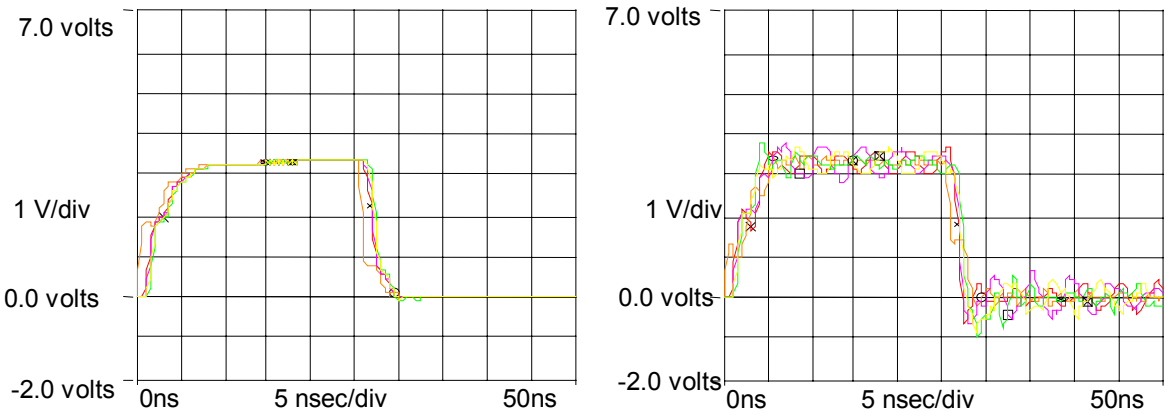

Figure 38 PCI 9030 Simulation Results

Simulation results for no termination (0 Ω) and series termination (22 Ω and 33 Ω) for the PCI 9030 interface are presented in the above figures. It is clear that with no termination (right), more overshoot, undershoot, and ringing occurs than with the termination resistors.

5.3 POWER ESTIMATE AND THERMAL ANALYSIS

Table 29 Power Consumption by Supply Rail for Each Device

	Power (mW)	Current (mA)
1.8V		
S/UNI-IMA-84	929	516
TEMUX-84	1350	750
TOTAL 1.8V	2579	1266
3.3V		
S/UNI-IMA-84	396	120
S/UNI-DUPLEX	1097	333
TEMUX-84	224	68
PCI 9030	495	150
P149FCT3807 x2	792	240
Xilinx XC9536XL	100	33
TOTAL 3.3V	3104	944
5.0V		
SPECTRA-155	725	145
HFCT-5905E	770	154
TOTAL 5.0V	1495	299

The total power requirements for the board are:

TOTAL	**7178mW**	**2509mA**

These numbers are preliminary and may be revised in the future.

6 DESIGN ISSUES

6.1 Power Supply

6.1.1 Decoupling

One 0.01uF and 0.1uF capacitor is required for every two digital power pins. The capacitors should be placed as close to the actual pin as possible.

The analog power supply pins require a filtering network between the GND plane and the +3.3V plane. The network is a single RC network with a resistor between the 3.3V plane and the AVD pin and the capacitor from the AVD pin to the GND plane. Please refer to Appendix A: Bill of Materials for component values.

6.1.2 Power-Up Sequence

The power up sequence must be adhered to, otherwise device latchup can occur. The power supplies must turn on in the following sequence:

1. 5V Power
2. 3.3V Power
3. 1.8V Power

The power down of the card must be performed in the reverse sequence.

The delaying of the 1.8V digital power versus the 3.3V digital power is the critical factor since 1.8V is the core supply voltage for some of the devices and must come up after the 3.3V I/O supply voltage. The delaying of analog supplies to come up after its digital counterpart is easily accomplished by the analog supply filtering components. Since it takes time to charge the filter capacitors, the charging delays the analog supply rail a reasonable amount of time for the digital power to stabilize.

If the simple solution of a filtering network cannot be implemented, then the analog power pins should be current limited to the maximum latch-up current of 100mA.

6.2 SPECTRA-155 Design Considerations

Analog power pins QAVD, RAVD and TAVD must be applied after VDD. A simple solution is to use a small filtering network between the VDD and AVD plane to delay the power to the AVD plane, which will delay power to each AVD pin. The following scheme is implemented on the S/UNI-IMA-84/TEMUX-84 Development Kit:

- Digital supply pins (VDD) are decoupled with 0.1μF capacitors providing high frequency bypassing near the device pins.
- Analog supply pins (TAVD, RAVD, QAVD) are bypassed from the +5V power plane with five separate RC filters consisting of a series resistance and bypass capacitance. Groupings and values are as follows:
    - QAVD1, 2, 3: 4.7Ω series; 10μF, 0.1μF, 0.01μF capacitor to ground
    - RAVD1, 3, 4: 4.7Ω series; 10μF, 0.1μF, 0.01μF capacitor to ground
    - TAVD1, 3: 10Ω series; 10μF, 0.1μF, 0.01μF capacitor to ground
    - RAVD2: 4.7Ω series; 47μF, 0.1μF, 0.01μF capacitor to ground
    - TAVD2: 4.7Ω series; 47μF, 0.1μF, 0.01μF capacitor to ground

6.3 TEMUX-84 Design Considerations

The clock signals XCLK_T1 and XCLK_E1 must be carefully routed from the clock buffers to the TEMUX-84 parts. The lines should be properly terminated and should not run near any of the data busses if possible.

6.4 S/UNI-DUPLEX Design Considerations

The S/UNI-DUPLEX should be placed so that there are no major components and the smallest distance possible between the S/UNI-DUPLEX and the LVDS connectors.

The length of the traces in each of the LVDS line pairs should be kept the same to ensure correct impedance on the transmission line.

6.5 Telecom, SBI, UTOPIA L2 Bus Design Considerations

Each signal on the bus requires adequate termination to prevent reflections. At each point where a bus line connects to a device, a series resistor should be

placed on the line so that the source impedance of the line driver plus the impedance of the series resistor is matched to the characteristic impedance of the line.

6.6 PCI Bridge Design Considerations

During power up, the PCI RST# signal resets the default values of the PCI 9030 internal registers. In return, the PCI 9030 outputs the local reset signal (LRESET#) and checks for the existence of the serial EEPROM. If a serial EEPROM is installed, and the first 16-bit word word is not FFFF, the PCI 9030 initializes the internal registers from the serial EEPROM. Otherwise, default values are used. The PCI 9030 configuration registers can only written by the optional serial EEPROM or the PCI host processor. During the serial EEPROM initialization, the PCI 9030 response to PCI target accesses is RETRYs.

7 LAYOUT DESCRIPTION

7.1 Component Placement

The overall placement strategies of the components are:

- Place the analog circuitry away from the digital circuitry.
- Keep analog transmit side components separate from the analog receive side components.
- For all high-speed data lines, load termination resistors are placed near the receiver inputs.
- For all high-speed data lines, source termination resistors are placed near the driver outputs.
- The Telecom bus, SBI bus should be routed so that the bus length is approximately the same to the TEMUX-84 from the SPECTRA-155 and the S/UNI-IMA-84.
- The PCI Bridge and the CPLD should be placed so that the I/O interface bus can be routed perpendicular to the Telecom/SBI buses.
- All pull up/down resistors are placed near the output pins.
- Oscillators should be placed in quiet digital sections as noise on their power supply will cause jitter on the output, and the oscillators themselves generate noise that may affect sensitive analog circuits.
- The PCI Bridge device is placed such that all the PCI interface traces are within the specified length limits of the PCI Rev. 2.1 Specification.
- All decoupling capacitors are placed near the power supply pins.
- The power supply should be placed in a low-component density area of the board so that sufficient copper on the component layer can be used for heatsinking of the supply regulators.
- Use a single plane for both analog and digital grounds.

The approximate placement of major components is shown in Figure 39 below. (The diagram is drawn to scale.)

6U Euro Card Form Factor

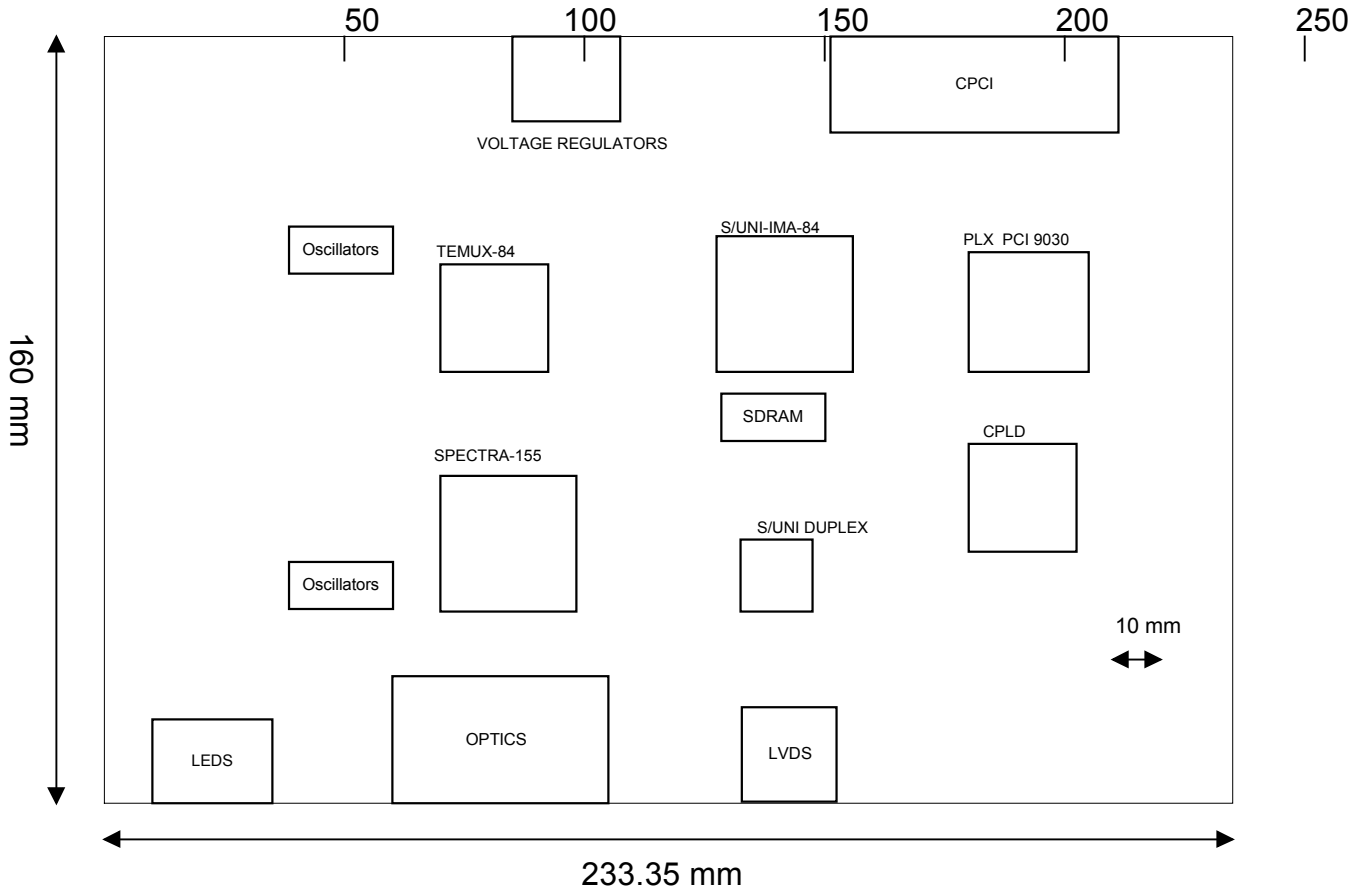

Figure 39 Card Floorplan

7.2 Layer Stacking and Impedance Control

7.3 PCI Bus Signal Specification

This layout follows the PCI Rev. 2.1 Specification layout restrictions. The PCI SIG specification has stringent and detailed rules on decoupling, power consumption, trace length limits, routing, trace impedance, as well as signal loading. Therefore, it is essential to check the latest PCI specification before proceeding with new designs and layouts.

The S/UNI-IMA-84/TEMUX-84 Development Kit design board conforms to the following PCI Specification/Recommendations:

- Component height on the component side does not exceed 0.570 inches, and on the solder side does not exceed 0.105 inches.
- PCI CLK signal trace is 2.5 inches +/- 0.1 inches and is connected to only one load.
- All 32-bit interface signals have the maximum trace length of 1.5 inches.
- Trace impedance for shared PCI signals are within 60 - 100 Ohm range, and trace velocity is between 150 and 190 ps/inch.
- 20 mil wide traces are used to connect the power and ground pins on PCI connector to their respective planes and the trace lengths are limited to 250 mil.

7.4 Routing

- All power and ground traces are as wide and as short as possible to minimize trace inductance.
- All high-speed traces are routed over continuous image planes (power or ground planes).
- All traces carrying transmit and receive line rate data should be routed on the same side and kept as short as possible.
- Both signals of a differential pair should be of equal length and routed close to each other.

8 PHYSICAL AND MECHANICAL DESCRIPTIONS

8.1 Form Factor

The card is based on the CPCI 6U (233.35 mm by 160 mm) board size.

8.2 LEDs

Several LEDs will be used on the front panel to indicate the status of the SONET/SDH links and the status of the card power supply. See below for a description of all status LEDs.

8.2.1 Card Status LEDs

- +5 V, super-red – indicates presence of +5 V
- +3.3 V, super-red – indicates presence of +3.3 V
- +1.8V super-red – indicates presence of +2.5 V
- RESET, super-red – indicates whether a reset condition exists on the board.

8.2.2 SPECTRA-155 LED's

- SALM (Section Alarm), red – Asserted when OOF, LOS, LOF, LAIS, or LRDI alarm conditions exist.
- LOF (Loss of Frame), red – Asserted when a Loss of Frame persists for more than 3 ms.
- LOS (Loss of Signal), red – Asserted when a violating period (20 $\pm$ 2.5 μs) of consecutive all zeros pattern is detected in the incoming stream.
- LAIS (Line Alarm Indication), red – Asserted when an AIS (Alarm Indication Signal) is detected in the incoming stream (111 pattern in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames).
- LRDI (Line Remote Defect Indication), red – Asserted when line RDI (Remote Defect Indication) is detected in the incoming stream (110 pattern in bits 6, 7 and 8 of the K2 byte for three or five consecutive frames).

- RALM <3..1> (Receive Alarm), red – Asserted when the following alarm conditions exist in the incoming stream: LOP (Loss of Pointer), PAIS (Path Alarm Indication), PRDI (Path RDI), PERDI (Path Enhanced RD), LOM (Loss of Multiframe), LOPCON (Loss of Pointer Concatenation), or PAISCON (Path AIS Concatenation).

9 SOFTWARE INTERFACE

9.1 System Processor Requirement

The S/UNI-IMA-84/TEMUX-84 Development Kit must be accompanied with a CPU processor card on the same CPCI shelf.

9.2 S/UNI-IMA-84/TEMUX-84 Development Kit Operating System

The S/UNI-IMA-84/TEMUX-84 Development Kit supports the VxWorks real time operating system (RTOS). The device drivers for the Development Kit's chipsets are pre-ported for VxWorks.

9.3 Device Drivers

Upon request, PMC-Sierra Inc. provides drivers for each PMC-Sierra chip mounted on the Development Board.

9.4 S/UNI-IMA-84/TEMUX-84 Development Kit Memory Map

Table 30 lists the memory map for the S/UNI-IMA-84/TEMUX-84 Development Kit.

Table 30 S/UNI-IMA-84/TEMUX-84 Development Kit Memory Map

PCI 9030 CHIP SELECT	ADDRESS RANGE	DEVICE	CHIP SELECT
CS0	0x00000 – 0x40000	SPECTRA-155	SPECTRA_CS
CS1	0x40000 – 0x80000	TEMUX-84	TEMUX_CS
CS2	0x80000 - 0xC0000	S/UNI-IMA-84	IMA_CS
CS3	0xC0000 - 0x100000	S/UNI-DUPLEX	DUPLEX_CS

Within this development kit, there is a local bus on which one 16-bit device (S/UNI-IMA-84), and three 8-bit devices (SPECTRA-155, TEMUX-84, S/UNI-DUPLEX) reside. Dealing with this constraint allowed for two possibilities. One would have been to use the 9030's ability to dynamically interface a 32-bit PCI bus to 8- and 16-bit local busses. While this option would have maximized memory efficiency on the CPU side, it also would have increased the design's complexity, both in hardware and in software.

The option that was chosen for this reference design was to treat all devices as if they were 32 bit devices. All devices are assigned a 32-bit address space by the

CPU. In the case of the 8-bit devices, 24 bits of every CPU lword are ignored. For the 16-bit device, 16 bits of the CPU lwords are ignored. The disadvantage of this design choice is that more CPU memory is required. However, because the S/UNI-IMA-84/TEMUX-84 Development kit does not require a large amount of memory space, this design choice is acceptable, considering the reduction in complexity it offers.

Address translation works as follows: For a 16-bit local bus, the 9030 expects all addresses to be lword (32-bit) aligned, causing all addresses to end with ‘00’. Because of this, the 9030 does not even provide the two lowest address bits on the Local address bus. To accommodate this, every local address is mapped to an lword aligned boundary on the CPU side. i.e. register 0x0011 on the S/UNI-DUPLEX is addressed as 0x0044on the CPU side.

10 BOARD MODIFICATIONS

10.1 Signal Detect on HFCT 5905

The signal detect symbol on the HFCT 5905 part was pulled high externally to 3.7 V using a voltage divider and the +5V power source. This was necessary because the HFCT 5905 is a +3.3V part whereas the SPECTRA-155 is +5V part. It is recommended that a +5V optics module such as the HFCT 5205 be used instead of the HFCT 5905. The HFCT 5205 is implemented in the updated schematics.

10.2 UTOPIA L2 Bus

On the S/UNI-IMA-84, the UTOPIA L2 Bus is connected to TADR_SCAN<0..4>, not TADR<7..10>. This change is reflected is the updated schematics.

10.3 SCANENB pin on S/UNI-IMA-84

The SCANENB pin on the S/UNI-IMA-84 should be pulled high externally via 4.7kΩ pull-up resistor, not pulled low externally. This change is reflected in the updated schematics.

11 GLOSSARY

T1	A level 1 digital trunk operating at 1.544 Mbit/s that is popular in North America and Japan. It is made up of 193 bits, grouped as 1 framing bit followed by 24 DS-0 channels of 8 bits each.
E1	European First Order transmission format. This is the standardized (ITU-T G.704) base format of the European Pleisosynchronous Digital Hierarchy. It operates at 2.048Mbps. The E1 format consists of frames consisting of 32 octets, or timeslots (numbered 0 to 31). Timeslot 0 alternates between containing an FAS and containing the National Use bits (Sa[8:4]) and an A-bit for RAI. Timeslot 0 also contains an International Use Bit (Si) which can be used to support CRC Multiframe.
SPE	Synchronous Payload Envelope
PCI	Peripheral Component Interconnect – A bus standard that defines 32 bit transfers over a defined electrical interface.
PCI Host	An adapter board for a PCI system which acts as a PCI Master and performs the additional functions of clock distribution and bus arbitration.
PCI Target	An adapter board for a PCI system which does not initiate bus transactions. Also known as a slave.
CompactPCI	Compact Peripheral Component Interconnect. A bus standard based on the PCI standard that defines a more rugged mechanical form factor for industrial use.
SEEP	Serial EEPROM (Electrically Erasable Programmable Read Only Memory) – A type of non-volatile memory which is programmed and read using a serial interface.

12 REFERENCES

1. PMC-Sierra Inc., PMC-1970133, “SPECTRA-155 SONET/SDH Payload Extractor/Aligner”, August 1998, Issue 4.

2. PMC-Sierra Inc., PMC-1991437, “TEMUX-84 High Density 81 T1/63 E1 Framer with Integrated VT/TU Mappers and M13 Multiplexers”, October 2000, Issue3.

3. PMC-Sierra Inc., PMC-2000223, ”S/UNI-IMA-84 S/UNI Inverse Multiplexing for ATM, 84 Links”, April 2000, Issue 2.

4. PMC Sierra Inc., PMC-1980581, “S/UNI-DUPLEX Dual Serial Link Phy Multiplexer Data Sheet”, April 2000, Issue 5.

5. PCI Technology, PCI 9030-1 Data Book, Version 1.0, April 2000.

6. PCI Industrial Computer Manufacturers, CompactPCI PICMG, Revision 2.0, September 2, 1997.

13 APPENDIX A: BILL OF MATERIALS

Item	Description	Part Number	Manufacturer	Reference Designator	Quantity
1	SURFACE MOUNT SWITCHING DIODE	1N4148W	VISHAY/LITE-ON	D5	1
2	IC 3.3V 1:10 CMOS CLOCK DRIVER SOIC20W	PI49FCT3807AS	PERICOM	U6	1
3	OCTAL BUFFER LINE DRIVER WITH 3 STATE OUTPUT, SOIC20W	SN74HC540	TEXAS INSTRUMENTS	U2	1
4	IC QUAD 2 IN AND GATE SOIC14	MM74HC08M	FAIRCHILD SEMI	U8	1
5	CAP 1.01UF 50V CERAMIC 0603 SMD	DIGIKEY PCC103BVCT-ND	DIGI-KEY	C321, C329, C344	3
6	MULTILAYER CERAMIC CHIP CAPACITOR X7R 0603 0.1UF 16V	PANASONIC -- ECJ-1VB1C104K	PANASONIC	C323, C326	2
7	CAPR TANT 22UF EIA SIZE B	PANASONIC	PANASONIC	C1, C2	2
8	CAP CERAMIC X7R 0603 50V 0.01UF	ECU-V1H103KBV	PANASONIC	C12-C16, C27, C29, C30, C70, C77, C80, C82-C85, C87, C90, C91, C93, C95, C96, C98, C100-C108, C113, C114, C116-C128, C131-C136, C138, C139, C145, C146, C149, C151, C153, C154, C156, C158-C160, C165, C166, C169, C171, C172, C177, C179-C181, C183, C184, C188, C190-C192, C194, C200-C202	83
9	CAP CERAMIC X7R 0603 25V 0.022UF	ECJ-1VB1E223K	PANASONIC	C53	1
10	CAP CERAMIC X7R 0850 50V 0.047UF	08055C473JATN	AVX	C55	1
11	CAP CERAMIC X7R 0603 16V 0.1UF	ECJ-1VB1C104K	PANASONIC	C3, C28, C35, C36, C39-C41, C49, C50, C52, C71-C76, C78, C79, C81, C86, C88, C89, C92, C94, C97, C99, C109-C112, C115, C129, C130, C137, C140-C144, C147, C148, C150, C152, C155, C157, C161-C164, C167, C168, C170, C173-C176, C178, C182, C185-C187, C189, C193, C195-C199,	75

				C203-C209	
12	CAP CERAMIC X7R 0603 10V 0.22UF	ECJ-1VB1A224K	PANASONIC	C62-C69	8
13	CAP CERAMIC X7R 1206 16V 0.33UF	ECJ-3VB1C334K	PANASONIC	C54	1
14	CAP CERAMIC NPO 0805 50V 1000PF	ECU-V1H102JCX	PANASONIC	C19	1
15	CAP ELECTRO VA SMD 10V 20% 1000UF	ECE-V1AA102P	PANASONIC	C43, C59	2
16	CAP TANCAPC 10V 20% 10UF	ECS-H1AC106R	PANASONIC	C4	1
17	CAP TANCAPA 6.3V 20% 10UF	ECS-T0JY106R	PANASONIC	C9-C11, C17, C18	5
18	CAP TANCAPA 16V 20% 1UF	ECS-H1CY105R	PANASONIC	C24, C44, C60	3
19	CAP TANCAPD 10V 20% 33UF	ECS-H1AD336R	PANASONIC	C20-C23, C25, C26, C31-C34, C37, C38, C42, C45-C47, C56-C58	19
20	CAP TANCAPA 6.3V 20% 4.7UF	ECS-T0JY475R	PANASONIC	C48, C51	2
21	CAP TANCAPD 6.3V 20% 47UF	ECS-H0JD476R	PANASONIC	C7, C8	2
22	CONNECTOR 38 POS VERTICAL .025" TO .64" SMD MICTOR	2-767004-2	AMP	J10-J12	3
23	PART OF PCB COMPACT PCI ESD STRIP	PART OF PCB	PART OF PCB	P1	1
24	TRANSFORMER, DUAL, 10/100BASE-TX	H1026	PULSE ENGINEERING	T1	1
25	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	PZC36SAAN	SULLINS ELECTRONICS	J13	1
26	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	PZC36SAAN	SULLINS ELECTRONICS	J7	1
27	CONN HEADER 8 PIN	PZC36SAAN	SULLINS	J3, J4, J9	3
28	PITCH HEADER - STRAIGHT SQUARE 3 ROW 1 POSITION/ROW	53047-0310	MOLEX	J5	1
29	TEMPERATURE 0C TO 70C	HFCT-5205BD	HEWLETT PACKARD	U21	1
30	0.007 OHM, 20 V, HEXFET POWER MOSFET	IRL3502S	INTERNATIONAL RECTIFIER	Q1, Q2	2
31	T-1 3/4 LED BLUE VERTICAL PCB MOUNT STATIC SENSITIVE	PANASONIC LNG91LCFB	PANASONIC	D4	1

32	3A FAST ULTRA LOW DROPOUT LINEAR REGULATOR 1.8V TO263-5	LP3966ES-1.8	NATIONAL SEMI	U13	1
33	4.6A LOW DROPOUT FIXED 3.3V REGULATOR	LT1585CT-3.3	LINEAR TECHNOLOGY	U16	1
34	HOT SWAP CONTROLLER	LTC1422CS8	LINEAR TECHNOLOGY	U15	1
35	GENERAL PURPOSE TRANSISTOR	MMBT3904LT1	MOTOROLA	Q3	1
36	2MM IEEE 1394-1995 SHIELD RIGHT ANGLE	53460-0611	MOLEX	J1, J2	2
37	MOUNTING HOLE .150" DIA	MOUNTING HOLE	N/A	M1	1
38	3.3V, 100MHZ, 8MB SDRAM (1MBIT X 4BANKS X 16WIDE)	MT48LC4M16A2-75	MICRON	U11	1
39	2048 BIT SERIAL EEPROM W/ DATA PROTECT AND SEQ READ DIP8	NM93CS56LEN	FAIRCHILD SEMI	U9	1
40	OSCILLATOR, 25MHZ, 3.3V, 50PPM	CB3LV-3C-25.0000- T	CTS REEVES	Y2	1
41	OSCILLATOR 19.440MHZ 3.3V [TOL= 20PPM] [TEMP= 0-70C] [DUTY= 10%]	EH2645TS-19.440M	ECLIPTEK	Y1	1
42	OSCILLATOR 55.000MHZ 3.3V [TOL= 50PPM] [TEMP= 0-70C] [DUTY= 10%]	EH2645TS-55.000M	ECLIPTEK	Y6	1
43	OSCILLATOR 37.056MHZ 3.3V, 32PPM	EP2632TTS-37.056M	ECLIPTEK	Y5	1
44	OSCILLATOR 49.152MHZ 3.3, 32PPM	EP2632TTS-49.152M	ECLIPTEK	Y4	1
45	OSCILLATOR, 51.84MHZ, 3.3V, 50PPM	EP2645TTS-51.840M	ECLIPTEK	Y3	1
46	RIGHT ANGLE PCB MOUNT SPST PUSH BUTTOM	DIGIKEY -- CKN4002-ND	DIGI-KEY	SW1	1
47	IC 3.3V PCI INTERFACE(180 PIN UBGA PACKAGE)	PCI9030-AA60BI	PLX TECHNOLOGY	U12	1
48	POWER BLOCK			P2, P3	2
49	RES 0603 1/16W 5% ZERO OHM	ERJ-3GSY0R00V	PANASONIC	R200, R201	2
50	RES 2512 1W 1% 0.01	WSL2512-R01-1	VISHAY	R107, R112	2

	OHM				
51	RES 0603 1/16W 5% 1.0K OHM	ERJ-3GSYJ102V	PANASONIC	R7, R124	2
52	RES 0603 1/16W 5% 1.2K OHM	ERJ-3GSYJ122V	PANASONIC	R199	1
53	RES 0603 1/16W 5% 10 OHM	ERJ-3GSYJ100V	PANASONIC	R5, R19, R119, R125, R195	5
54	RES 0603 1/16W 5% 100 OHM	ERJ-3GSYJ101V	PANASONIC	R8, R16	2
55	RES 0603 1/16W 5% 100K OHM	ERJ-3GSYJ104V	PANASONIC	R198	1
56	RES 0603 1/16W 5% 10K OHM	ERJ-3GSYJ103V	PANASONIC	R105	1
57	RES 0805 1/10W 5% 10M OHM	ERJ-6GEYJ106V	PANASONIC	R31, R37, R83	3
58	RES 0603 1/16W 5% 130 OHM	ERJ-3GSYJ131V	PANASONIC	R2, R3	2
59	RES 0603 1/16W 1% 2.43K OHM	ERJ-3EKF2431V	PANASONIC	R122	1
60	RES 0603 1/16W 5% 22 OHM	ERJ-3GSYJ220V	PANASONIC	R78, R155, R158, R169, R170	5
61	RES 0603 1/16W 1% 237 OHM	ERJ-3EKF2370V	PANASONIC	R14, R15	2
62	RES 0603 1/16W 5% 270 OHM	ERJ-3GSYJ271V	PANASONIC	R4	1
63	RES 0603 1/16W 5% 3.0K OHM	ERJ-3GSYJ302V	PANASONIC	R6	1
64	RES 0603 1/16W 5% 330 OHM	ERJ-3GSYJ331V	PANASONIC	R20, R32, R33, R35, R36, R38-R40, R51, R53, R56, R58, R61, R62, R66, R69-R73, R77, R91, R145-R147, R154, R156, R159, R162, R163, R174, R175, R178, R180-R183, R185, R187-R193, R202, R203	47
65	RES 0603 1/16W 5% 4.7 OHM	ERJ-3GSYJ4R7V	PANASONIC	R17, R18, R29, R30, R34	5
66	RES 0603 1/16W 1% 4.75K OHM	ERJ-3EKF4751V	PANASONIC	R148	1
67	RES 0603 1/16W 5% 4.7K OHM	ERJ-3GSYJ472V	PANASONIC	R1, R49, R50, R60, R63-R65, R68, R74, R81, R84, R88, R89, R93, R96, R98, R104, R106, R108-R111, R113-R118, R120, R126, R127, R149, R150, R152, R153, R157, R160, R161, R164, R166, R171-R173, R197, R204	45
68	RES 0603 1/16W 1% 47.5 OHM	ERJ-3EKF47R5V	PANASONIC	R196	1
69	RES 0603 1/16W 1%	ERJ-3EKF49R9V	PANASONIC	R21-R24	4

	49.9 OHM				
70	RES 0603 1/16W 5% 56 OHM	ERJ-3GSYJ560V	PANASONIC	R9, R10, R13, R25-R28, R41-R48, R52, R54, R55, R57, R59, R67, R75, R76, R79, R80, R82, R85-R87, R90, R92, R94, R95, R97, R99-R103, R151, R165, R167, R168, R176, R179, R186, R194	47
71	RES 0603 1/16W 1% 6.81K OHM	ERJ-3EKF6811V	PANASONIC	R123	1
72	RES 1.00M OHM 1/16W 1% 0603 SMD	DIGI-KEY -- P<VALUE>MHCT-ND	PANASONIC	R130-R137	8
73	RES 1.0M OHM 1/10W 5% 0805 SMD	DIGI-KEY -- P<VALUE>ACT-ND	PANASONIC	R121	1
74	RES 2.7 OHM 5% 0603	DIGI-KEY -- P<VALUE>ACT-ND	DIGI-KEY	R11, R12	2
75	RES 237 OHM 5% 0603	DIGI-KEY -- P<VALUE>GCT-ND	DIGI-KEY	R177	1
76	RES 330 OHM 5% 0603	DIGI-KEY -- P<VALUE>GCT-ND	DIGI-KEY	R129, R138, R140	3
77	RES 430 OHM 5% 0603	DIGI-KEY -- P<VALUE>GCT-ND	DIGI-KEY	R141, R143	2
78	RES 49.9 OHM 5% 0603	DIGI-KEY -- P<VALUE>GCT-ND	DIGI-KEY	R128, R139	2
79	RES 681 OHM 5% 0603	DIGI-KEY -- P<VALUE>GCT-ND	DIGI-KEY	R184	1
80	RES 750 OHM 1/16W 5% 0603 SMD	DIGI-KEY -- P<VALUE>GCT-ND	PANASONIC	R142, R144	2
81	RES ARRAY 10 OHM 5% 4 RES SMD	PANASONIC -- EXB-V8V100JV	PANASONIC	RN89-RN95, RN130-RN13 5	13
82	RES ARRAY 22 OHM 5% 4 RES SMD	DIGI-KEY -- Y4<VALUE CODE>-ND	PANASONIC	RN5-RN10, RN12, RN14, RN25-RN30, RN35-RN37, RN45, RN49, RN63-RN67	24
83	RES ARRAY 33 OHM 5% 4 RES SMD	PANASONIC -- EXB-V8V330JV	PANASONIC	RN71-RN77, RN83	8
84	RES ARRAY 330 OHM 5% 4 RES SMD	DIGI-KEY -- Y4<VALUE CODE>-ND	PANASONIC	RN21-RN24, RN31-RN34, RN40, RN43, RN46, RN48, RN50, RN51, RN53, RN54, RN56-RN62, RN68-RN70, RN78, RN79, RN96-RN103 , RN105,	50

				RN106, RN108-RN11 5, RN122-RN12 5	
85	RES ARRAY 4.7K OHM 5% 4 RES SMD	PANASONIC -- EXB-V8V472JV	PANASONIC	RN19, RN20, RN55, RN82, RN84-RN88, RN116-RN12 1, RN126-RN12 9	19
86	RES ARRAY 470 OHM 5% 4 RES SMD	DIGI-KEY -- Y4<VALUE CODE>-ND	PANASONIC	RN1, RN2	2
87	RES ARRAY 56 OHM 5% 4 RES SMD	PANASONIC -- EXB-V8V560JV	PANASONIC	RN3, RN4, RN11, RN13, RN15-RN18, RN38, RN39, RN41, RN42, RN44, RN47, RN52, RN80, RN81, RN104, RN107	19
88	SMB VERTICAL GOLD	903-499J-51P2	AMPHENOL	J6, J8	2
89	IC PMC SPECTRA-155	PM5342-BI	PMC SIERRA	U4	1
90	LED QUAD RED HORIZONTAL	SSF-LXH5147LID	LUMEX	D1, D2	2
91	LED QUAD SUPER RED HORIZONTAL	SSF-LXH5147SRD	LUMEX	D3	1
92	S/UNI-DUPLEX SCIPHY MODE	PM7350-PI	PMC-SIERRA	U5	1
93	IC S/UNI INVERSE MULTIPLEXING FOR ATM 84 LINKS	PM7341	PMC SIERRA	U7	1
94	IC HIGHSPEED CMOS QUAD 2 INPUT AND GATE SO14NB	TC74LVX08FN	TOSHIBA	U14	1
95	IC HIGH DENSITY T1/E1 FRAMER WITH INTEGRATED VT/TU MAPPER AND M13 MUX	PM8316	PMC SIERRA	U10	1
96	IC IN SYSTEM PROGRAMMABLE CPLD PLCC44	XC9536XL-7PC44C	XILINX	U3	1
97	CONNECTOR ZPACK CPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD	352068-1	AMP	J15	1

14 APPENDIX B: SCHEMATICS

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

DRAWING:
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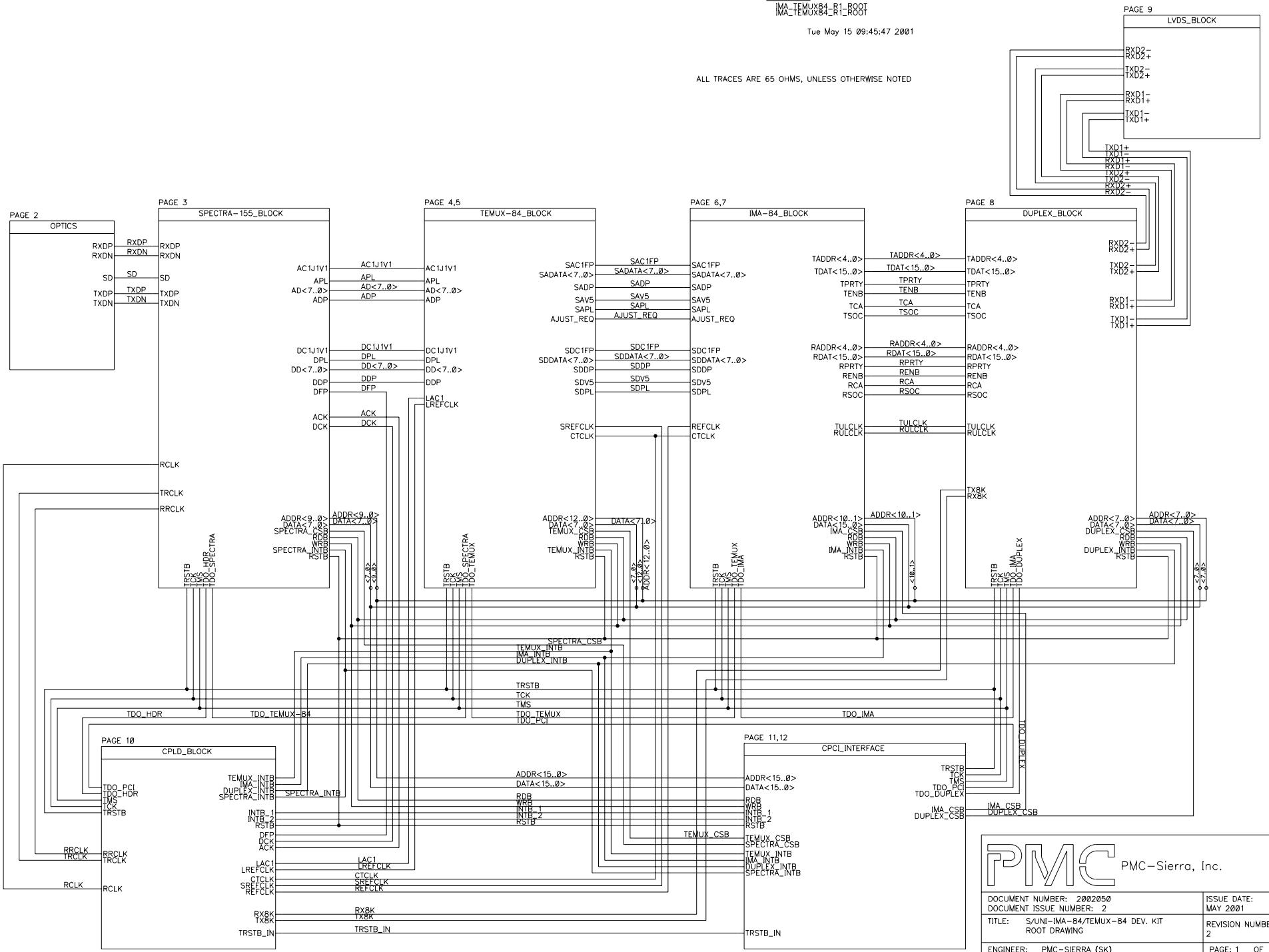
IMA_TEMUX84_R1_ROOT

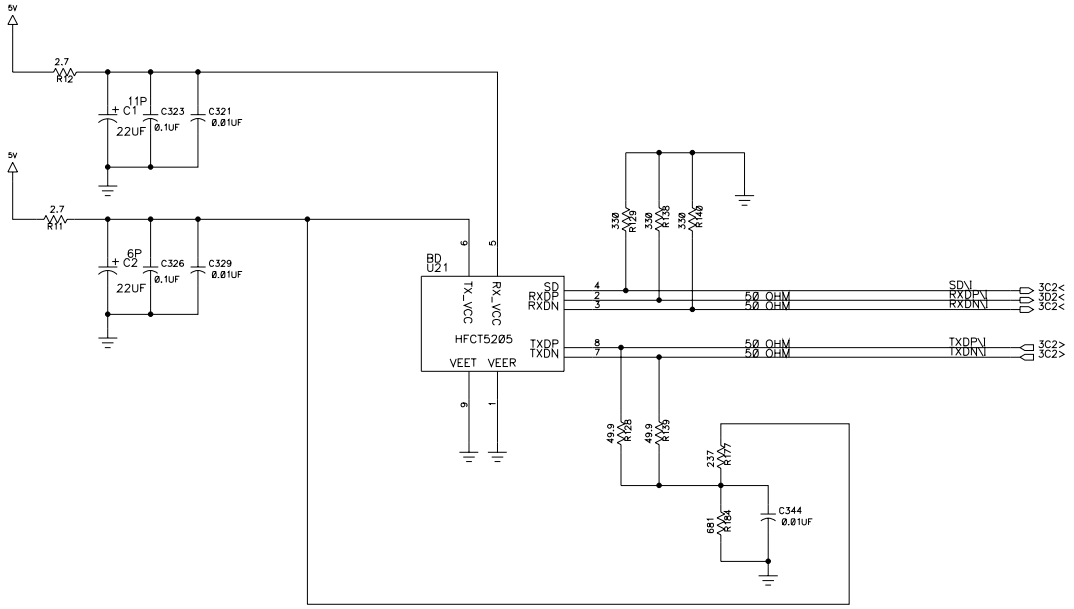
Tue May 15 09:45:47 2001

ALL TRACES ARE 65 OHMS, UNLESS OTHERWISE NOTED



PMC-Sierra, Inc.	
DOCUMENT NUMBER: 2002050 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT ROOT DRAWING	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)	PAGE: 1 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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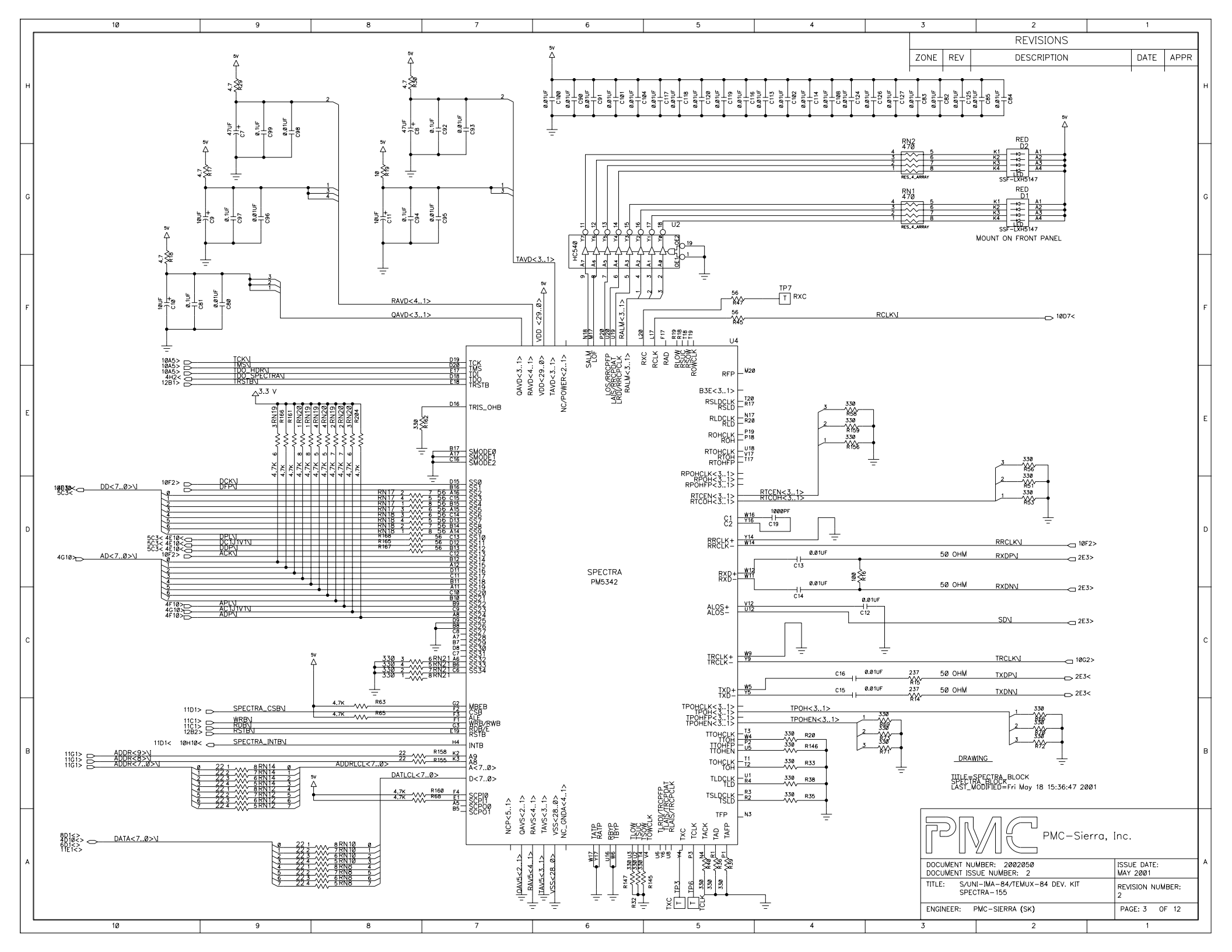
LAST_MODIFIED=Fri May 18 15:36:01 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: 2002050 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT OPTICS BLOCK	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)	PAGE: 2 OF 12


REVISIONS
ZONE | REV | DESCRIPTION | DATE | APPR
SPECTRA
PM5342
U4
U2
HC540
RN2
470
RN1
470
RED
D2
RED
D1
SSF-LXH5147
MOUNT ON FRONT PANEL
TP7
RXC
RCLK\
10D7<
TAVD<3..1>
RAVD<4..1>
QAVD<3..1>
VDD <29..0>
SPECTRA_CSB\
WRB\
RDB\
RSTB\
SPECTRA_INTB\
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ADDR<8>\
ADDR<7..0>\
ADDRLCL<7..0>
DATLCL<7..0>
DATA<7..0>\
TRIS_OHB
SMODE0
SMODE1
SMODE2
DCK\
DFP\
DPL\
DC1J1V1\
DDP\
ACK\
APL\
AC1J1V1\
ADP\
RRCLK+
RRCLK–
RXD+
RXD–
ALOS+
ALOS–
TRCLK+
TRCLK–
TXD+
TXD–
TPOHCLK<3..1>
TPOH<3..1>
TPOHF<3..1>
TPOHEN<3..1>
TTOHCLK
TTOH
TTOHFP
TTOHEN
TOHCLK
TOH
TLDCLK
TLD
TSLDCLK
TSLD
TFP
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RTCEN<3..1>
RTCOH<3..1>
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B3E<3..1>
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RSLD
RLDCLK
RLD
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RTOHCLK
RTOH
RTOHFP
RXC
RCLK
RAD
RLOW
RSOC
RSOW
ROWCLK
RALM<3..1>
SALM
LOF
LOS/TRCPFP
LOP/TRCPCLK
LRAIS/TRCPDAT
RLAIS/TRCPCLK
TLRDI/TRCPFP
TLAIS/TRCPDAT
TLAIS/TRCPCLK
TXC
TCLK
TACK
TAD
TAFP
TATP
TATPI
TBYP
TLOW
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SS2
SS3
SS4
SS5
SS6
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SS13
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SS21
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SS23
SS24
SS25
SS26
SS27
SS28
SS29
SS30
SS31
SS32
SS33
SS34
MBEB
CSB
ALE
WRB/RWB
RDB/E
RSTB
INTB
A9
A8
A<7..0>
D<7..0>
SCPI0
SCPI1
SCPO0
SCPO1
TCK
TMS
TDI
TDO
TRSTB
TCK\
TMS\
TDO_HDR\
TDO_SPECTRA\
TRSTB\
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RXDP\
RXDN\
SD\
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LAST_MODIFIED=Fri May 18 15:36:47 2001
PMC-Sierra, Inc.
DOCUMENT NUMBER: 2002050
DOCUMENT ISSUE NUMBER: 2
ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT SPECTRA-155
REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)
PAGE: 3 OF 12

REVISIONS				
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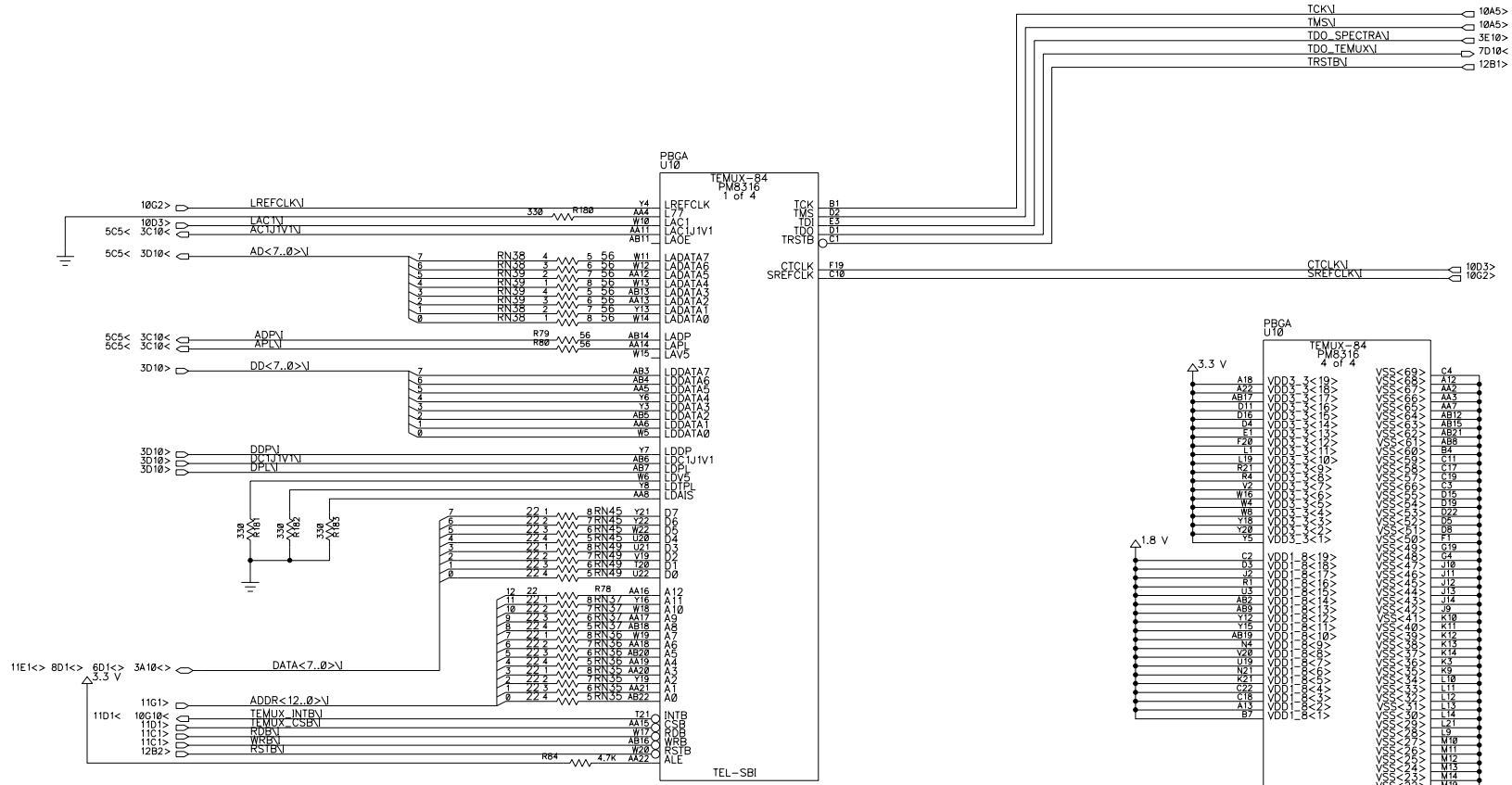

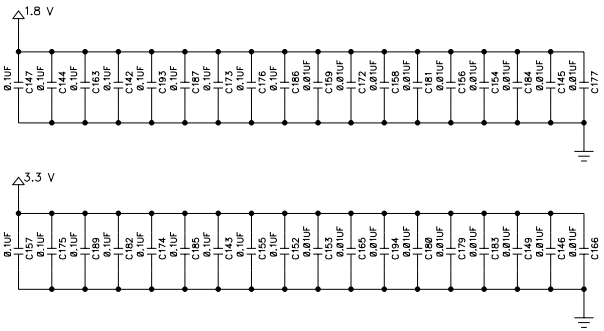

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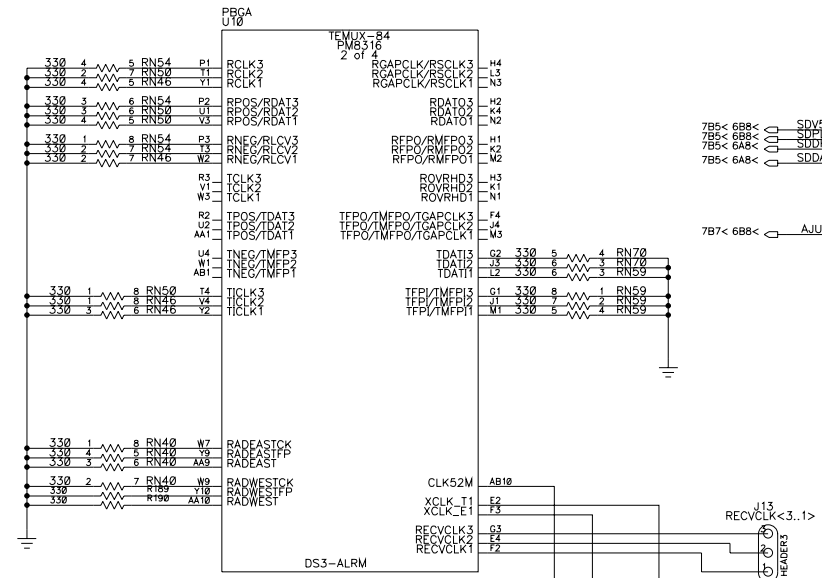
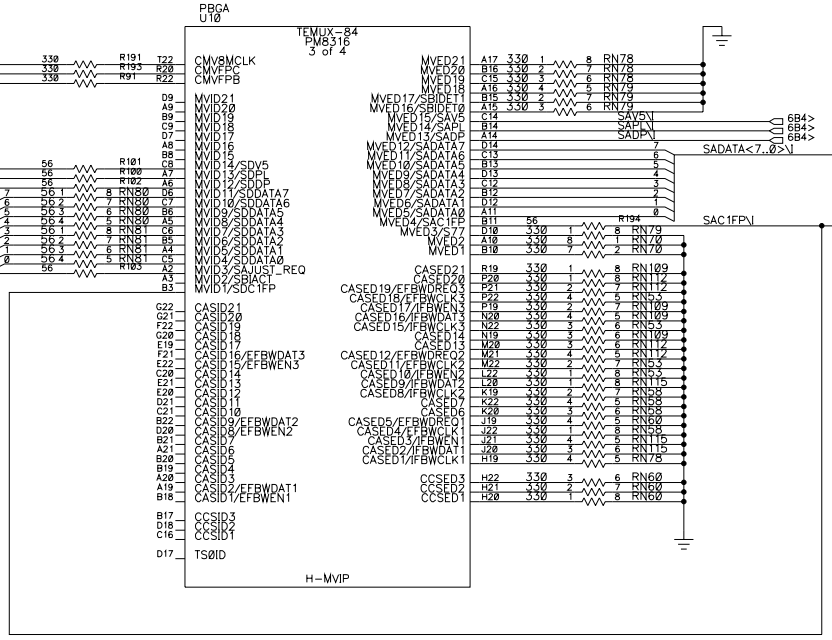
Fri May 18 15:36:33 2001

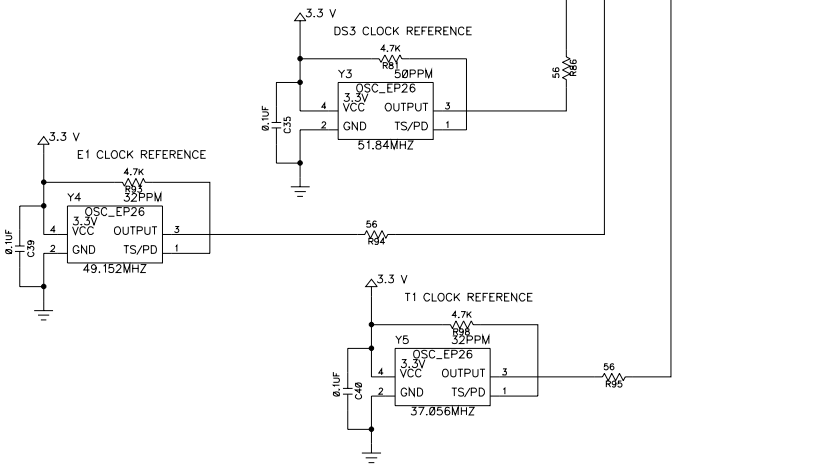
PMC-Sierra, Inc.

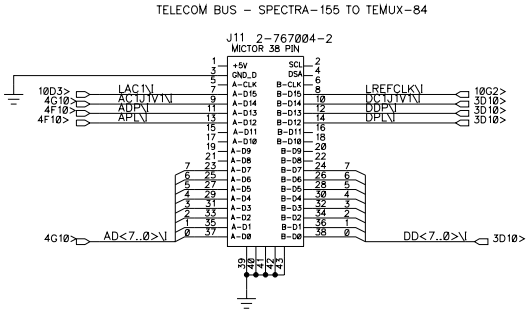
DOCUMENT NUMBER: 2002050 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84-TEMUX-84 DEV. KIT TEMUX-84 1/2	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)	PAGE: 4 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR









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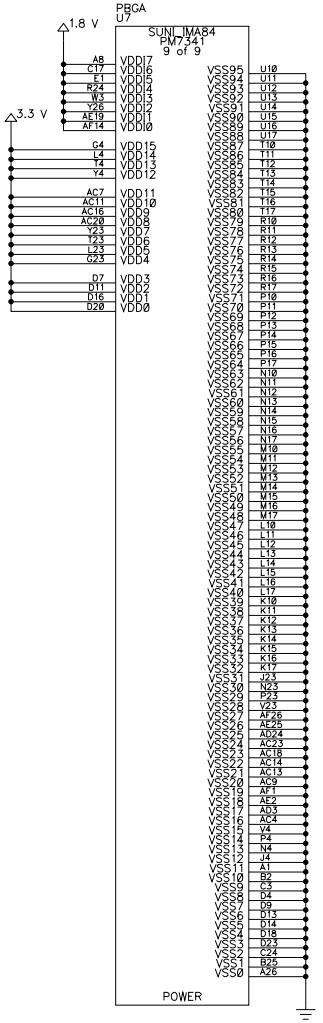
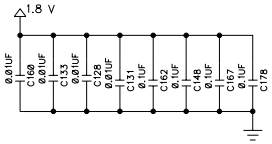
Fri May 18 15:36:39 2001

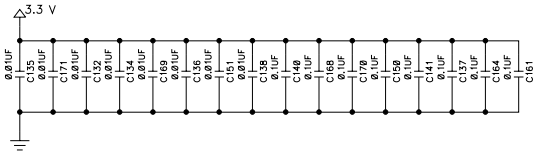
PMC-Sierra, Inc.

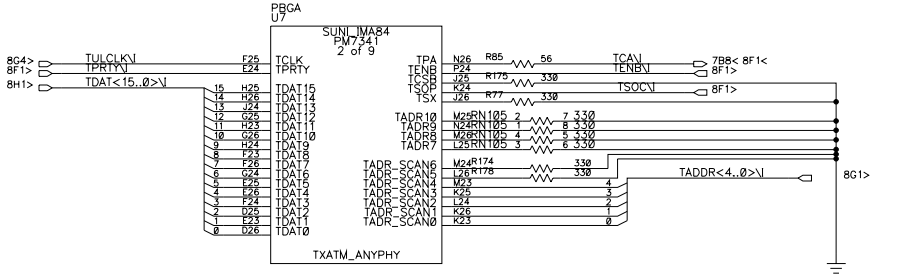
DOCUMENT NUMBER: 2002050 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT TEMUX-84 2/2	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)	PAGE: 5 OF 12

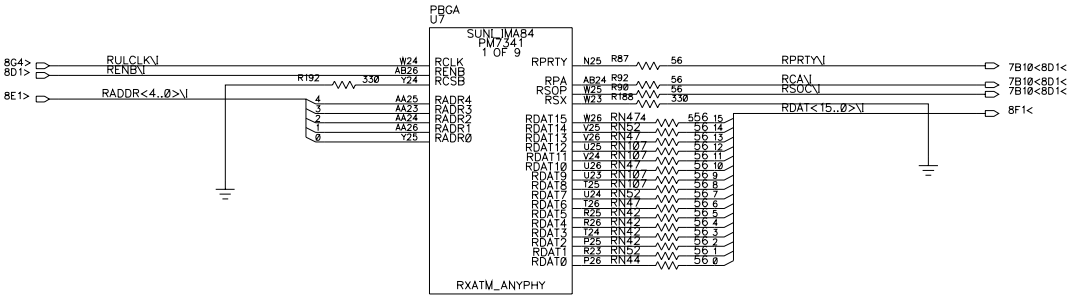
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

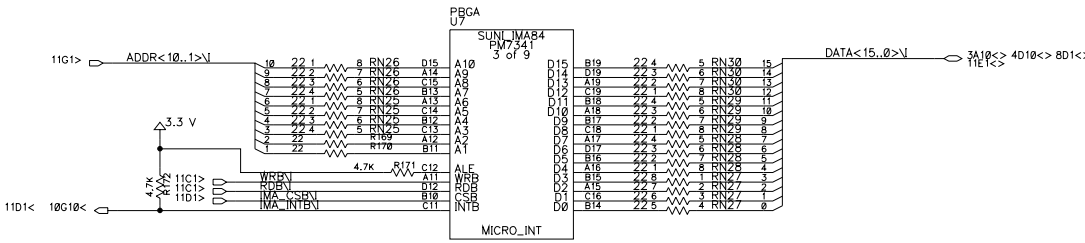


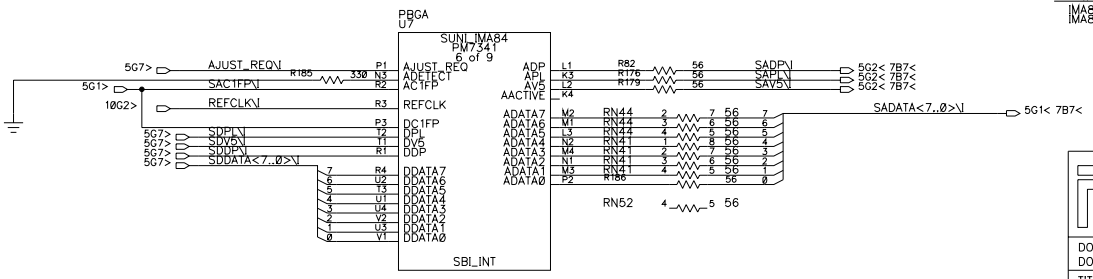












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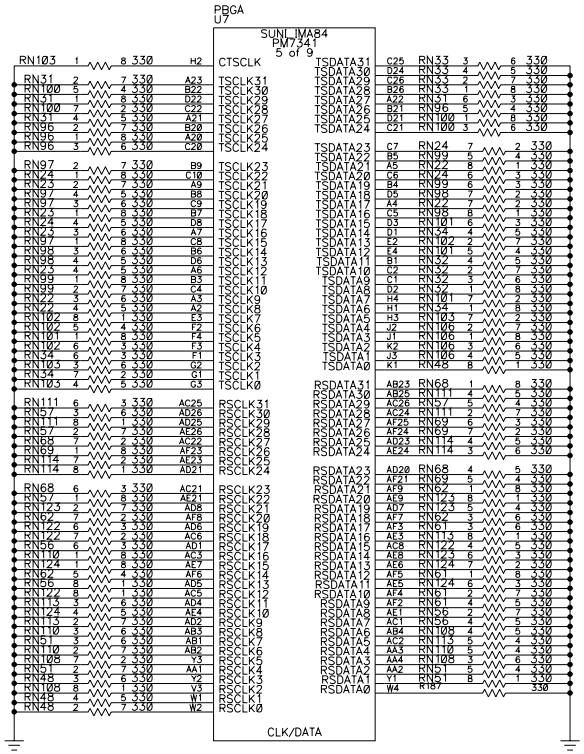
Fri May 18 15:36:15 2001

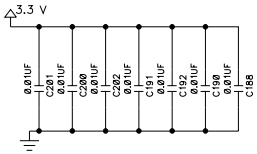
PMC-Sierra, Inc.

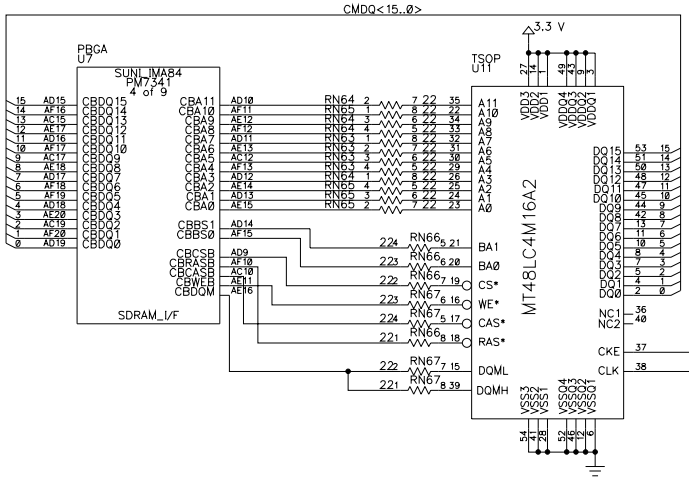
DOCUMENT NUMBER: 2002050 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT S/UNI-IMA-84 1/2	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)	PAGE: 6 OF 12

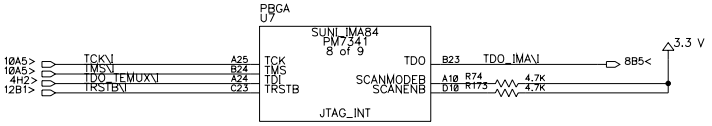
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

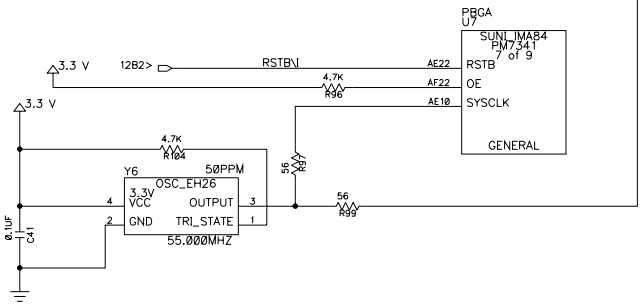


DECOUPLING CAPACITORS FOR EXTERNAL SDRAM

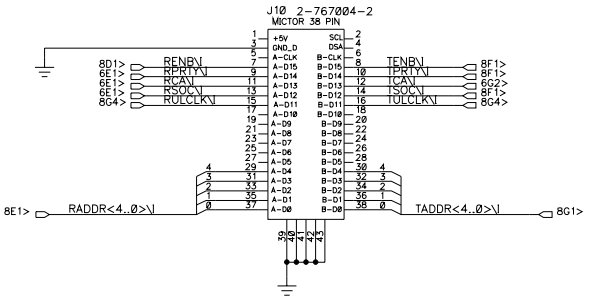




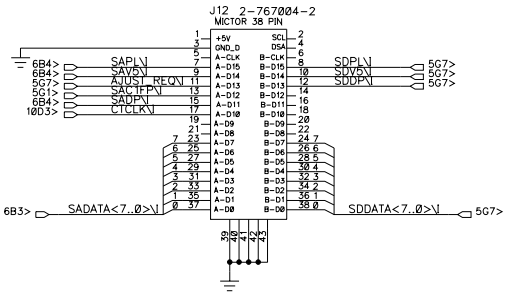




UTOPIA LEVEL2 BUS – S/UNI-IMA-84 TO S/UNI-DUPLEX



SBI BUS – TEMUX-84 TO S/UNI-IMA-84



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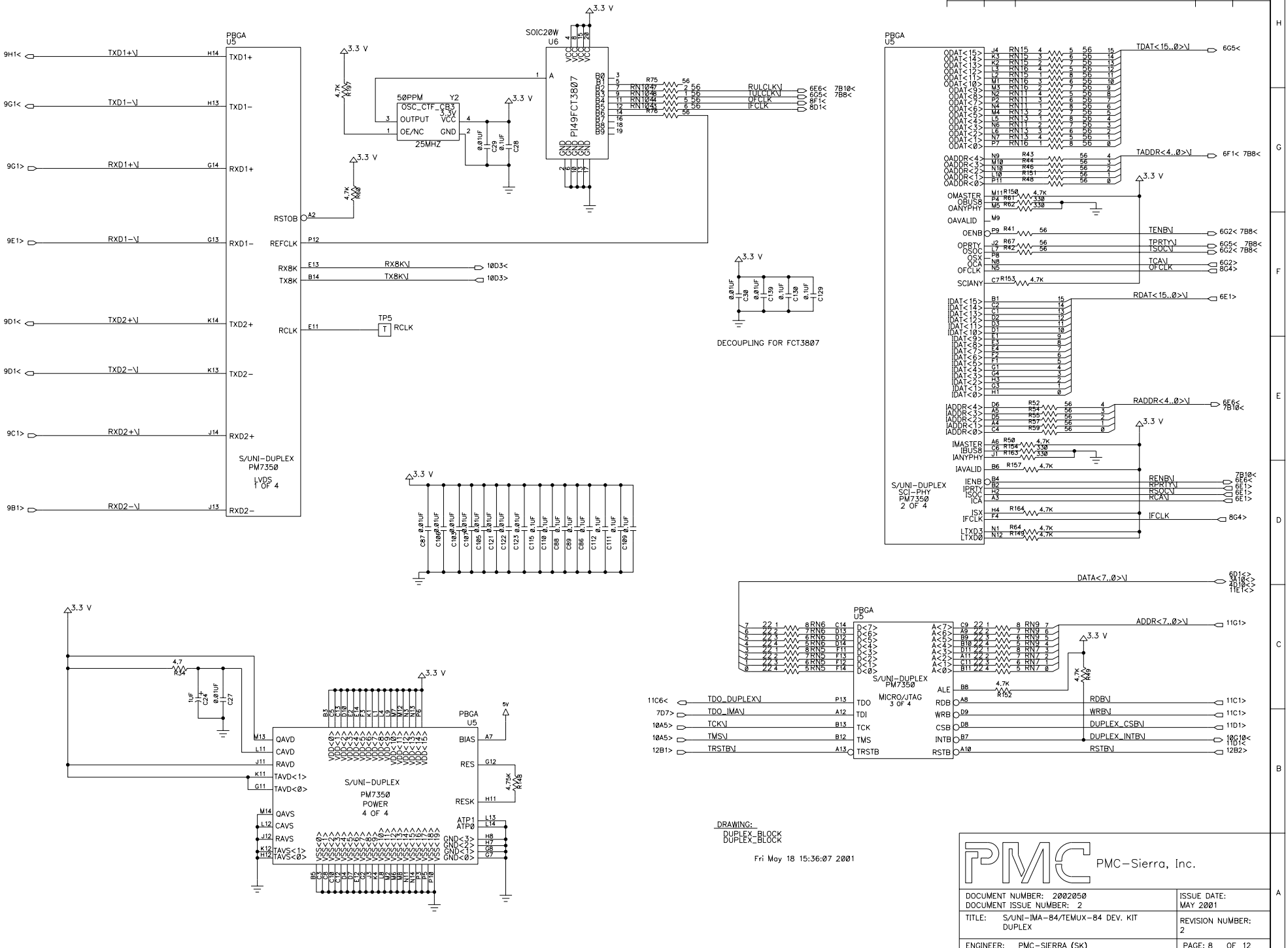
Fri May 18 15:36:26 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: 2002050 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT S/UNI-IMA-84 2/2	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)	PAGE: 7 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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Fri May 18 15:36:07 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: 2002050 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT DUPLEX	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)	PAGE: 8 OF 12

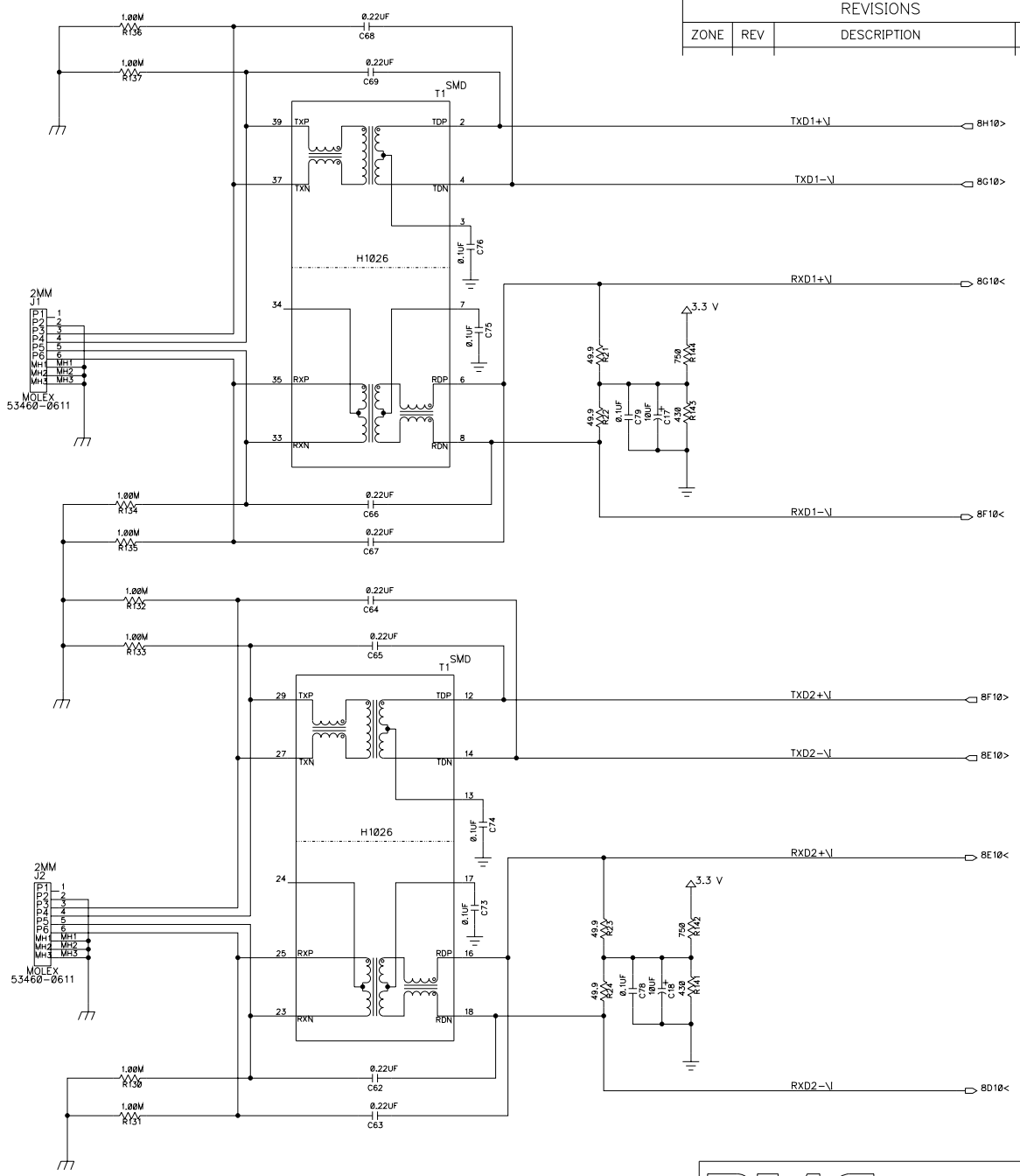
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

POPULATE WITH EITHER TRANSFORMERS OR CAPACITORS/RESISTORS, NOT BOTH

FOR TRANSFORMER COUPLING, POPULATE:
TRANSFORMER PACKAGE – T1

FOR CAPACITIVE COUPLING, POPULATE:
CAPACITORS C62–C69
RESISTORS R130–R137

ALL LVDS LINES 50 OHMS



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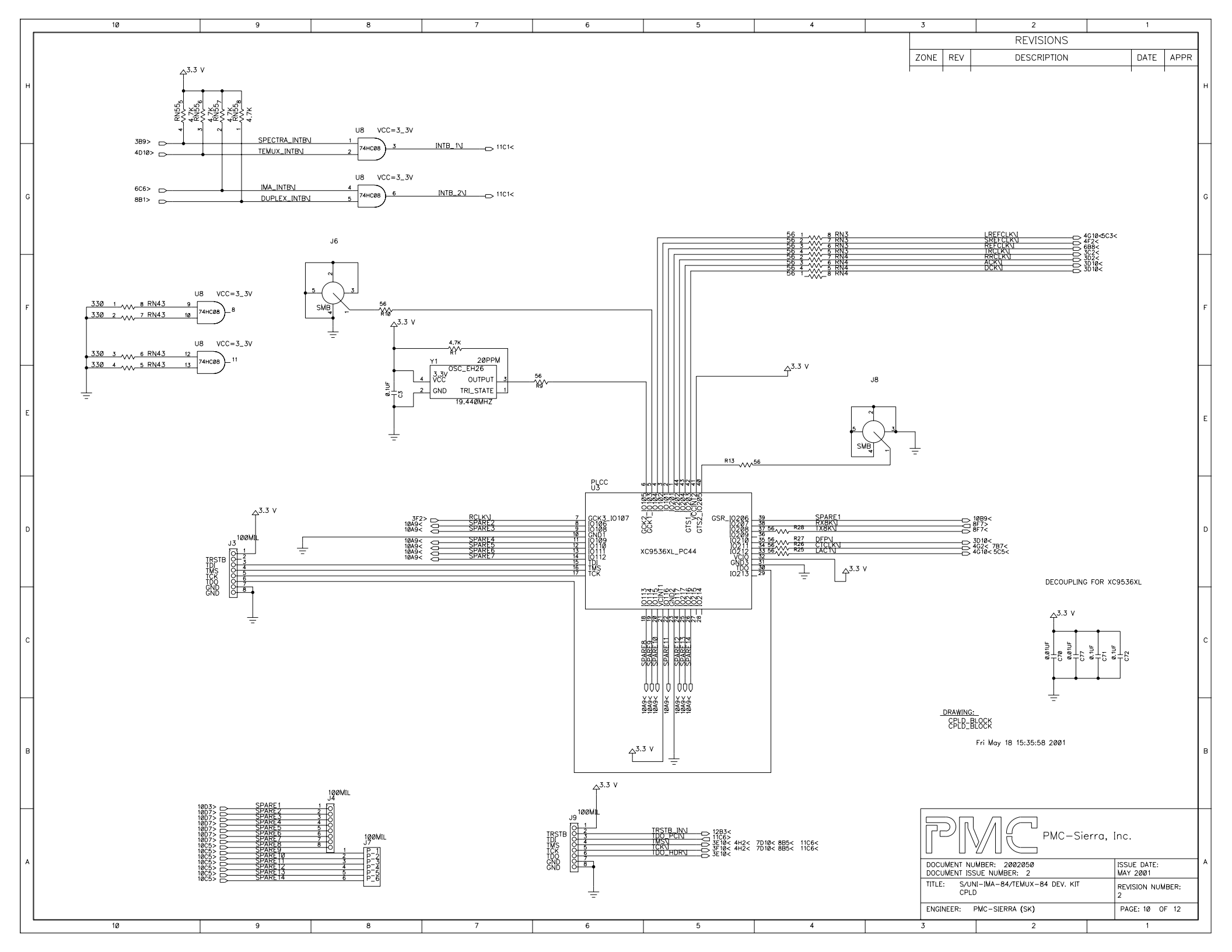
LVDS_BLOCK

Fri May 18 15:36:51 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: 2002050 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT LVDS INTEFACE	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)	PAGE: 9 OF 12


REVISIONS
ZONE REV DESCRIPTION DATE APPR
3.3 V
RN55 4.7K
RN56 4.7K
RN57 4.7K
RN58 4.7K
U8 VCC=3_3V
74HC08
3B9>
4D10>
SPECTRA_INTB\
TEMUX_INTB\
INTB_1\
11C1<
6C6>
8B1>
IMA_INTB\
DUPLEX_INTB\
INTB_2\
J6
SMB
56
R10
330
RN43
R1
4.7K
Y1
20PPM
OSC_EH26
3.3V
VCC
GND
OUTPUT
TRI_STATE
19.440MHZ
C3
0.1UF
R9
J8
R13
PLCC
U3
XC9536XL_PC44
3F2>
RCLK\
10A9<
SPARE1
SPARE2
SPARE3
SPARE4
SPARE5
SPARE6
SPARE7
GCK3_IO107
IO108
IO109
IO110
IO111
IO112
TDI
TMS
TCK
GSR_IO206
IO207
IO208
IO209
IO210
IO211
IO212
IO213
VCIO
GND3
TDO
R28
R27
R26
R25
SPARE1
RXBK\
TXBK\
DFP\
CTCLK\
LAC1\
10B9<
8F7>
8F7<
3D10<
4G2< 7B7<
4G10< 5C5<
J3
100MIL
TRSTB
TDI
TMS
TCK
TDO
GND
GND
DECOUPLING FOR XC9536XL
C70 0.01UF
C77 0.1UF
C71 0.1UF
C72 0.1UF
DRAWING:
CPLD_BLOCK
CPLD_BLOCK
Fri May 18 15:35:58 2001
J4
J7
10D3>
10D7>
10C5>
SPARE8
SPARE9
SPARE10
SPARE11
SPARE12
SPARE13
SPARE14
P_1
P_2
P_3
P_4
P_5
P_6
J9
TRSTB_IN\
TDO_PCN\
TMS\
TCK\
TDO_HDR\
12B3<
11C6>
3E10< 4H2< 7D10< 8B5< 11C6<
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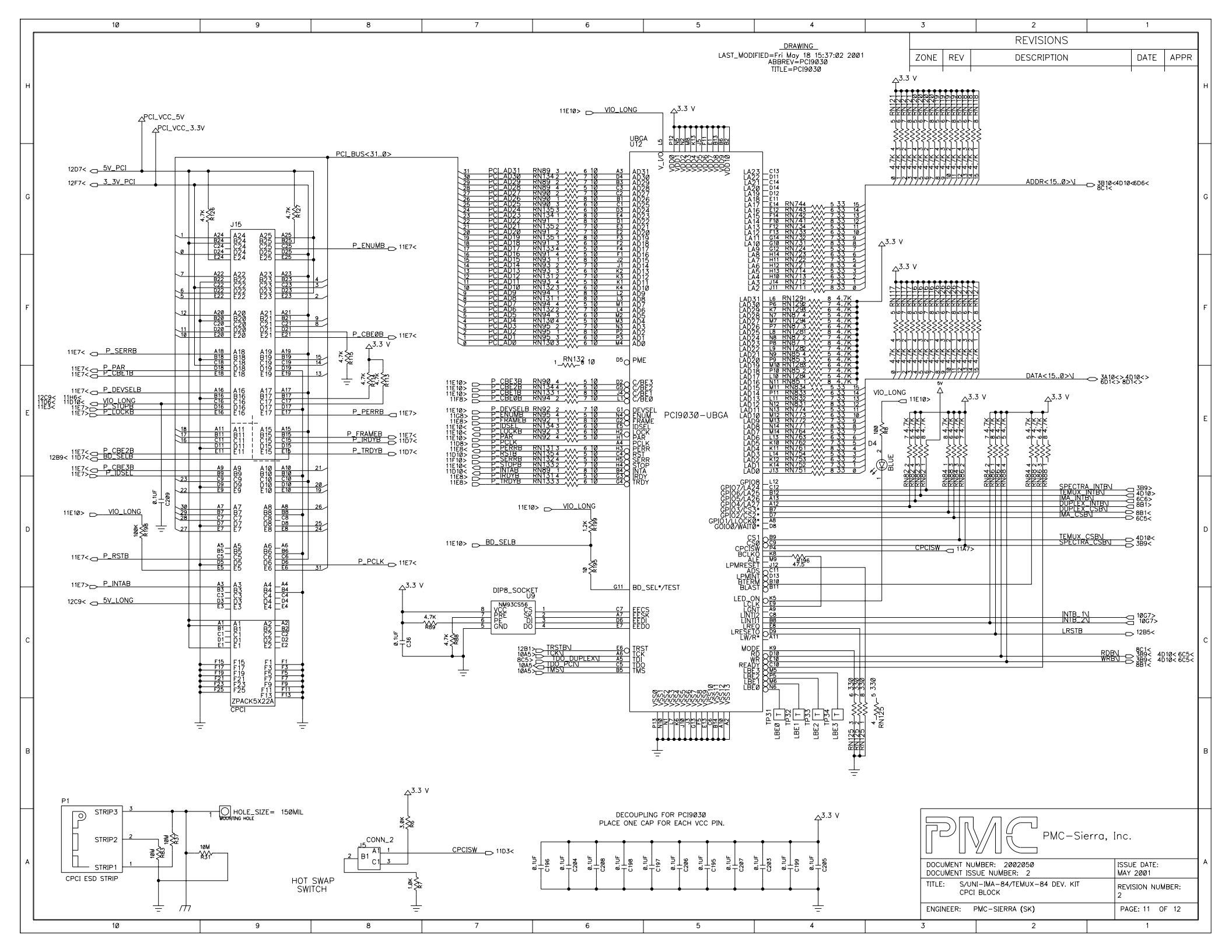
3E10<
PMC PMC-Sierra, Inc.
DOCUMENT NUMBER: 2002050
DOCUMENT ISSUE NUMBER: 2
ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT CPLD
REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)
PAGE: 10 OF 12

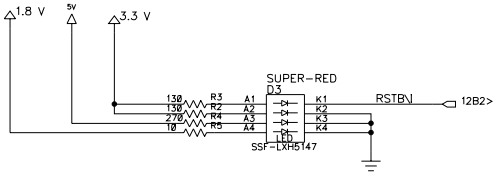

DRAWING
LAST_MODIFIED=Fri May 18 15:37:02 2001
ABBREV=PCI9030
TITLE=PCI9030
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPR
PCI9030-UBGA
UBGA
U12
J15
ZPACK5X22A
CPCI
DIP8_SOCKET
U9
NM93CS56
CPCI ESD STRIP
HOT SWAP
SWITCH
CONN_2
DECOUPLING FOR PCI9030
PLACE ONE CAP FOR EACH VCC PIN.
PMC-Sierra, Inc.
DOCUMENT NUMBER: 2002050
DOCUMENT ISSUE NUMBER: 2
ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT CPCI BLOCK
REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)
PAGE: 11 OF 12

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

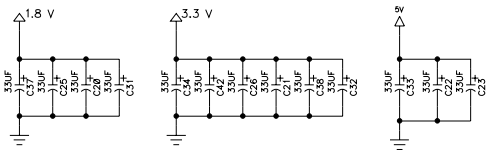
DRAWING

PCI9030
PCI9030
LAST_MODIFIED=Fri May 18 15:37:08 2001

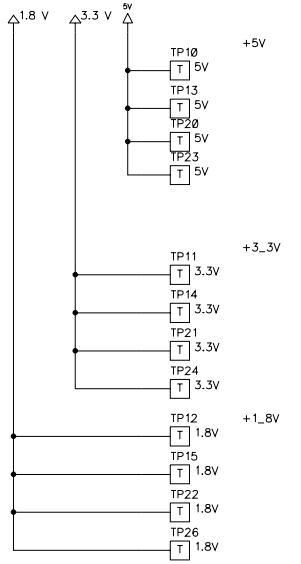
POWER / RESET INDICATORS



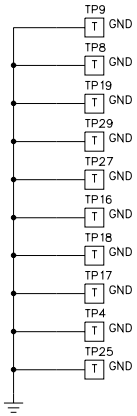
BULK CAPACITORS

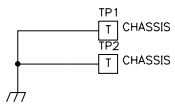


POWER SUPPLY TEST POINTS

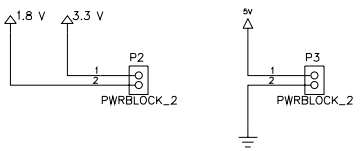


GND TESTPOINTS





MOUNTING HOLES FOR DIRECT POWER SUPPLY



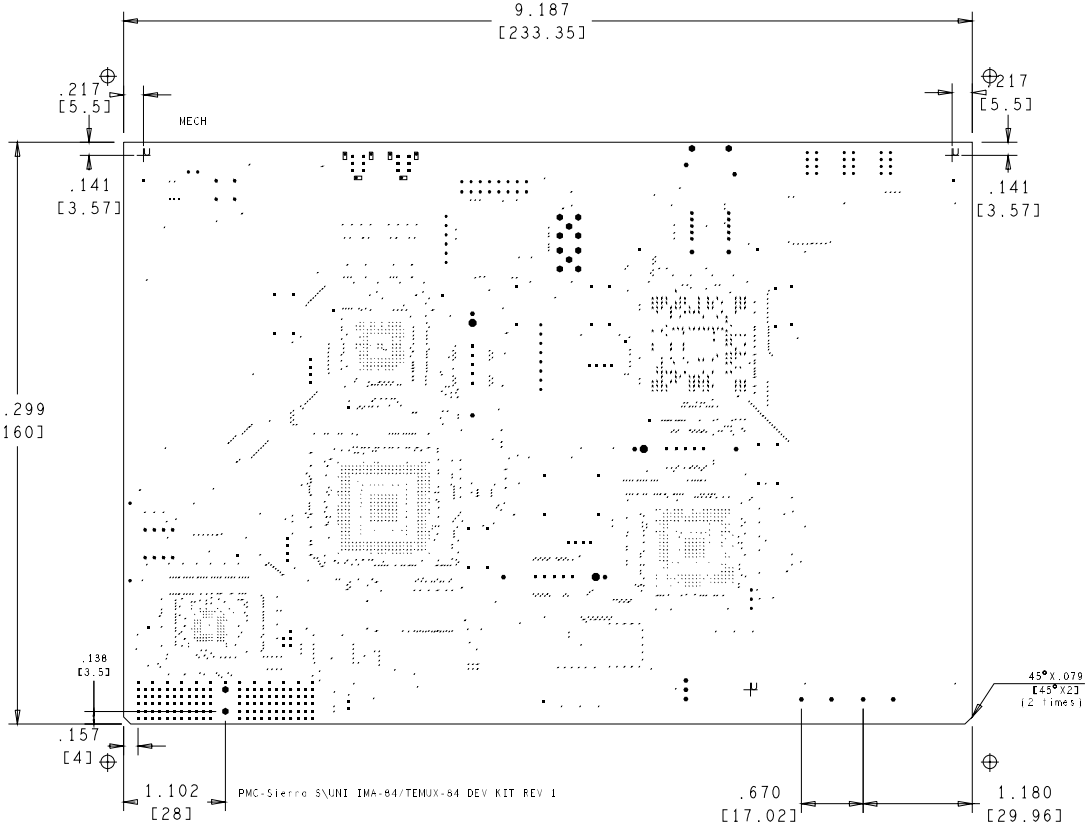
PMC-Sierra, Inc.

DOCUMENT NUMBER: 2002050 DOCUMENT ISSUE NUMBER: 2	ISSUE DATE: MAY 2001
TITLE: S/UNI-IMA-84/TEMUX-84 DEV. KIT POWER SUPPLY AND HOT SWAP	REVISION NUMBER: 2
ENGINEER: PMC-SIERRA (SK)	PAGE: 12 OF 12

15 APPENDIX C: LAYOUT

16 APPENDIX D: VHDL CODE FOR CPLD

REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED



	ARTWORK FILM
#	TOP LAYER
	GND1_PLANE
	5V_PLANE
#	SIG1 LAYER
	3V3_PLANE
	GND2_PLANE
#	SIG2 LAYER
	1V8_PLANE
	GND3_PLANE
#	BOTTOM LAYER
	SILKSCREEN TOP
	SILKSCREEN BOTTOM
	SOLDER MASK TOP
	SOLDER MASK BOTTOM
	SOLDER PASTE TOP
	SOLDER PASTE BOTTOM
	MECH DRAWING
	ASSY TOP
	ASSY BOTTOM

Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
FR-4	DIELECTRIC	-------	-------	5 mil	4.5
COPPER	CONDUCTOR	GND1_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	3 mil	4.5
COPPER	CONDUCTOR	5V_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	13 mil	4.5
COPPER	CONDUCTOR	SIG1	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	13 mil	4.5
COPPER	CONDUCTOR	3V3_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	3 mil	4.5
COPPER	CONDUCTOR	GND2_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	13 mil	4.5
COPPER	CONDUCTOR	SIG2	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	13 mil	4.5
COPPER	CONDUCTOR	1V8_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	3 mil	4.5
COPPER	CONDUCTOR	GND3_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	5 mil	4.5
COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------

Note: Controlled impedance traces are used on all signal layers.
They are: for 50 Ohm - 0.009"
for 65 Ohm - 0.005"

FINISHED HOLES SIZE			
All Units are in mils			
FIGURE	SIZE	PLATED	QTY
·	8.0	PLATED	849
·	12.0	PLATED	168
·	13.0	PLATED	1176
·	20.0	PLATED	3
·	25.0	PLATED	61
·	26.0	PLATED	123
·	32.0	PLATED	27
·	36.0	PLATED	59
·	39.0	PLATED	6
·	39.37	PLATED	2
·	42.0	PLATED	22
•	55.0	PLATED	17
•	79.0	PLATED	12
⊕	149.606	PLATED	1
⊕	150.0	PLATED	2
•	78.74	NOT PLATED	2
•	94.0	NOT PLATED	3

NOTES:

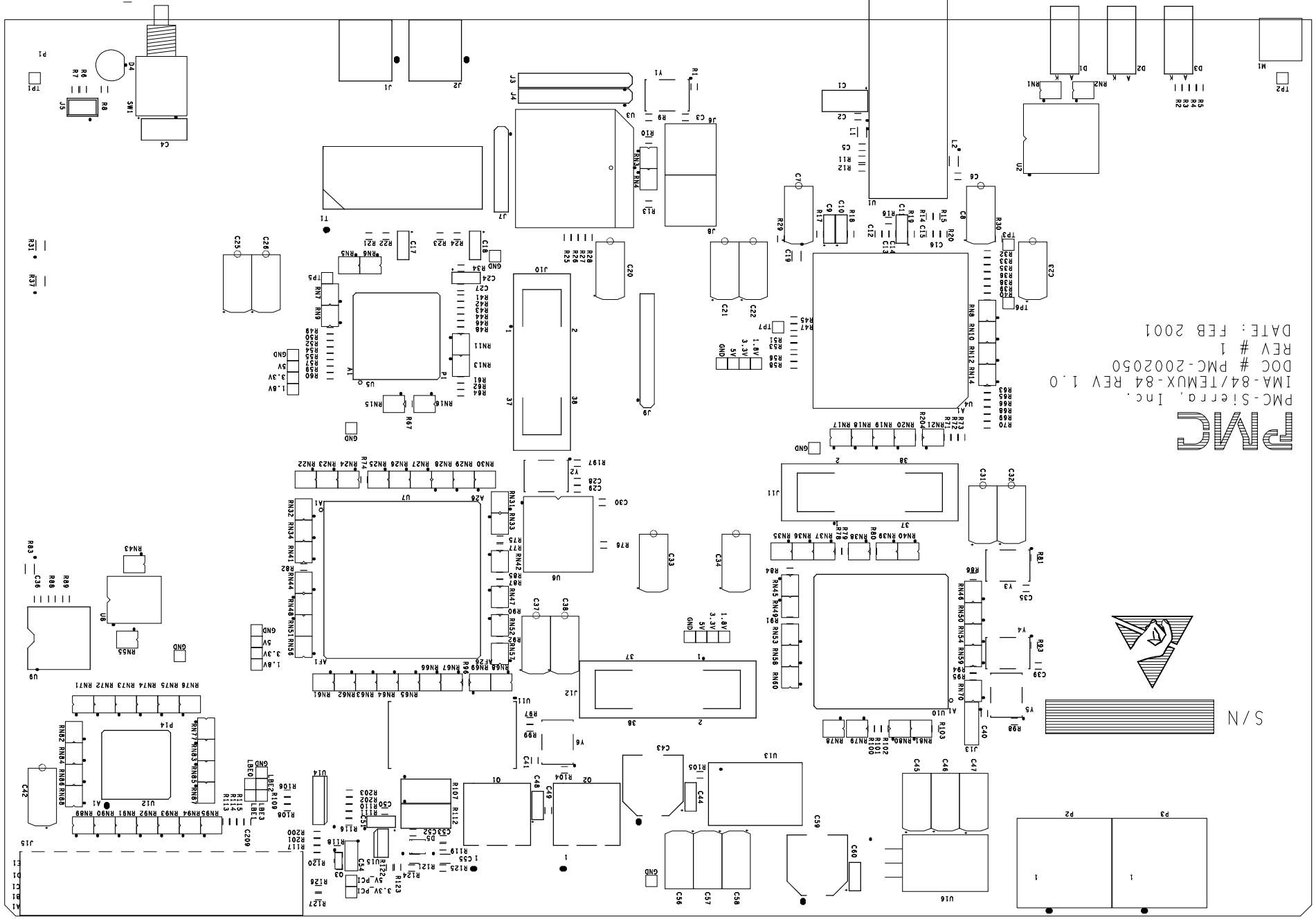
1. COPPER THICKNESS IS 1/2 OZ ON OUTER LAYER AND 1 OZ ON INNER LAYERS, UNLESS OTHERWISE STATED.
2. TOTAL THICKNESS OF BOARD SHALL BE 84 MIL +/- 7 MIL.
3. MATERIAL: FR4 WITH IMMERSION GOLD SURFACE FINISH.
4. THE OUTLINE DIMENSION ARE SPECIFIED ON THIS DRAWING.
5. ALL HOLES SHALL HAVE 1 MIL MINIMUM COPPER WALL THICKNESS.
6. SOLDER MASK MATERIAL: LIGHT GREEN LIQUID PHOTOIMAGEABLE.
7. DIELECTRIC CONSTANT: SEE BOARD MATERIAL DETAILS ABOVE.
8. SILKSCREEN SHALL BE SCREENED IN NONCONDUCTIVE WHITE BASE INK AND MUST BE CLIPPED AWAY FROM SOLDER PADS/VIAS.
9. MAXIMUM WARP AND TWIST OF FINISHED PCB SHALL NOT EXCEED 0.010 IN/IN PER IPC-D-300.
10. ALL MATERIAL COMPRISING THE PCB MUST BE RECOGNIZED BY UL TO THE 94V-0 RATING.
11. TEARDROPS MAY BE ADDED FOR INNER LAYER VIAS FOR MANUFACTUREABLITY IF NECESSARY.
12. UNFUNCTIONAL INNER LAYERS VIAS/PADS HAVE TO BE REMOVED FOR MANUFACTUREABILITY.
13. PLATED HOLES MARKED WITH SQUARE R-0.026" SHALL BE WITHIN +0.004"/-0.0" TOLERANCE.
14. TRACE WIDTH 9 MIL ON OUTER LAYERS ARE 50 OHM +/-10% CONTROLLED IMPEDANCE.
    TRACE WIDTH 5 MIL ON OUTER LAYERS ARE 65 OHM +/-10% CONTROLLED IMPEDANCE.
    TRACE WIDTH 9 MIL ON INNER LAYERS ARE 50 OHM +/-10% CONTROLLED IMPEDANCE.
    TRACE WIDTH 5 MIL ON INNER LAYERS ARE 65 OHM +/-10% CONTROLLED IMPEDANCE.

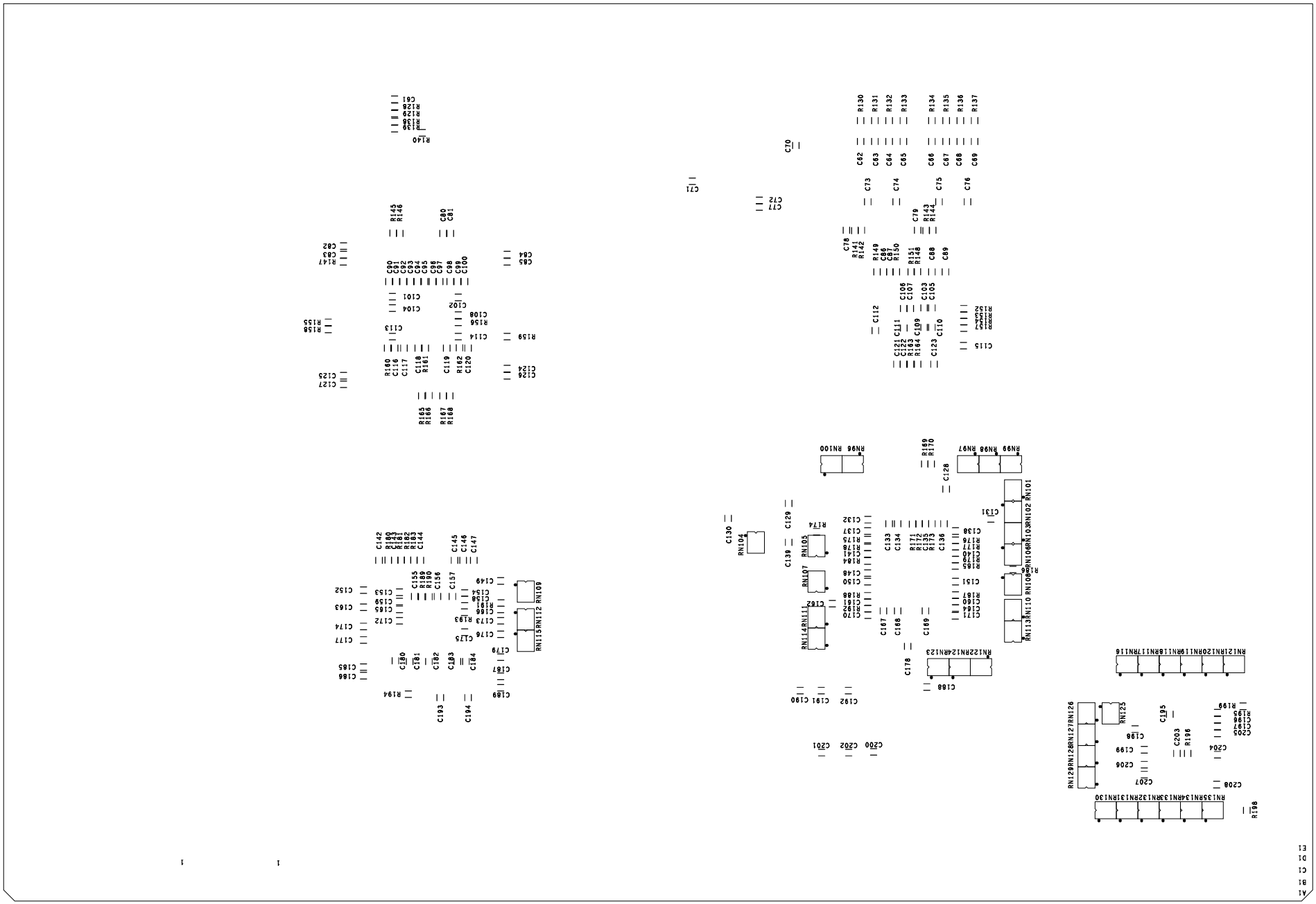
UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN			
TOLERANCES ON;				
2 PL DECIMALS ±	CHECKED			
3 PL DECIMALS ±	ENGRG			
ANGLES ±	ISSUED			
FRACTIONS ±				
DOC# PMC-2002050				
DOC ISSUE# 1				
REV # 1.0				
DATE: JAN 2001				

PMC-Sierra, Inc.
105-8555 Baxter Place, Burnaby B.C. Canada, V5A 4V7
Tel: 604 415-6000 Fax: 604 415-6200

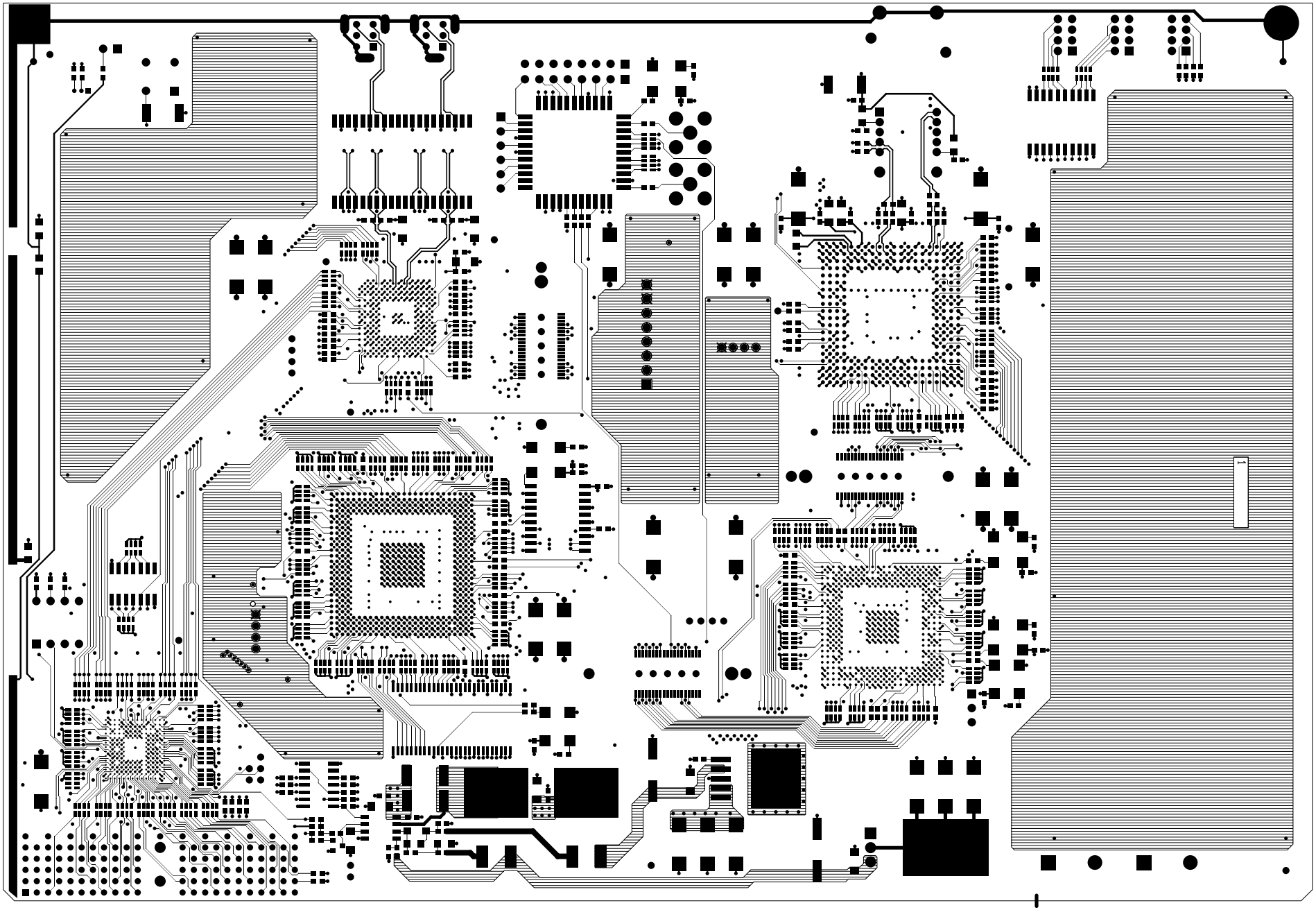
SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF

SILKSCREEN_TOP



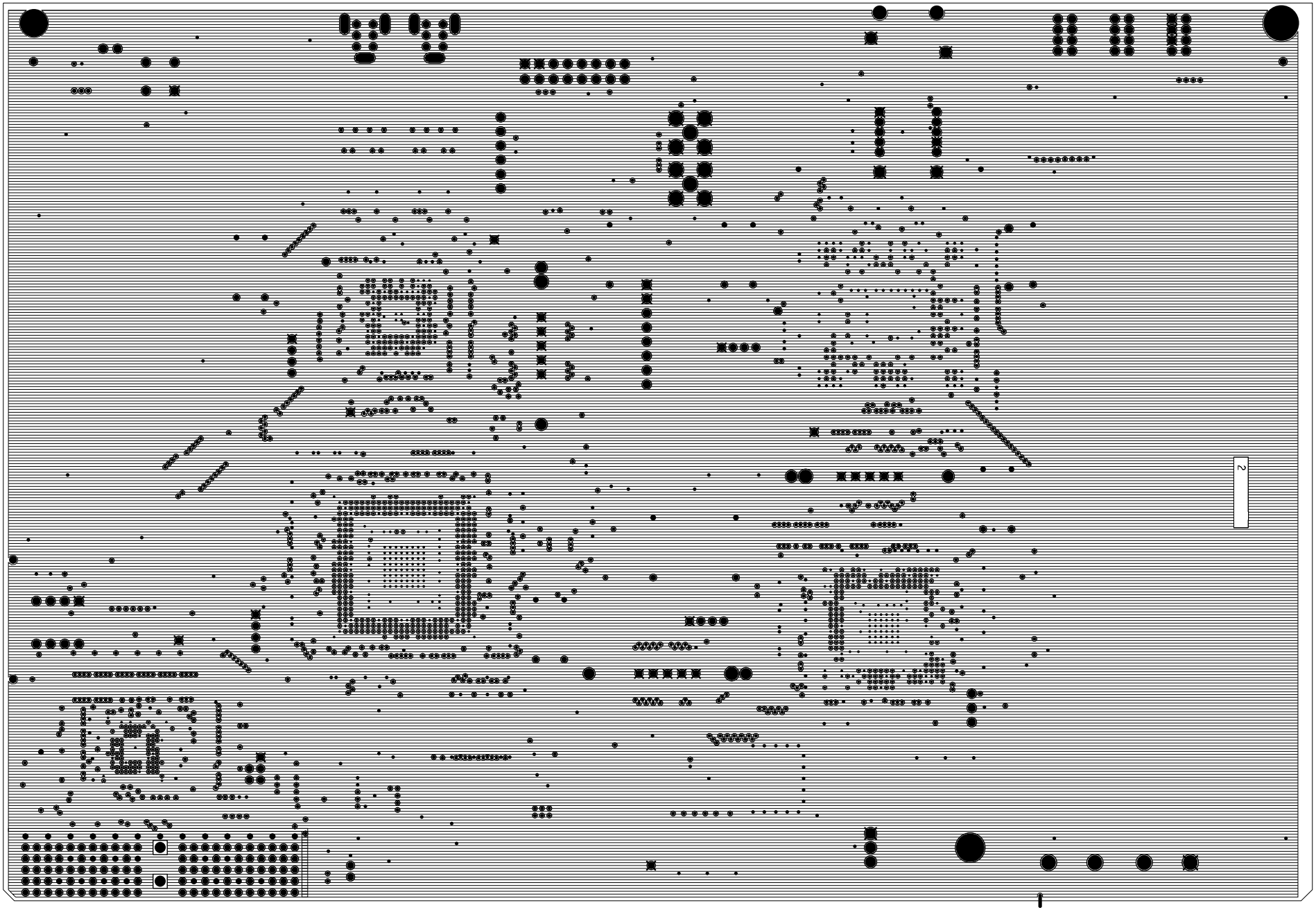


TOP



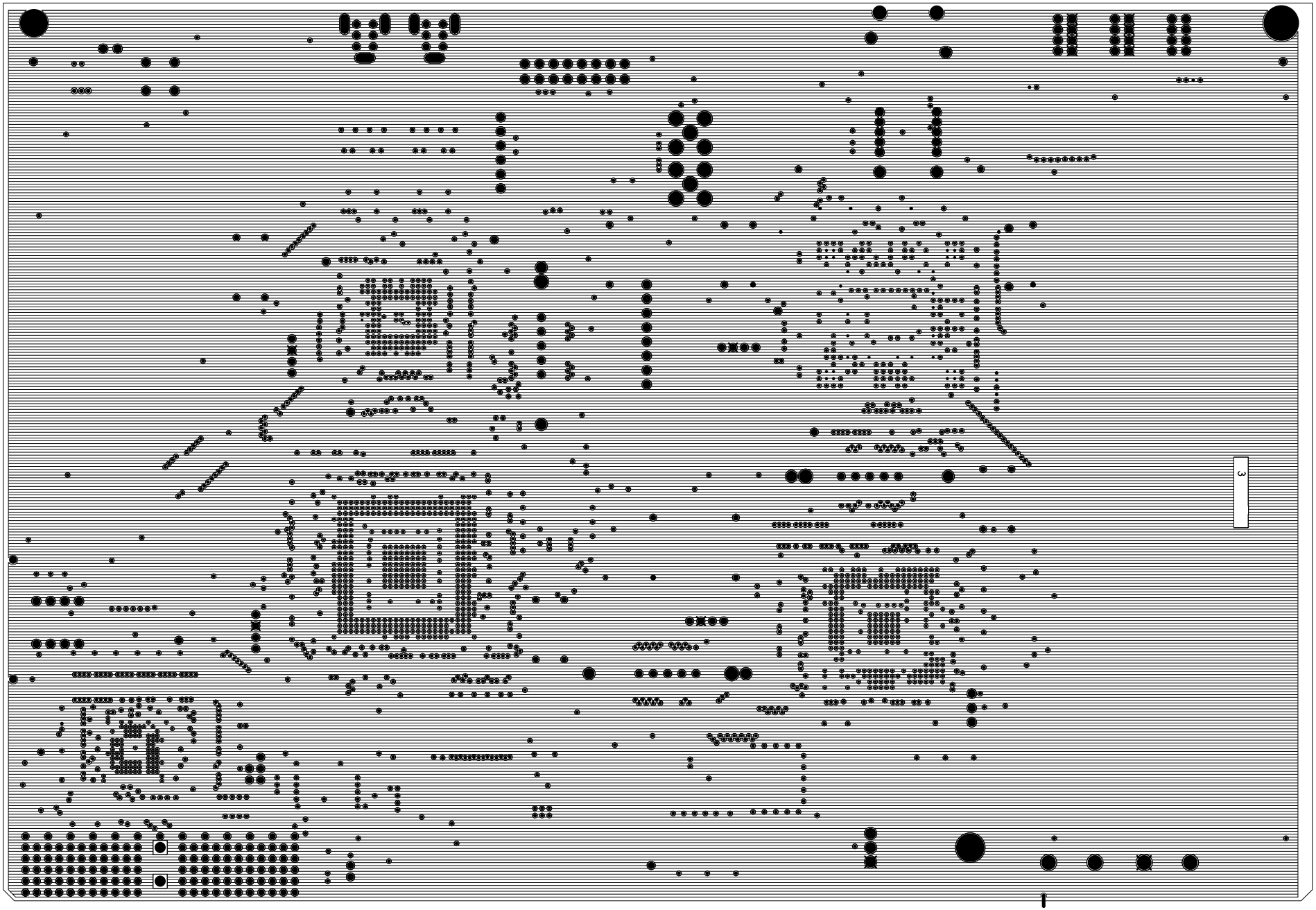
PMC-Sierra S\UNI IMA-84/TEMUX-84 DEV KIT REV 1

GND1_PLANE

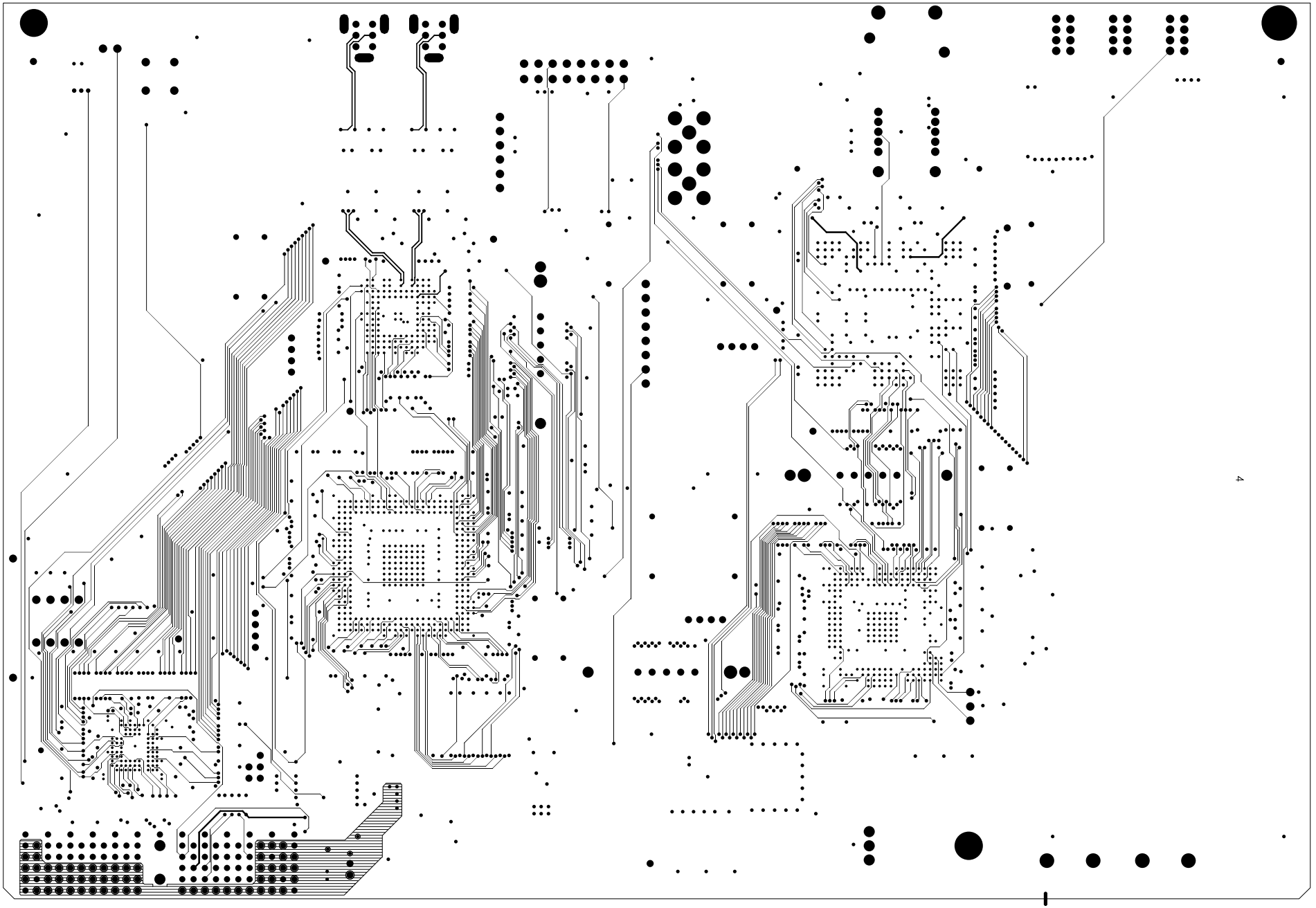


PMC-Sierra S\UNI IMA-84/TEMUX-84 DEV KIT REV 1

5V_PLANE

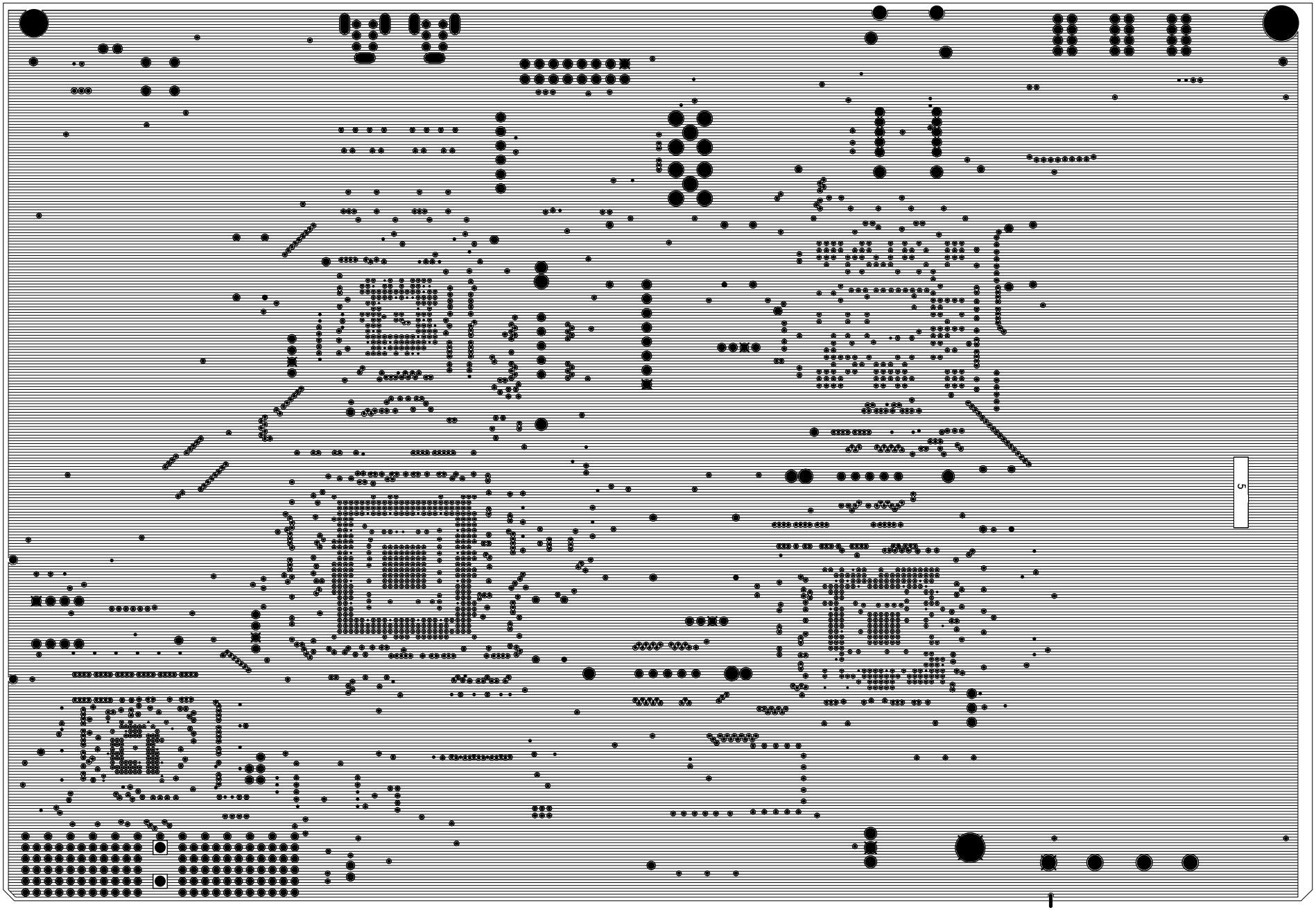


SIG1

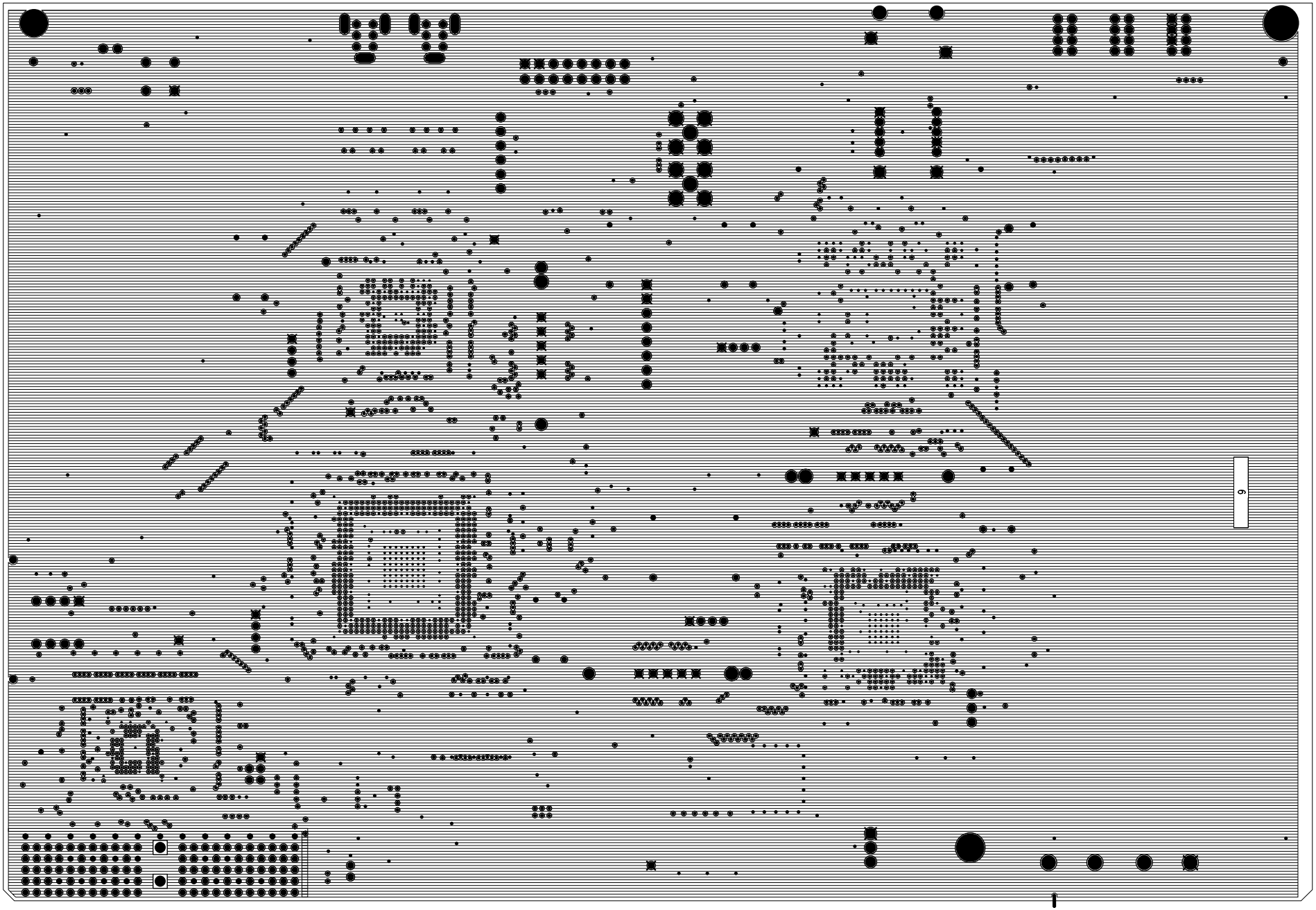


4

3V3_PLANE

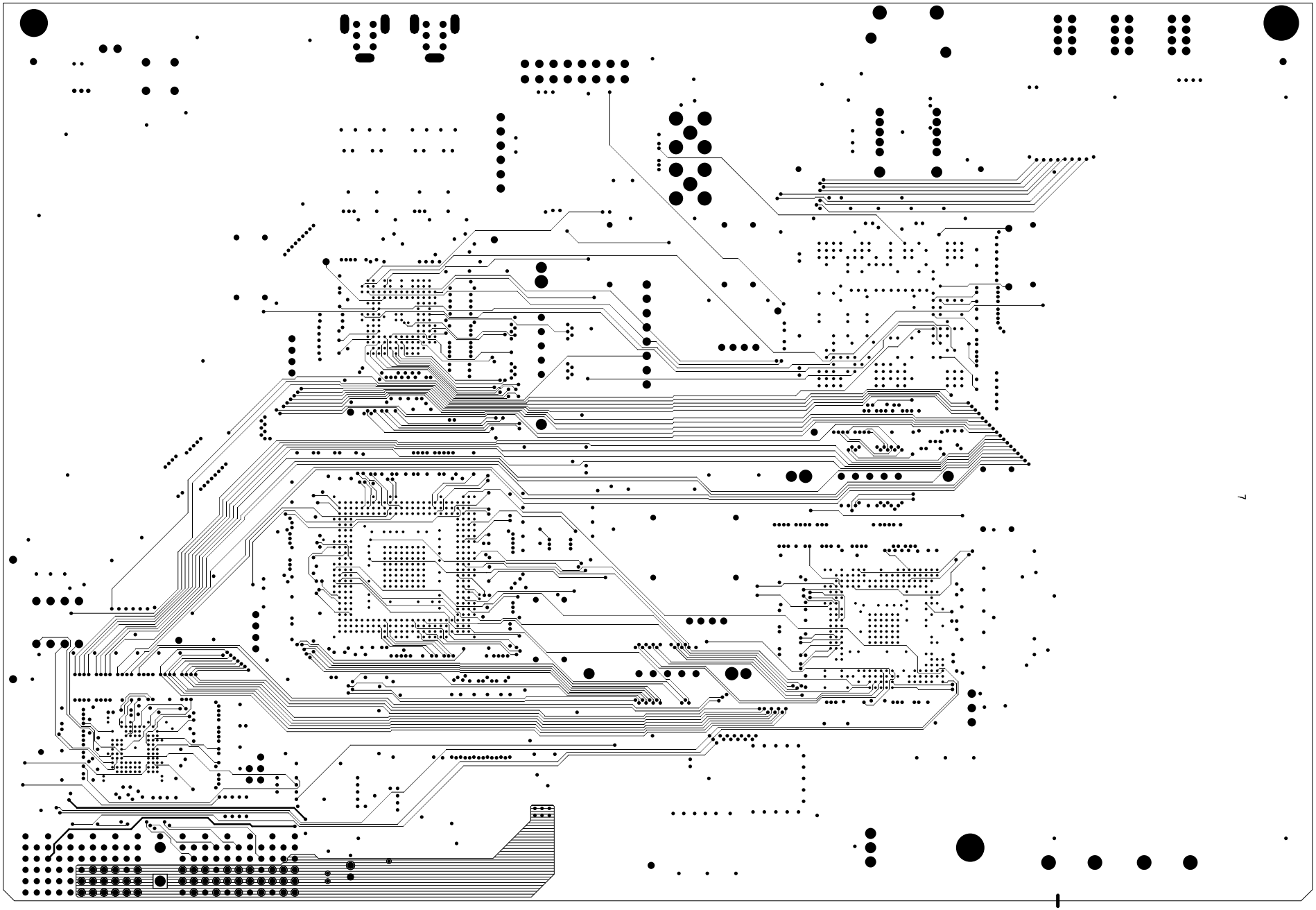


GND2_PLANE



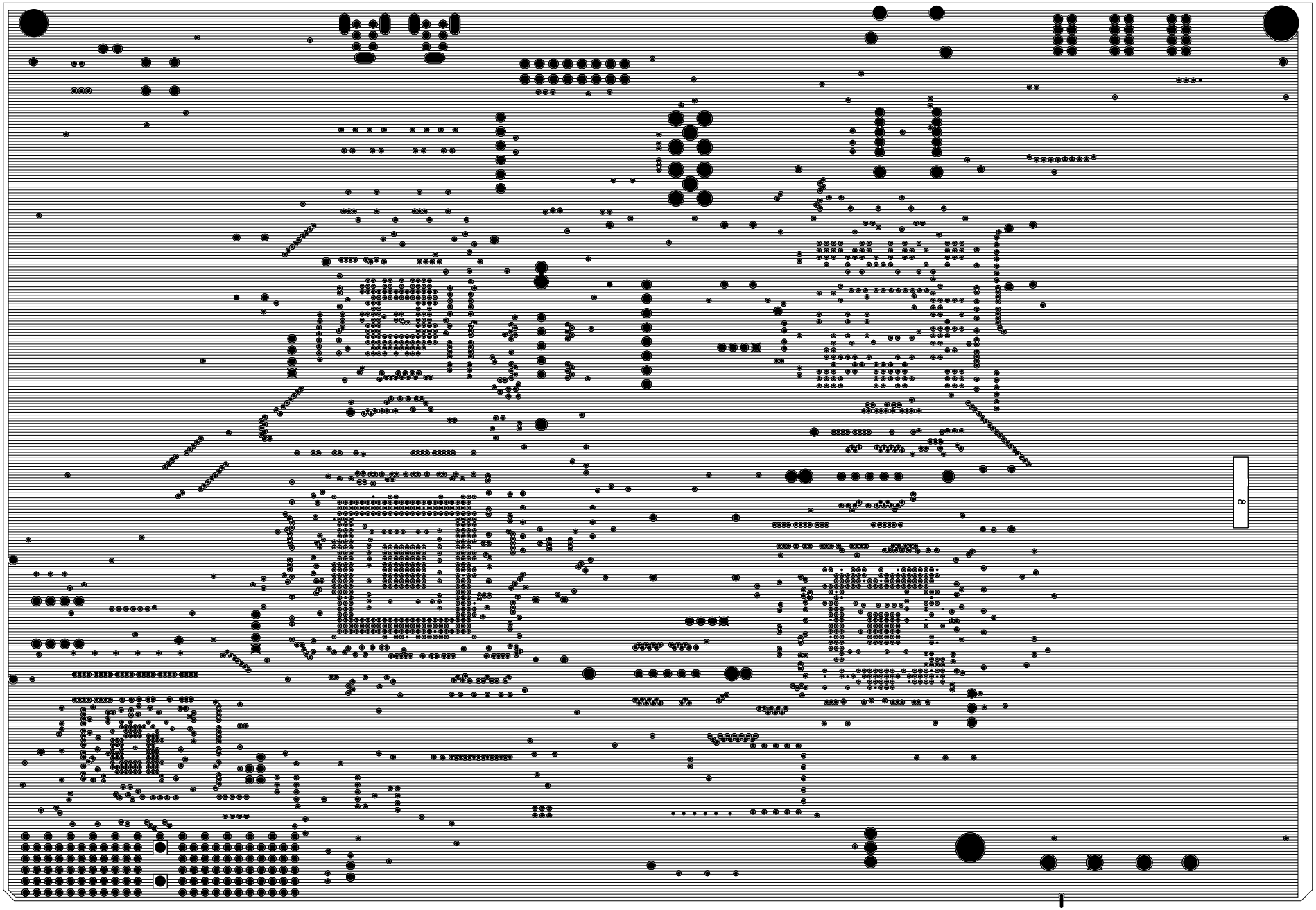
PMC-Sierra S\UNI IMA-84/TEMUX-84 DEV KIT REV 1

SIG2



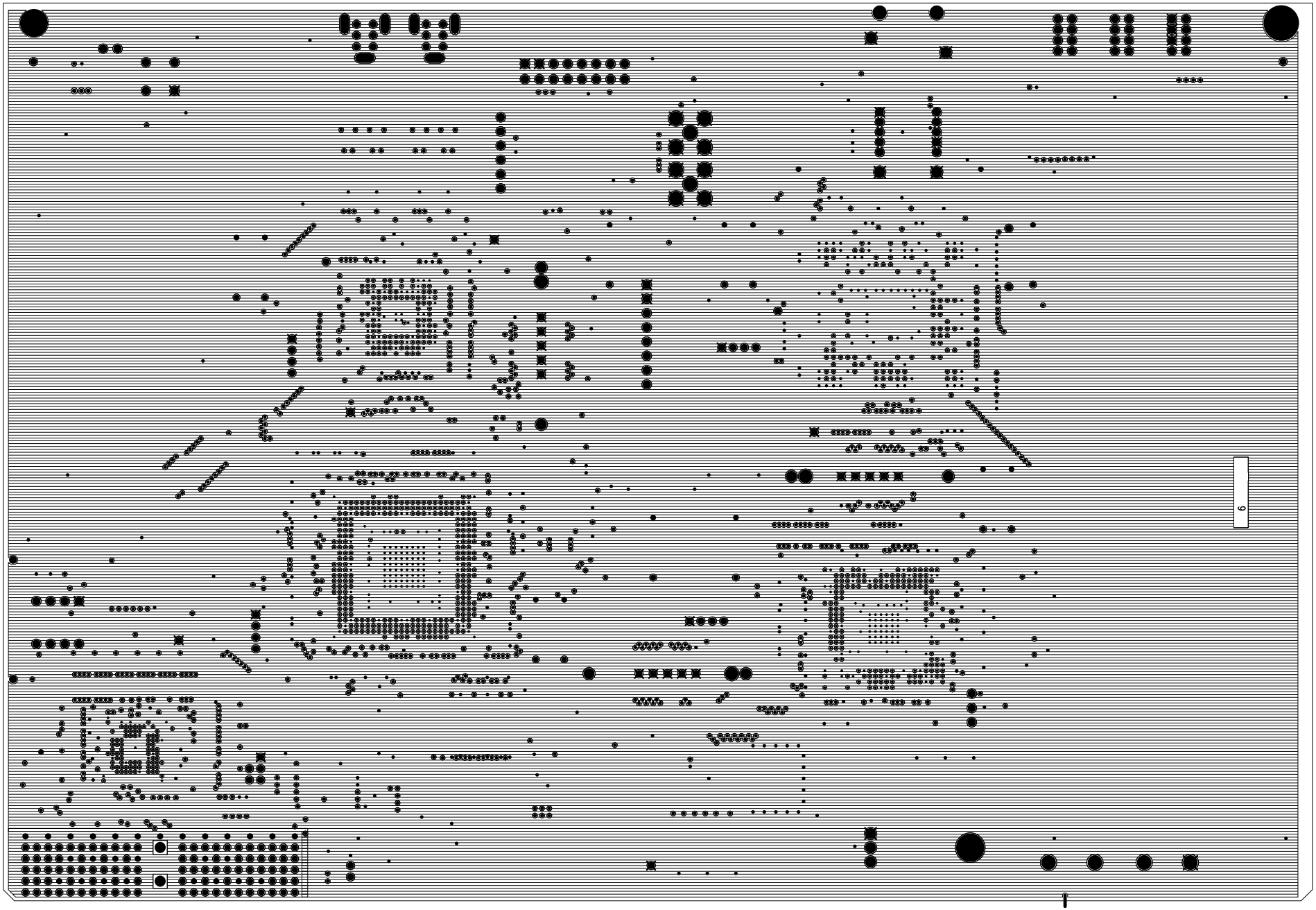
PMC-Sierra S\UNI IMA-84/TEMUX-84 DEV KIT REV 1

1V8_PLANE

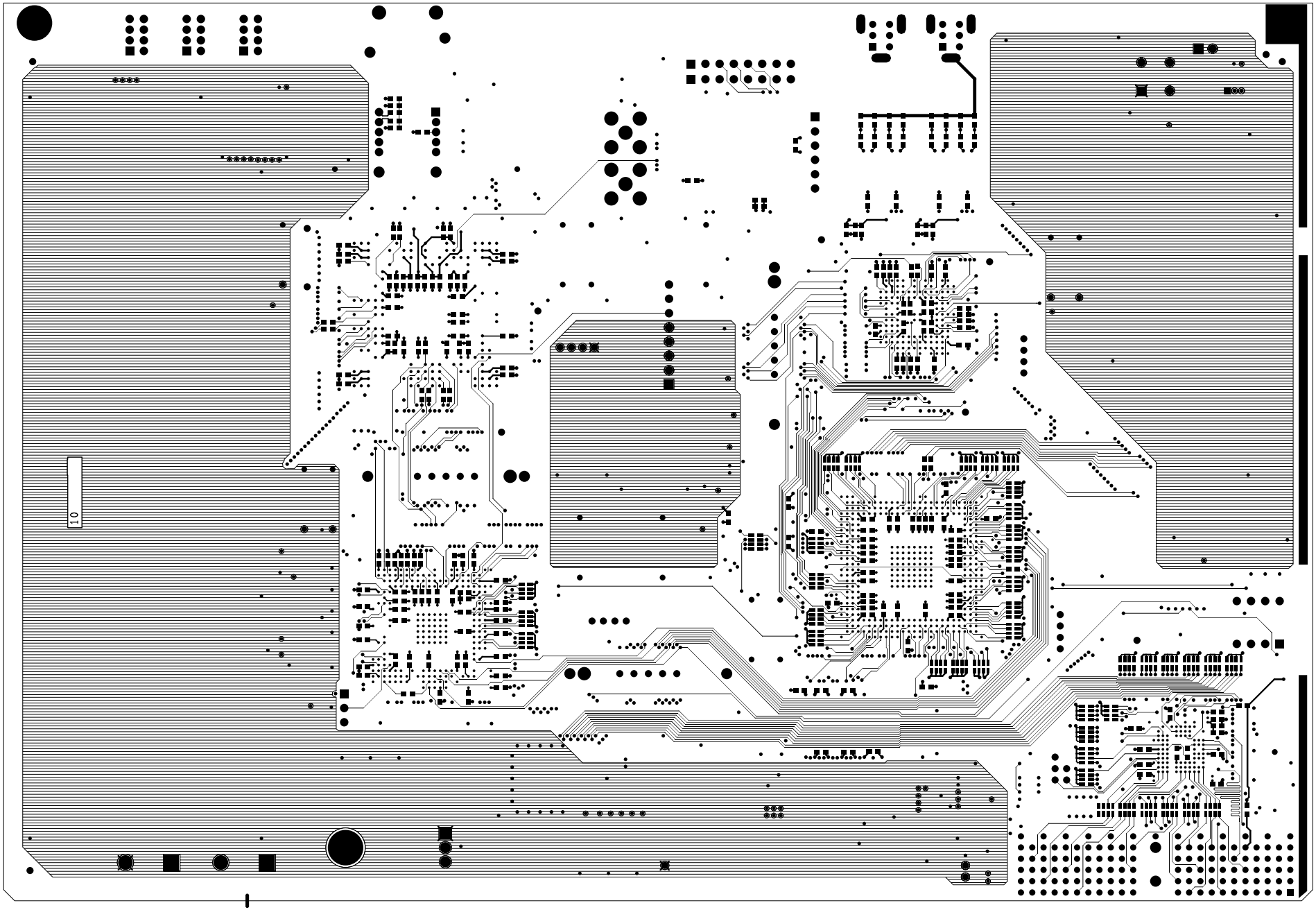


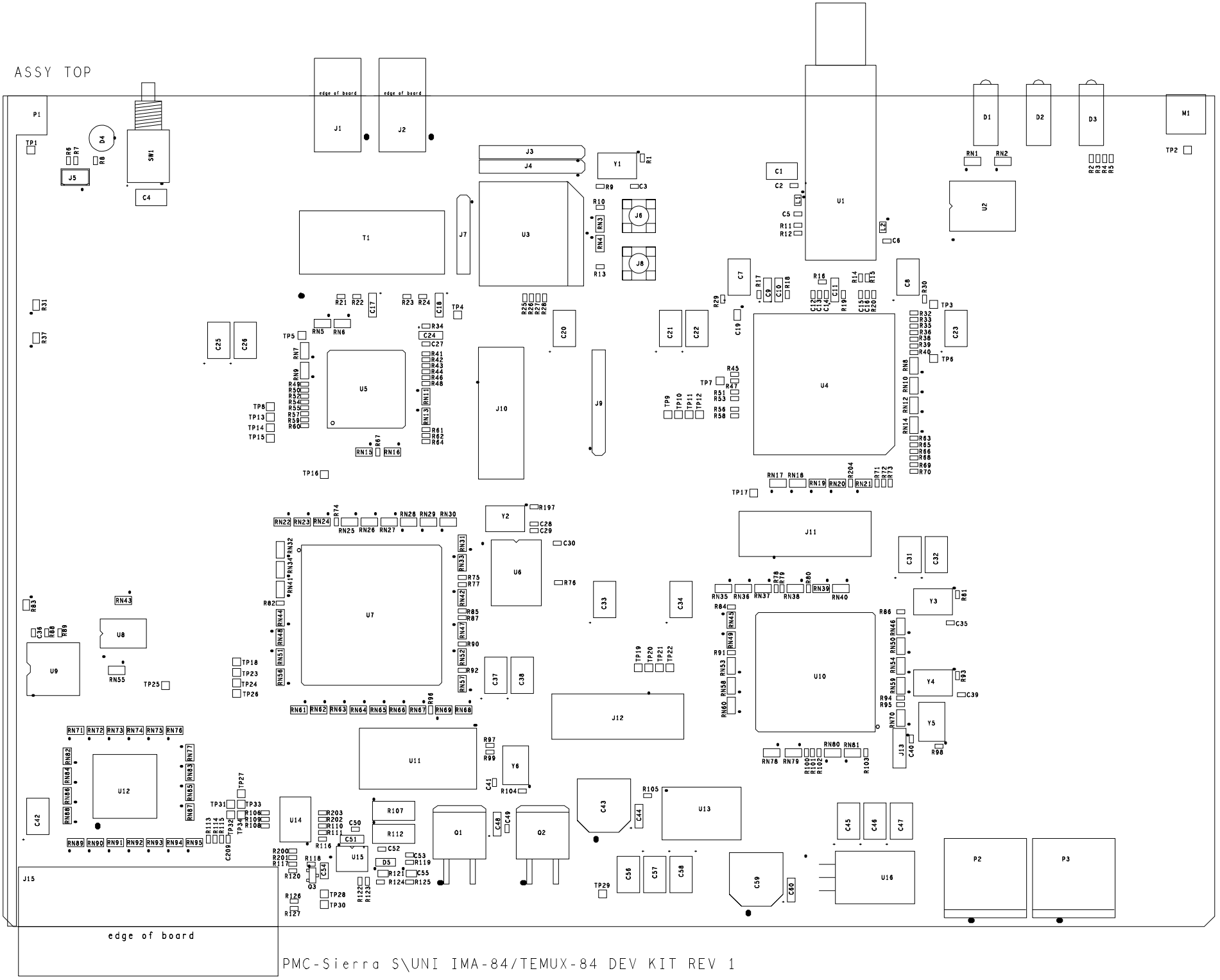
PMC-Sierra S\UNI IMA-84/TEMUX-84 DEV KIT REV 1

GND3_PLANE

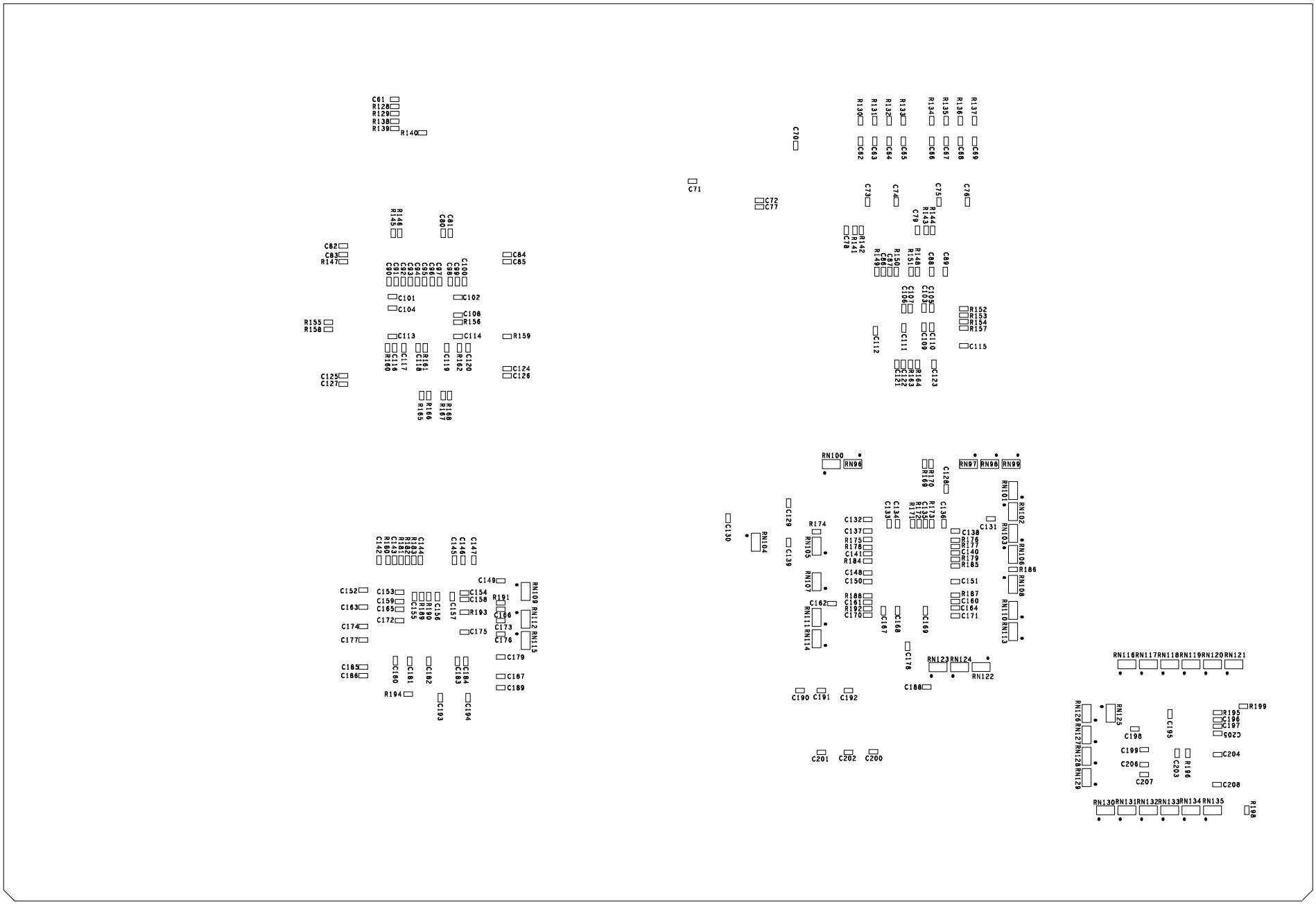


BOTTOM




ASSY TOP
edge of board
edge of board
edge of board
P1
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J15
P2
P3
M1
SW1
D1
D2
D3
D4
Y1
Y2
Y3
Y4
Y5
Y6
T1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
Q1
Q2
Q3
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
TP20
TP21
TP22
TP23
TP24
TP25
TP26
TP27
TP28
TP29
TP30
TP31
TP32
TP33
TP34
D5
edge of board
PMC-Sierra S\UNI IMA-84/TEMUX-84 DEV KIT REV 1

ASSY BOTTOM



PMC-Sierra S\UNI IMA-TEMUX-84 DEV KIT REV 1

```
library IEEE;
use IEEE.std_logic_1164.all;


entity myima is
   port (
      osc: in STD_LOGIC;
      dfp: out STD_LOGIC;
      lac1: out STD_LOGIC;
      ctclk: inout STD_LOGIC;
      lrefclk: out STD_LOGIC;
      refclk: out STD_LOGIC;
      srefclk: out STD_LOGIC;
      trclk: out STD_LOGIC;
      ack: out STD_LOGIC
   );
end myima;

architecture myima_arch of myima is
begin

        -- FRAME PULSE GENERATION
process (osc)
        variable COUNT_INT: integer range 0 to 10000;
begin
        if osc='0' and osc'event then
                if COUNT_INT=9719 then
                        LAC1 <='1';
                        DFP <='1';
                        COUNT_INT := 0;
                else
                        COUNT_INT := COUNT_INT+1;
                        LAC1 <='0';
                        DFP <='0';
                end if;
        end if;
end process;

-- PROCESS sync8k_gen: Generates the 8kHz signal for the SBI bus.
        -- The process divide 19.44M by 2430 (2430/2-1=1214)
process (osc)
        variable count2: integer range 0 to 5000;
begin
        --      count2 := 0;
        if osc'event and osc='1' then
                if count2=1214 then
                        ctclk <= not ctclk;                     -- 8k clock
                        count2 := 0;
                else
                        count2 := count2 + 1;
                end if;
        end if;
end process;

-- Clock generation
```

```
lrefclk <= osc;
srefclk <= osc;
refclk <= osc;
trclk <= osc;
ack <= osc;


end myima_arch;
```

NOTES

CONTACTING PMC-SIERRA, INC.

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Canada V5A 4V7

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Fax: (604) 415-6200

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Application Information: apps@pmc-sierra.com
Web Site: http://www.pmc-sierra.com

PMC-2002050 (p2) Issue date: June 2001