# FMS72510
## Phase Locked Loop Clock Driver

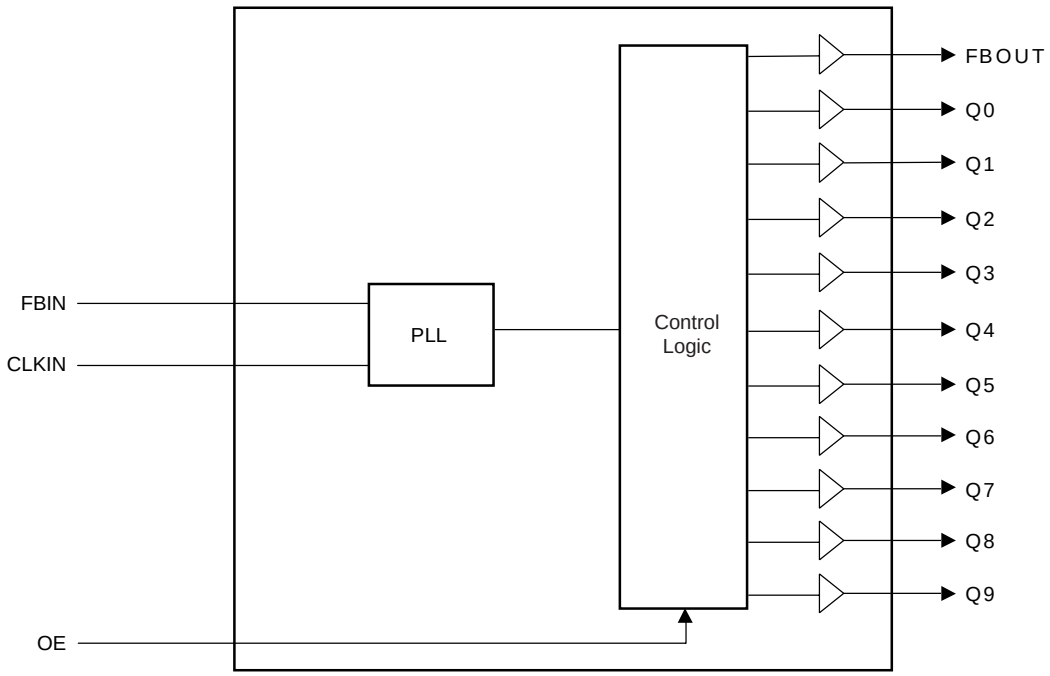
### Features

- PC-133 Spread Spectrum Compliant
- Frequency Range of 25 to 140 MHz
- $V_{DD}$ Range of 3.0 to 3.6 Volts
- Up to 11 outputs
- Less than 100 pS of Output to Output Skew
- Less than 90 pS of Cycle to Cycle Jitter
- Output Enable pin
- Integrated Damping Resistor
- Commercial Temperature Range
- Available in 24 pin TSSOP

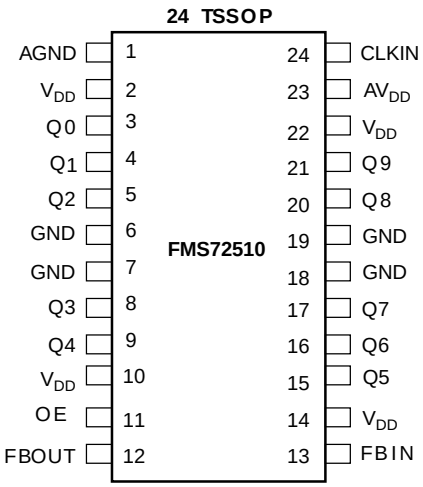
### Description

FMS72510 is a zero delay clock buffer designed for high fan out applications. It contains 11 outputs. It provides precise phase and frequency alignment between incoming clock and the output clocks. This makes it ideal for high speed application in the range of 25 to 140 MHz. The Phase Locked Loop is capable of tracking incoming clock modulation of up to ±1% of the clock period. With the exception of FBOUT, the output Enable (OE) pin, when pulled low, will force the outputs to logic low.

### Block Diagram



## Pin Assignments




## Pin Description

| Pin Name | Pin # | Pin Type | Pin Function Description |
|---|---|---|---|
| GND | 6, 7, 18, 19 | PWR | **Ground Connection:** Connect all ground pins to the common system ground plane. |
| AGND | 1 | PWR | **Analog Ground Connection:** Connect to common system ground plane. |
| $V_{DD}$ | 2, 10, 14, 22 | PWR | **Power Connection:** Power supply for all the outputs. |
| $AV_{DD}$ | 23 | PWR | **Power Connection:** Power supply for the PLL. When connected low, it shuts off and bypass's the PLL. |
| Q (0:9) | 3, 4, 5, 8, 9, 15, 16, 17, 20, 21 | OUT | **Clock outputs:** Outputs are buffer clocks of input. |
| OE | 11 | IN | **Outputs Enable:** When low, all outputs, with the exception of FBOUT, goes to logic low. Normal operation when asserted high. |
| FBOUT | 12 | OUT | **Feedback Clock Output:** Dedicated pin for FB pin. It is not effected by OE pin. |
| FBIN | 13 | IN | **Feedback Clock Input:** PLL feedback input. The user connects it to FBOUT. |
| CLKIN | 24 | IN | **Input Clock:** One of the inputs of the PLL. |

## Functionality Table

| AVDD | OE | PLL | Q (0:9) | FBOUT |
|---|---|---|---|---|
| L | L | BYPASS | L | Buffered CLKIN |
| L | H | BYPASS | Buffered Clocked | Buffered CLKIN |
| H | L | Enabled | L | Running in phase with CLKIN |
| H | H | Enabled | Running in phase with CLKIN | Running in phase with CLKIN |

## Absolute Maximum Rating

| Symbol | Parameter | Ratings | Units |
|---|---|---|---|
| $V_{DD}$, $V_{IN}$ | Voltage on any pin with respect to ground | –0.5 to 7.0 | V |
| $T_{STG}$ | Storage Temperature | –65 to 150 | °C |
| $T_B$ | Ambient Temperature | –55 to 125 | °C |
| $T_A$ | Operating Temperature | 0 to 70 | °C |

Stresses greater than those listed in the table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may effect reliability.

## DC Electrical Characteristics

$T_A$ = 0 to 70°C; Supply Voltage $V_{DD}$ = 3.3 V ±0.3V, $C_L$ = 12pF (unless otherwise stated)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | | GND – 0.3 | | 0.8 | V |
| Input High Voltage | $V_{IH}$ | | 2.0 | | $V_{DD}$ + 0.3 | V |
| Input Low Current | $I_{IL}$ | $V_{IN}$ = 0 | -10 | | 10 | µA |
| Input High Current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | -10 | | 10 | µA |
| High Output Voltage | $V_{OH}$ | $I_{OH}$ = -6mA | 2.4 | 3.1 | | V |
| Low Output Voltage | $V_{OL}$ | $I_{OL}$ = 15mA | | 0.5 | 0.8 | V |
| Input Capacitance(1) | $C_{IN}$ | Frequency = 10MHz | 2.5 | | 6.0 | pF |
| Supply Current | $I_{DD}$ | Frequency = 100 MHz; $C_L$ = 12pF | | 200 | 290 | mA |
| | | Frequency = 133 MHz; $C_L$ = 12pF | | 230 | 320 | mA |
| Clock Stabilization(1) | $T_{STAB}$ | From $V_{DD}$ = 3.3 V to 1% Target | | | 1 | mS |

**NOTE:**

1. Guaranteed by design, not subject to 100% production testing.

## AC Electrical Characteristics

$T_A$ = 0 to 70°C; Supply Voltage $V_{DD}$ = 3.3V ±0.3V, $C_L$ = 12 pF (unless otherwise stated)

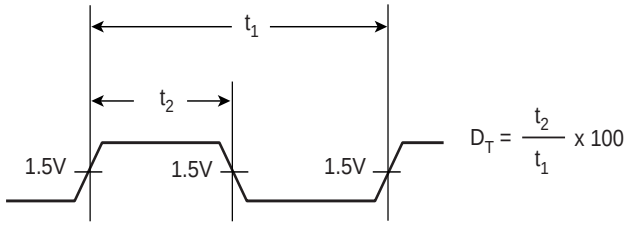
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Clock Input Duty Cycle(1) | $D_{T\_IN}$ | AVDD = 3.3V | 40 | | 60 | % |
| Input Frequency Range(1) | $F_{IN}$ | | 25 | | 140 | MHz |
| Rise Time(1) | $T_R$ | 0.4 to 2.0V | – | | 2.0 | nS |
| Fall Time(1) | $T_F$ | 2.0 to 0.4V | – | | 2.0 | nS |
| Duty Cycle(1) | $D_T$ | $V_{TH}$ = 1.25V | 45 | | 55 | % |
| Jitter (Cycle-Cycle)(1) | $T_{JIT}$ | $V_{TH}$ = 1.25V; 100 & 133 MHz | -120 | | 120 | pS |
| Spread Spectrum Induced Skew(1) | $T_{SK\_SSC}$ | $V_{TH}$ = $V_{DD}$/2 | -200 | | 200 | pS |
| Output to Output Skew(1) | $T_{SK1}$ | $V_{TH}$ = $V_{DD}$/2 | -120 | | 120 | pS |
| Input to Output Delay(1,2) | $T_{SK2}$ | $C_{LFB}$ = 4 pF; 100 & 133 MHz | -100 | | 100 | pS |

**NOTE:**

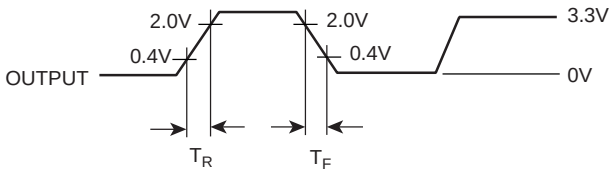
1. Guaranteed by design, not subject to 100% production testing.
2. Feedback trace length of 0.7”.

# Parameter Measurement Information

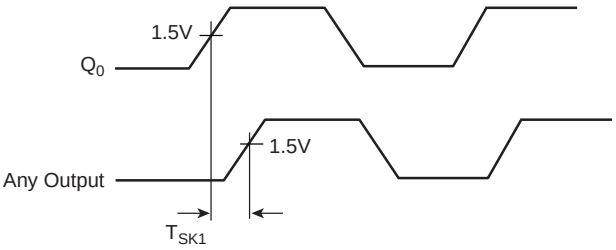
## Duty Cycle Timing ($D_T$)



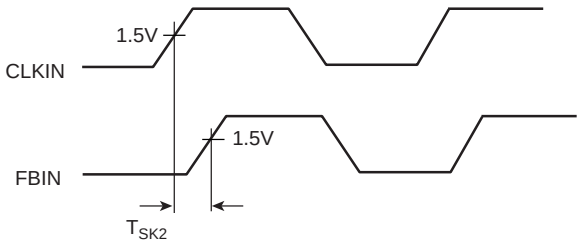

## Rise/Fall Time ($T_R/T_F$)



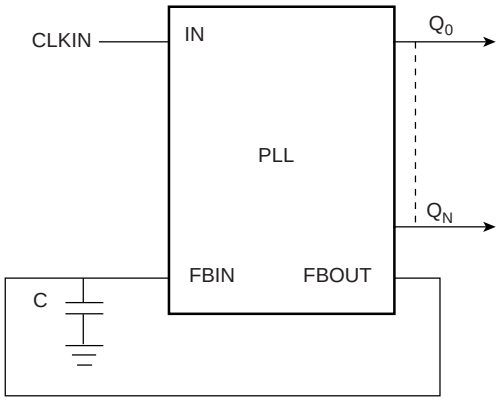

## Output to Output Skew ($T_{SK1}$)




## Input to Output Delay ($T_{SK2}$)



# Application Diagram




**Note:** Feedback capacitor value 'C' is to be determined based on the phase characteristics of the PLL.

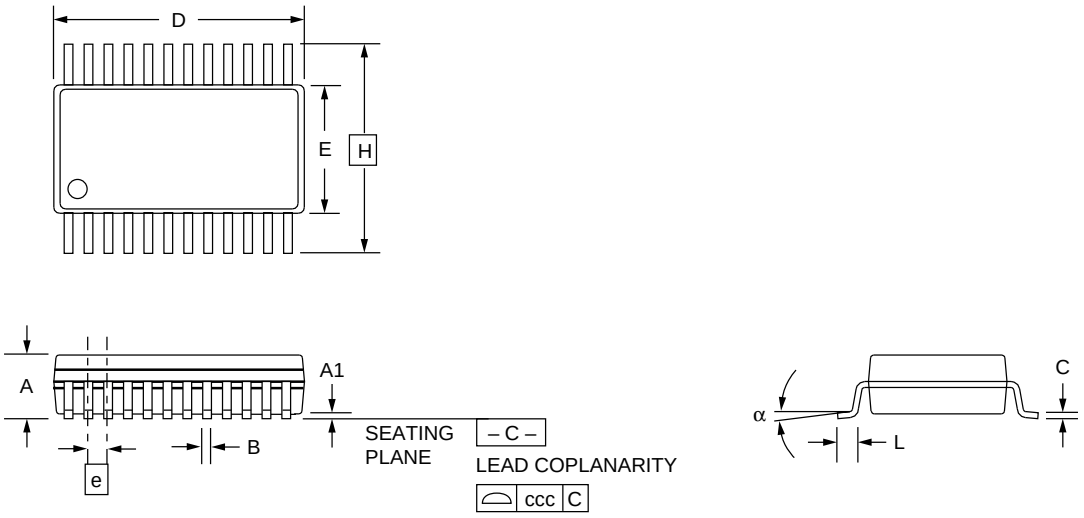
# Mechanical Dimensions

## 24-Lead TSSOP Package

| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | — | .047 | — | 1.20 | |
| A1 | .002 | .006 | 0.05 | 0.15 | |
| B | .007 | .012 | 0.19 | 0.30 | |
| C | .004 | .008 | 0.09 | 0.20 | |
| D | .308 | .316 | 7.70 | 7.90 | 2 |
| E | .172 | .180 | 4.30 | 4.50 | 2 |
| e | .026 BSC | | 0.65 BSC | | |
| H | .256 BSC | | 6.40 BSC | | |
| L | .018 | .030 | 0.45 | 0.75 | 3 |
| N | 24 | | 24 | | 5 |
| α | 0° | 8° | 0° | 8° | |
| ccc | — | .004 | — | 0.10 | |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .006 inch (0.15mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. Symbol "N" is the maximum number of terminals.



## Ordering Information

| Product Number | Tape & Reel | Package |
|---|---|---|
| FMS72510MTC | FMS72510MTCT | TSSOP-24 |