# PRELIMINARY

Integrated Circuit Systems, Inc.

# ICS843002I-01

## FemtoClocks™ Crystal-to-3.3V, 2.5V LVPECL Frequency Synthesizer

## General Description

The ICS843002I-01 is a 2 output LVPECL synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL[1:0]): 156.25MHz, 125MHz, and 62.5MHz. The ICS843002I-01 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS843002I-01 is packaged in a small 20-pin TSSOP package.

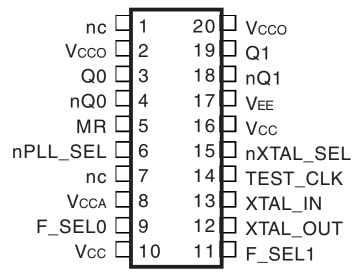
## Features

- Two 3.3V or 2.5V LVPECL outputs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Supports the following input frequencies: 156.25MHz, 125MHz and 62.5MHz
- VCO range: 560MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz-20MHz): 0.55ps (typical) design target
- Output skew: 10ps (typical)
- Supply Voltage Modes
  Core/Outputs
  3.3/3.3
  2.5/2.5
- -40°C to 85°C ambient operating temperature

### Frequency Select Function Table

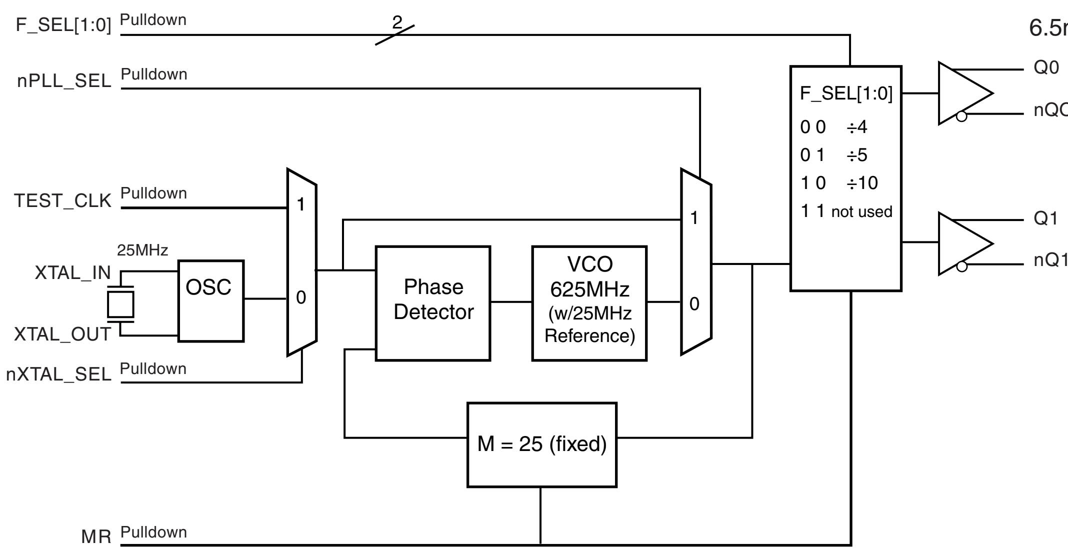
| Inputs | | | | Output Frequency (25MHz Ref.) |
|---|---|---|---|---|
| F_SEL1 | F_SEL0 | M Divider Value | N Divider Value | |
| 0 | 0 | 25 | 4 | 156.25 |
| 0 | 1 | 25 | 5 | 125 |
| 1 | 0 | 25 | 10 | 62.5 |
| 1 | 1 | Not Used | | Not Used |

## Pin Assignment




**ICS843002I-01**
**20-Lead TSSOP**
6.5mm x 4.4mm x 0.92mm package body
**G Package**
Top View

## Block Diagram




The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 7 | nc | Unused | | No connect. |
| 2, 20 | $V_{CCO}$ | Power | | Output supply pins. |
| 3, 4 | Q0, nQ0 | Ouput | | Differential output pair. LVPECL interface levels. |
| 5 | MR | Input | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 6 | nPLL_SEL | Input | Pulldown | Selects between the PLL and TEST_CLK as input to the dividers. When LOW, selects PLL (PLL Enable). When HIGH, deselects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels. |
| 8 | $V_{CCA}$ | Power | | Analog supply pin. |
| 9, 11 | F_SEL0, F_SEL1 | Input | Pulldown | Frequency select pins. LVCMOS/LVTTL interface levels. |
| 10, 16 | $V_{CC}$ | Power | | Core supply pin. |
| 12, 13 | XTAL_OUT, XTAL_IN | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. |
| 14 | TEST_CLK | Input | Pulldown | LVCMOS/LVTTL clock input. |
| 15 | nXTAL_SEL | Input | Pulldown | Selects between crystal or TEST_CLK inputs as the the PLL Reference source. Selects XTAL inputs when LOW. Selects TEST_CLK when HIGH. LVCMOS/LVTTL interface levels. |
| 17 | $V_{EE}$ | Power | | Negative supply pins. |
| 18, 19 | nQ1, Q1 | Output | | Differential output pair. LVPECL interface levels. |
| 2, 20 | $V_{CCO}$ | Power | | Output supply pins. |

NOTE: *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$ | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| $V_{CCO}$ | Output Supply Voltage | | 2.97 | 3.3 | 3.63 | V |
| $I_{EE}$ | Power Supply Current | | | 115 | | mA |
| $I_{CC}$ | Core Supply Current | | | 80 | | mA |
| $I_{CCA}$ | Analog Supply Current | | | 12 | | mA |
| $I_{CCO}$ | Output Supply Current | | | 25 | | mA |

**TABLE 3B. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 2.375 | 2.5 | 3.625 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 2.375 | 2.5 | 3.625 | V |
| $V_{CCO}$ | Output Supply Voltage | | 2.375 | 2.5 | 3.625 | V |
| $I_{EE}$ | Power Supply Current | | | 110 | | mA |
| $I_{CC}$ | Core Supply Current | | | 75 | | mA |
| $I_{CCA}$ | Analog Supply Current | | | 12 | | mA |
| $I_{CCO}$ | Output Supply Current | | | 25 | | mA |

**TABLE 3C. LVCMOS / LVTTL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10% OR 2.5V±5%, TA = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | TEST_CLK, MR, nPLL_SEL, nXTAL_SEL | $V_{CC} = V_{IN}$ = 3.63V | | | 150 | µA |
| $I_{IL}$ | Input Low Current | TEST_CLK, MR, nPLL_SEL, nXTAL_SEL | $V_{CC}$ = 3.63V, $V_{IN}$ = 0V | -5 | | | µA |

**TABLE 3D. LVPECL DC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10% OR 2.5V±10%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CCO}$ - 1.4 | | $V_{CCO}$ - 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CCO}$ - 2.0 | | $V_{CCO}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO}$ - 2V.

**TABLE 4. CRYSTAL CHARACTERISTICS**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 22.4 | 25 | 27.2 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

NOTE: Characterized using an 18pF parallel resonant crystal.

**TABLE 5A. AC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 3.3V±10%, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | F_SEL[1,:0] = 00 | 140 | | 170 | MHz |
| | | F_SEL[1,:0] = 01 | 112 | | 136 | MHz |
| | | F_SEL[1,:0] = 10 | 56 | | 68 | MHz |
| *t*sk(o) | Output Skew; NOTE 1, 2 | | | 10 | | ps |
| *t*jit(Ø) | RMS Phase Jitter; NOTE 2, 3 | 156.25MHz, (1.875MHz - 20MHz) | | 0.55 | | ps |
| | | 125MHz, (1.875MHz - 20MHz) | | 0.6 | | ps |
| | | 62.5MHz, (1.875MHz - 20MHz) | | 0.7 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | | 450 | | ps |
| odc | Output Duty Cycle | | | 50 | | % |

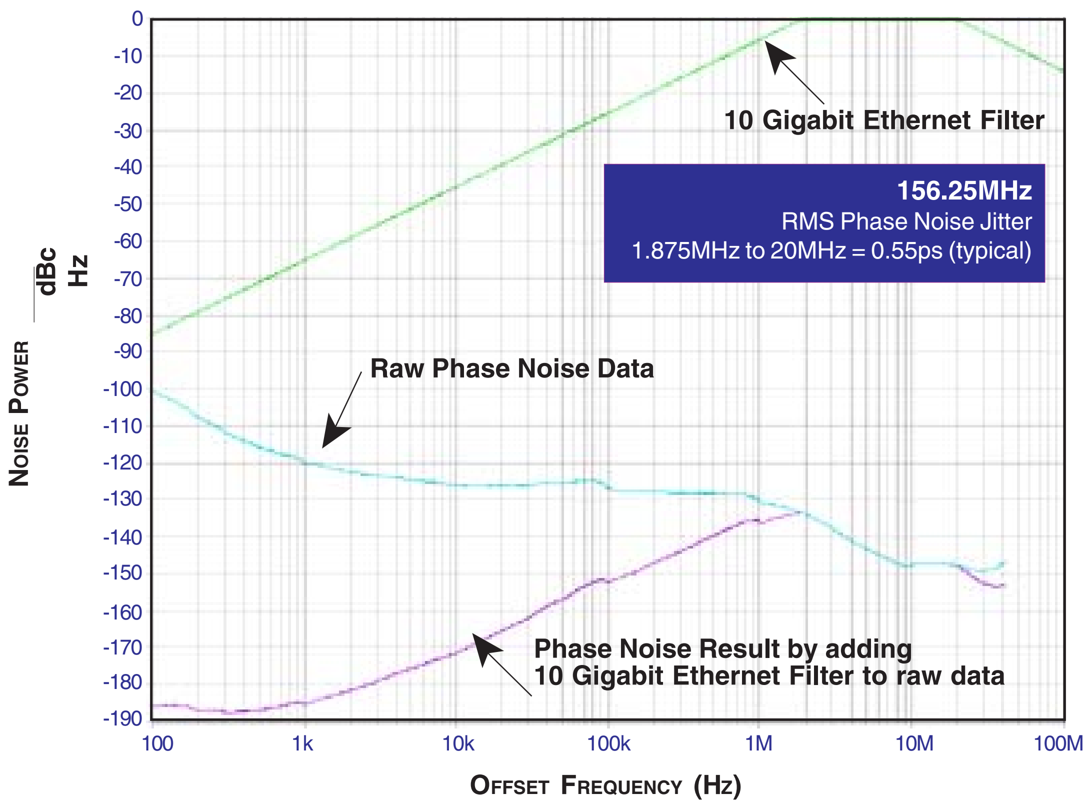
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{CCO}$/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Phase jitter is dependent on the input source used.

**TABLE 5B. AC CHARACTERISTICS,** $V_{CC} = V_{CCA} = V_{CCO}$ = 2.5V±5%, TA = -40°C TO 85°C

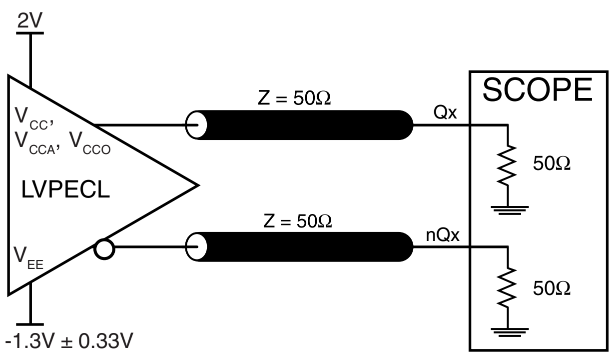
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | F_SEL[1,:0] = 00 | 140 | | 170 | MHz |
| | | F_SEL[1,:0] = 01 | 112 | | 136 | MHz |
| | | F_SEL[1,:0] = 10 | 56 | | 68 | MHz |
| *t*sk(o) | Output Skew; NOTE 1, 2 | | | TBD | | ps |
| *t*jit(Ø) | RMS Phase Jitter; NOTE 2, 3 | 156.25MHz, (1.875MHz - 20MHz) | | 0.55 | | ps |
| | | 125MHz, (1.875MHz - 20MHz) | | 0.6 | | ps |
| | | 62.5MHz, (1.875MHz - 20MHz) | | 0.74 | | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | | 470 | | ps |
| odc | Output Duty Cycle | | | 50 | | % |

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{CCO}$/2.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Phase jitter is dependent on the input source used.

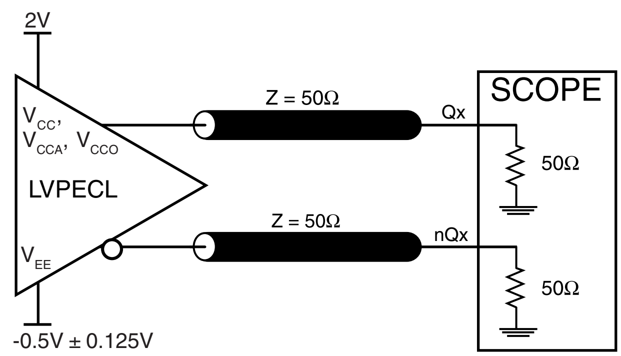
## TYPICAL PHASE NOISE AT 156.25MHZ



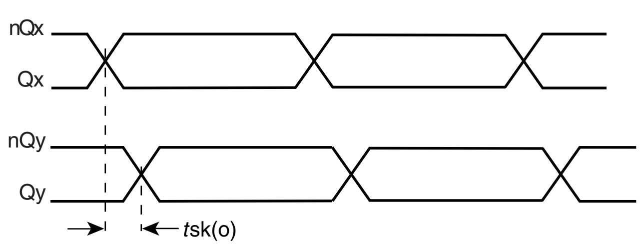
# PARAMETER MEASUREMENT INFORMATION



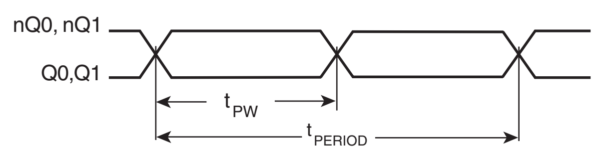

3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT




2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT

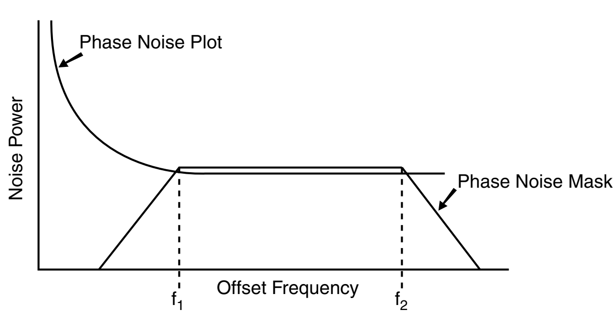



OUTPUT SKEW



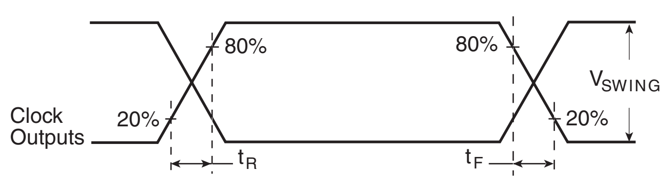

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD




$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

RMS PHASE JITTER




OUTPUT RISE/FALL TIME

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843002I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$, $V_{CCA}$, and $V_{CCO}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{CCA}$.

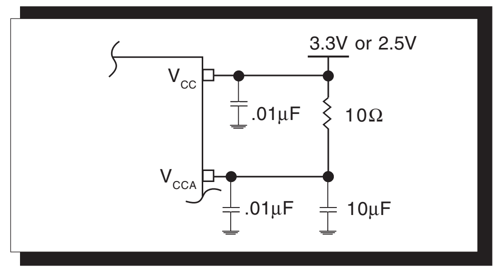



FIGURE 1. POWER SUPPLY FILTERING

## TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

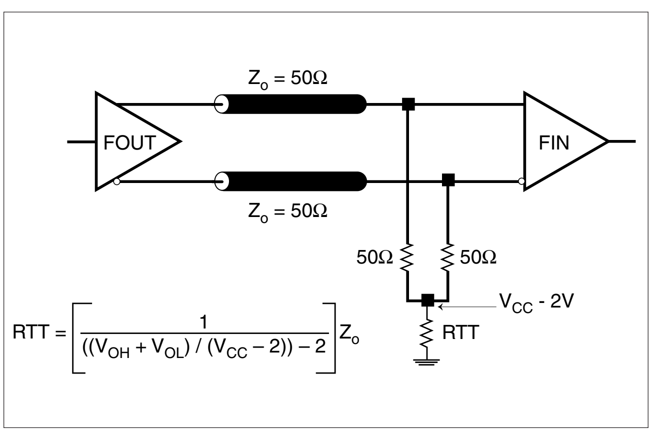



FIGURE 2A. LVPECL OUTPUT TERMINATION

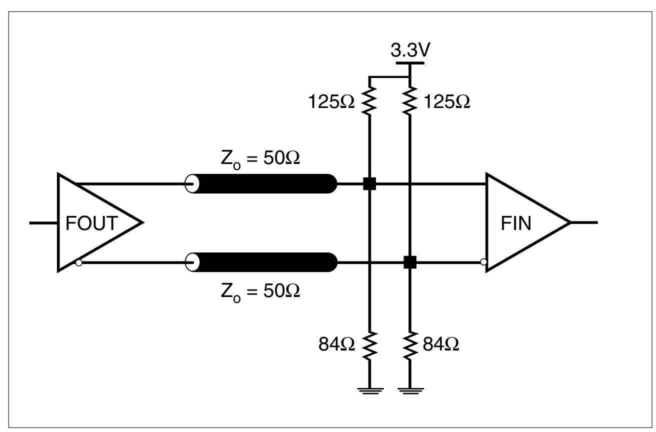



FIGURE 2B. LVPECL OUTPUT TERMINATION

## TERMINATION FOR 2.5V LVPECL OUTPUT

*Figure 3A* and *Figure 3B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC}$ - 2V. For $V_{CCO}$ = 2.5V, the $V_{CCO}$ - 2V is very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in *Figure 3C.*

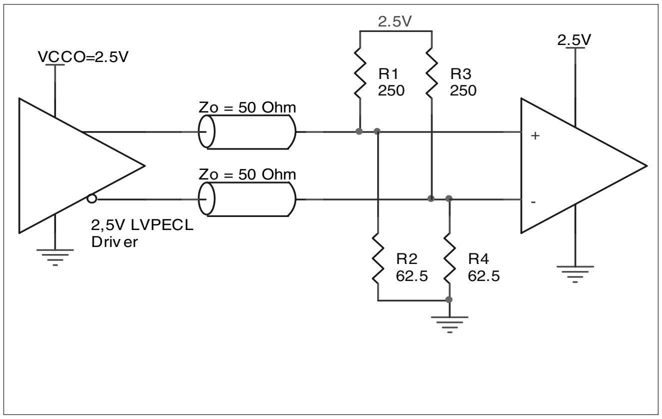



FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

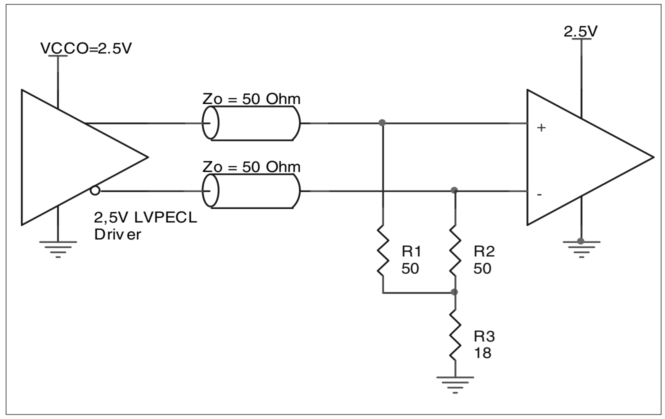



FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

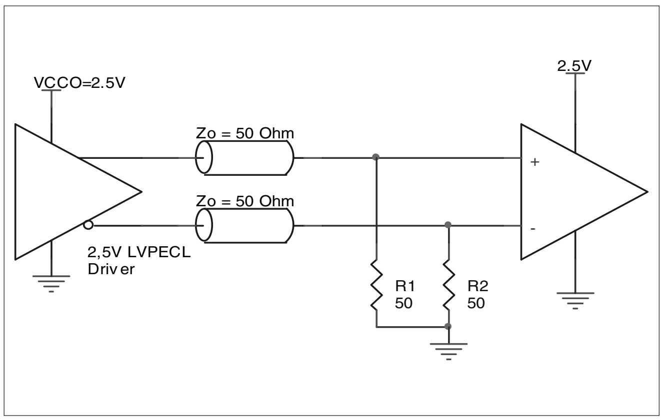



FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

## CRYSTAL INPUT INTERFACE

The ICS843002I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 4* below were determined using a 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

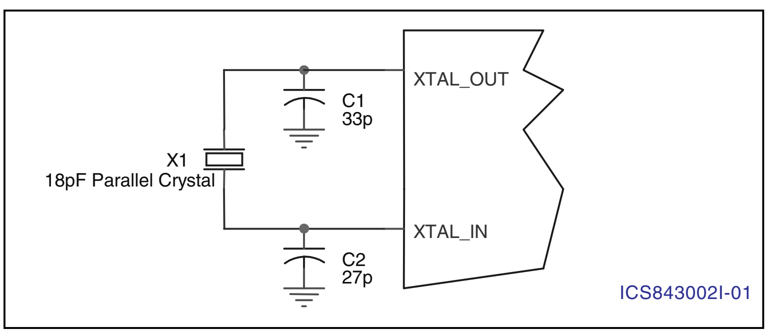



**Figure 4.** CRYSTAL INPUT INTERFACE

## LAYOUT GUIDELINE

*Figure 5A* shows a schematic example of the ICS843002I-01. An example of LVEPCL termination is shown in this schematic. Additional LVPECL termination approaches are shown in the LVPECL Termination Application Note. In this example, an 18 pF parallel resonant 26.5625MHz crystal is used. The C1=27pF and C2=33pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy.

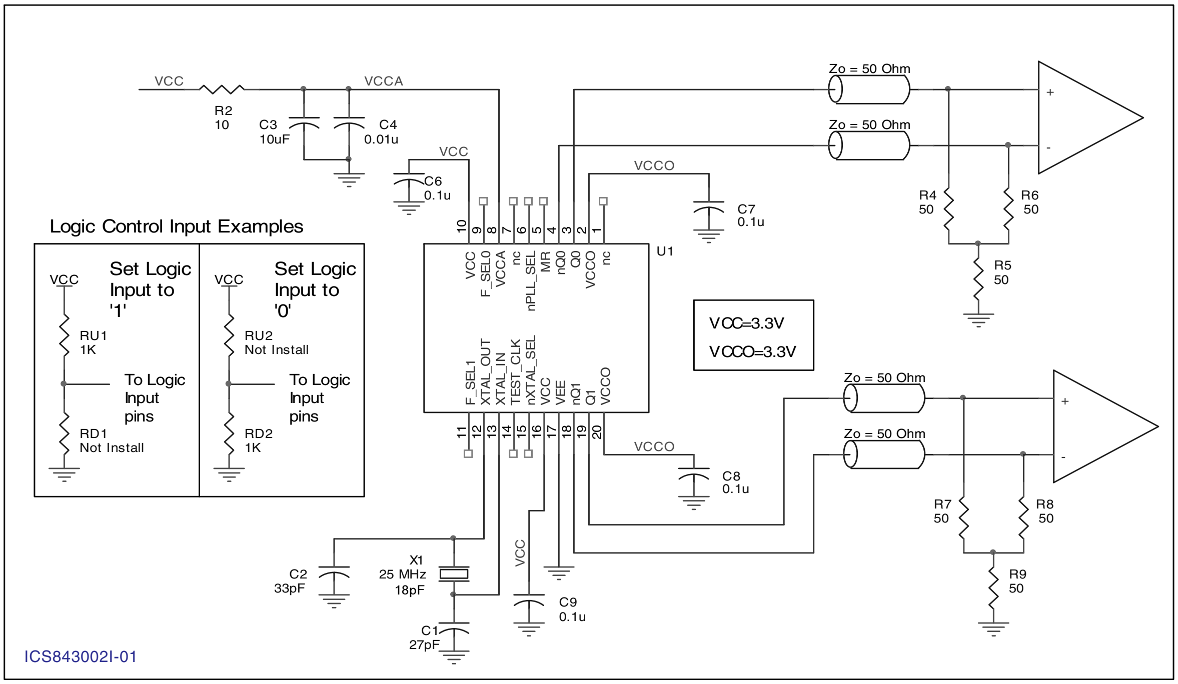



FIGURE 5A. ICS843002I-01 SCHEMATIC EXAMPLE

## PC BOARD LAYOUT EXAMPLE

*Figure 5B* shows an example of ICS843002I-01 P.C. board layout. The crystal X1 footprint shown in this example allows installation of either surface mount HC49S or through-hole HC49 package. The footprints of other components in this example are listed in the *Table 6.* There should be at least one decoupling capacitor per power pin. The decoupling capacitors should be located as close as possible to the power pins. The layout assumes that the board has clean analog power ground plane.

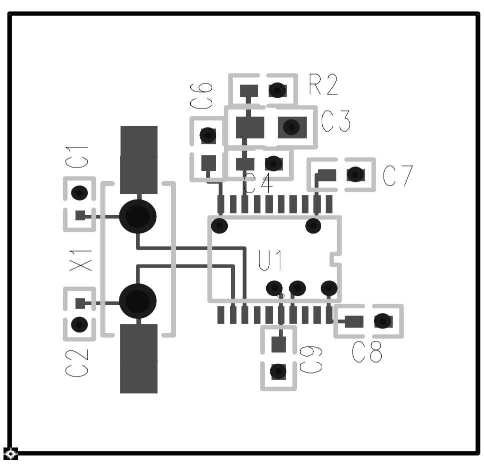



FIGURE 5B. ICS843002I-01 PC BOARD LAYOUT EXAMPLE

TABLE 6. FOOTPRINT TABLE

| Reference | Size |
|---|---|
| C1, C2 | 0402 |
| C3 | 0805 |
| C4, C5, C6, C7, C8 | 0603 |
| R2 | 0603 |

NOTE: Table 6, lists component sizes shown in this layout example.

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843002I-01. Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the ICS843002I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC}$ = 3.3V + 10% = 3.63V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.63V * 115mA = **417.45mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30mW = **60mW**

**Total Power**$_{\_MAX}$ (3.63V, with all outputs switching) = 417.5mW + 60mW = **477.5mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.478W * 66.6°C/W = 116.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 7. THERMAL RESISTANCE $\theta_{JA}$ FOR 20-PIN TSSOP, FORCED CONVECTION**

**$\theta_{JA}$ by Velocity (Linear Feet per Minute)**

| | **0** | **200** | **500** |
|---|---|---|---|
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

*3. Calculations and Equations.*

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

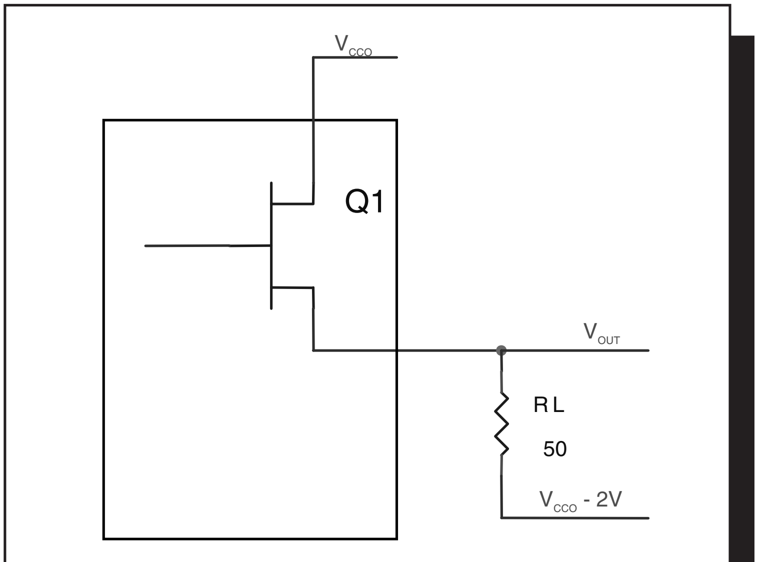



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO}$ - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

# RELIABILITY INFORMATION

TABLE 8. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

**$\theta_{JA}$ by Velocity (Linear Feet per Minute)**

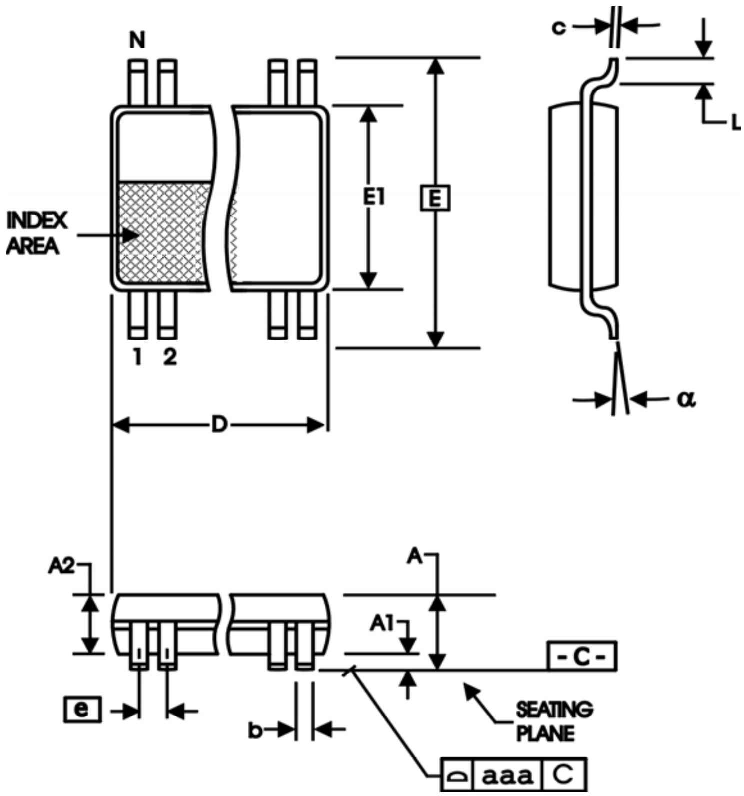
| | **0** | **200** | **500** |
|---|---|---|---|
| Single-Layer PCB, JEDEC Standard Test Boards | 114.5°C/W | 98.0°C/W | 88.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## TRANSISTOR COUNT

The transistor count for ICS843002I-01 is: 2955

### PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP




### TABLE 9. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|---|---|---|
| | MIN | MAX |
| N | 20 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 10. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|---|---|---|---|---|
| ICS843002AGI-01 | ICS43002AI01 | 20 Lead TSSOP | tube | -40°C to 85°C |
| ICS843002AGI-01T | ICS43002AI01 | 20 Lead TSSOP | 2500 tape & reel | -40°C to 85°C |