



GENERAL DESCRIPTION

The M2004-02 and its variants are VCISO (Voltage Controlled SAW Oscillator) based clock generator PLLs designed for clock frequency translation and jitter attenuation in a high-speed data communications system. The clock multiplication ratio and output divider ratio are pin selectable. External loop components allow the tailoring of PLL loop response. Variants of the device add the features Hitless Switching with Phase Build-out (HS/PBO) to ensure that reference clock reselection does not disrupt the output clock. A fixed Narrow Loop Bandwidth feature (Fixed NBW) is included in the some of the device variants.

FEATURES

- Ideal for OC-48/192 data clock
- Integrated SAW (surface acoustic wave) delay line
- VCISO frequency from 300 to 700MHz **
- Low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)
- Pin-selectable configuration
- Hitless Switching with Phase Build-out (HS/PBO) added to all but the M2004-02 to ensure SONET/SDH MTIE and TDEV compliance during reference clock reselection
- Fixed Narrow Loop Bandwidth feature (Fixed NBW) added to some of the product variants (see Table 2)
- Reference clock inputs support differential LVDS, LVPECL, as well as single-ended LVCMOS, LVTTTL
- Industrial temperature available
- Single 3.3V power supply
- Small 9 x 9 mm SMT (surface mount) package

PIN ASSIGNMENT (9 x 9 mm SMT)

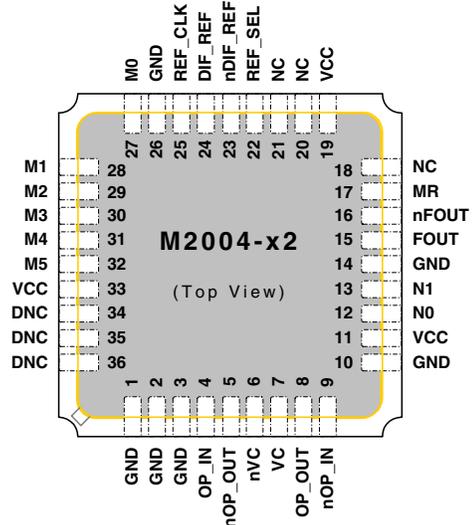


Figure 1: Pin Assignment

Example Input / Output Frequency Combinations

Input (MHz)	VCISO ** (MHz)	Output (MHz)	Application
19.44	622.08	77.76	OC-12 / 48 / 192
77.76		311.04	
155.52		622.08	

Table 1: Example Input / Output Frequency Combinations

Device Variants and Corresponding Functions

Variant	Hitless Switching / Phase Build-out Triggered by		Fixed NBW
	Phase Transient	Mux Reselection	
M2004-02	no	no	no
M2004-12	✓ Yes	✓ Yes	no
M2004-22	no	no	✓ Yes
M2004-32	✓ Yes	✓ Yes	✓ Yes
M2004-42	no	✓ Yes	no
M2004-52	no	✓ Yes	✓ Yes

Table 2: Device Variants and Corresponding Functions

* Series of parts numbered M2004-02, -12, -22, -32, -42, and -52.

** Specify VCISO center frequency at time of order.

SIMPLIFIED BLOCK DIAGRAM

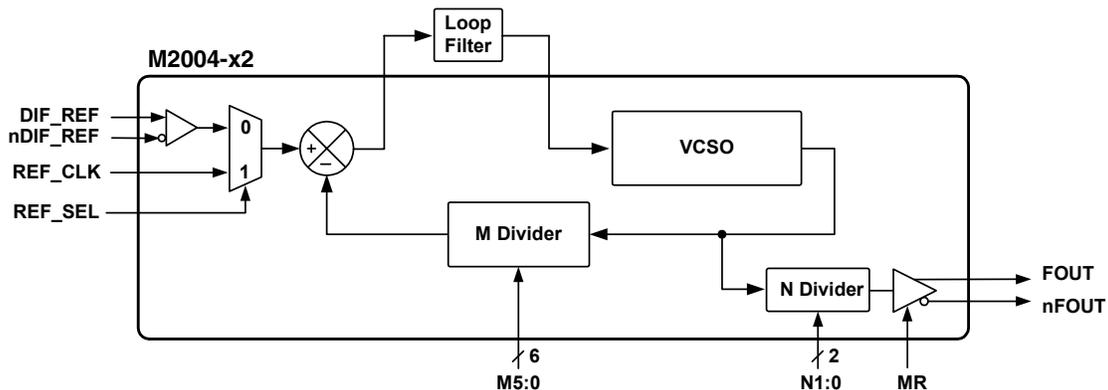


Figure 2: Simplified Block Diagram