

**TC74HC259AP, TC74HC259AF, TC74HC259AFN**

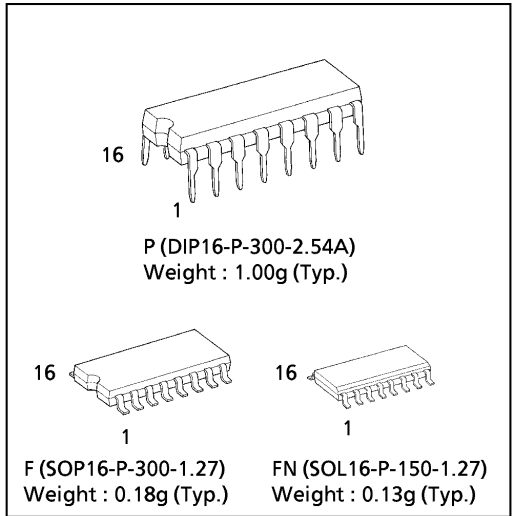
**8-BIT ADDRESSABLE LATCH**

The TC74HC259A is a high speed CMOS ADDRESSABLE LATCH fabricated with silicon gate C<sup>2</sup>MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The respective bits are controlled by address inputs A, B, and C. When CLEAR input is held high and enable input G is held low, the data is written into the bit selected by address inputs, the other bits hold their previous conditions. When both CLEAR and G held high, writing of all bits is inhibited regardless of address inputs, and their previous condition are held. When CLEAR is held low and G is held high, all bits are reset to low regardless of the other inputs. When both of CLEAR and G held low, all bits which aren't selected by address inputs are reset to low. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

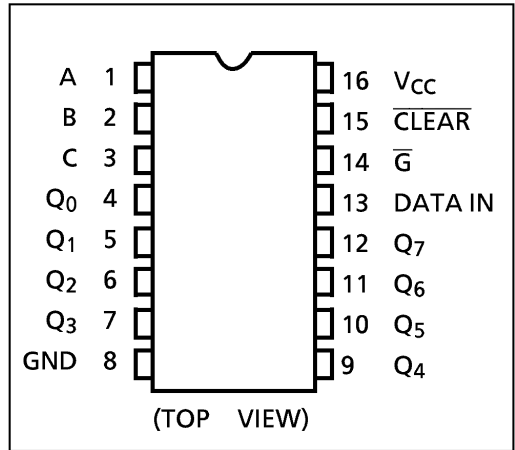
**FEATURES :**

- High Speed..... $t_{pd} = 15\text{ns}(\text{typ.})$  at  $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range...  $V_{CC} (\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS259

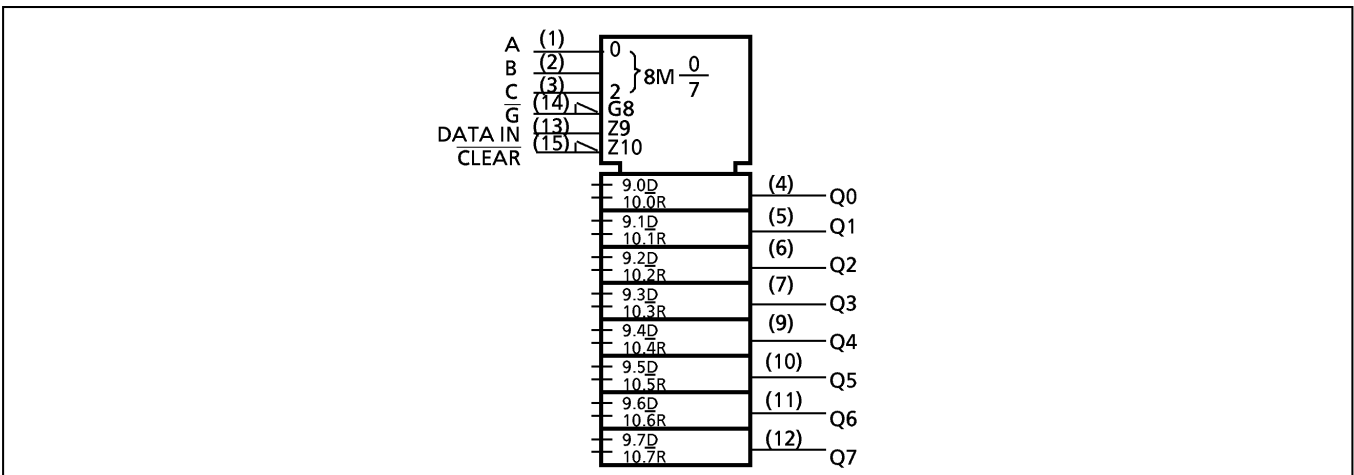
(Note) The JEDEC SOP (FN) is not available in Japan.



**PIN ASSIGNMENT**



**IEC LOGIC SYMBOL**



980508EBA2

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**TRUTH TABLE**

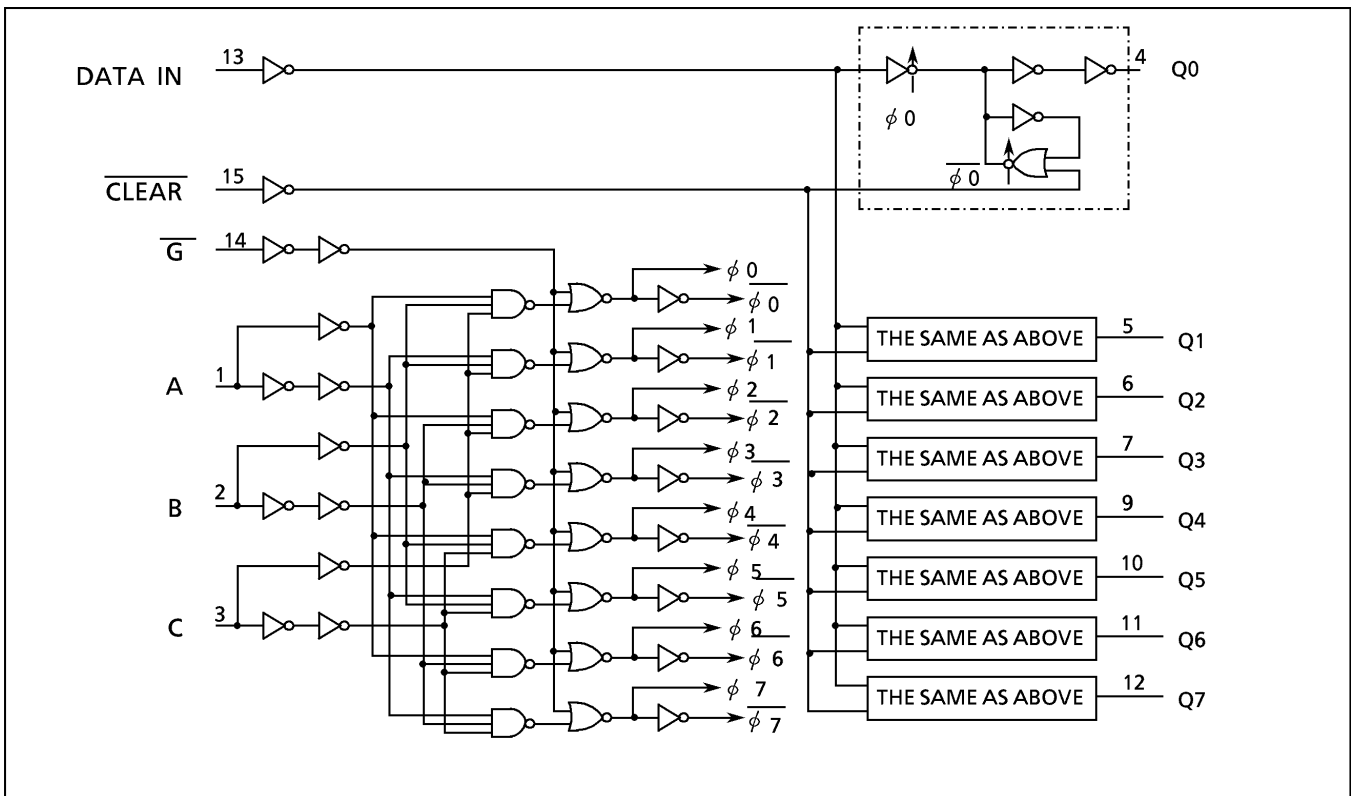
INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLEAR	$\overline{G}$			
H	L	D	Q <sub>i</sub> O	ADDRESSABLE LATCH MEMORY
H	H	Q <sub>i</sub> O	Q <sub>i</sub> O	8-LINE DEMULTIPLEXER
L	L	D	L	CLEAR ALL BITS TO "L"
L	H	L	L	

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D : The level at the data input.  
 O<sub>i</sub>O : The level before the indicated steady-state input conditions were established (i = 0, 1, ...7)

**SYSTEM DIAGRAM**



980508EBA2'

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## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	±20	mA
Output Diode Current	$I_{OK}$	±20	mA
DC Output Current	$I_{OUT}$	±25	mA
DC $V_{CC}$ / Ground Current	$I_{CC}$	±50	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  should be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2~6	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0\text{V}$ ) 0~500 ( $V_{CC} = 4.5\text{V}$ ) 0~400 ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	$V_{IH}$		2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low - Level Input Voltage	$V_{IL}$		2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			$I_{OH} = -4\text{mA}$ $I_{OH} = -5.2\text{mA}$	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			$I_{OL} = 4\text{mA}$ $I_{OL} = 5.2\text{mA}$	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	±0.1	—	±1.0	$\mu\text{A}$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0		

TIMING REQUIREMENTS (Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C	UNIT
			V <sub>CC</sub> (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width ( $\bar{G}$ )	$t_{W(L)}$		2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width ( $\overline{\text{CLEAR}}$ )	$t_{W(L)}$		2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (DATA)	$t_s$		2.0	—	50	60	
			4.5	—	10	12	
			6.0	—	9	11	
Minimum Set-up Time (A, B, C)	$t_s$		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	
Minimum Set-up Time (DATA)	$t_h$		2.0	—	25	30	
			4.5	—	5	6	
			6.0	—	5	5	
Minimum Hold Time (A, B, C)	$t_h$		2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	

AC ELECTRICAL CHARACTERISTICS ( $C_L = 15\text{pF}$ ,  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	$t_{TLH}$		—	4	8	ns
	$t_{THL}$					
Propagation Delay Time (DATA-Q)	$t_{pLH}$		—	15	22	
	$t_{pHL}$					
Propagation Delay Time (A, B, C-Q)	$t_{pLH}$		—	21	32	
	$t_{pHL}$					
Propagation Delay Time ( $\bar{G}$ -Q)	$t_{pLH}$		—	16	28	
	$t_{pHL}$					
Propagation Delay Time ( $\overline{\text{CLEAR}}$ -Q)	$t_{pHL}$		—	13	23	

AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.	
Output Transition Time	$t_{TLH}$ $t_{THL}$		2.0	—	30	75	—	95
			4.5	—	8	15	—	19
			6.0	—	7	13	—	16
Propagation Delay Time (DATA—Q)	$t_{pLH}$ $t_{pHL}$		2.0	—	56	130	—	165
			4.5	—	18	26	—	33
			6.0	—	15	22	—	28
Propagation Delay Time (A, B, C—Q)	$t_{pLH}$ $t_{pHL}$		2.0	—	83	185	—	230
			4.5	—	25	37	—	46
			6.0	—	21	31	—	39
Propagation Delay Time ( $\overline{G}$ —Q)	$t_{pLH}$ $t_{pHL}$		2.0	—	67	165	—	205
			4.5	—	20	33	—	41
			6.0	—	17	28	—	35
Propagation Delay Time ( $\overline{\text{CLEAR}}$ —Q)	$t_{pHL}$		2.0	—	52	135	—	170
			4.5	—	16	27	—	34
			6.0	—	14	23	—	29
Input Capacitance	C <sub>IN</sub>		—	5	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub> (1)		—	35	—	—	—	

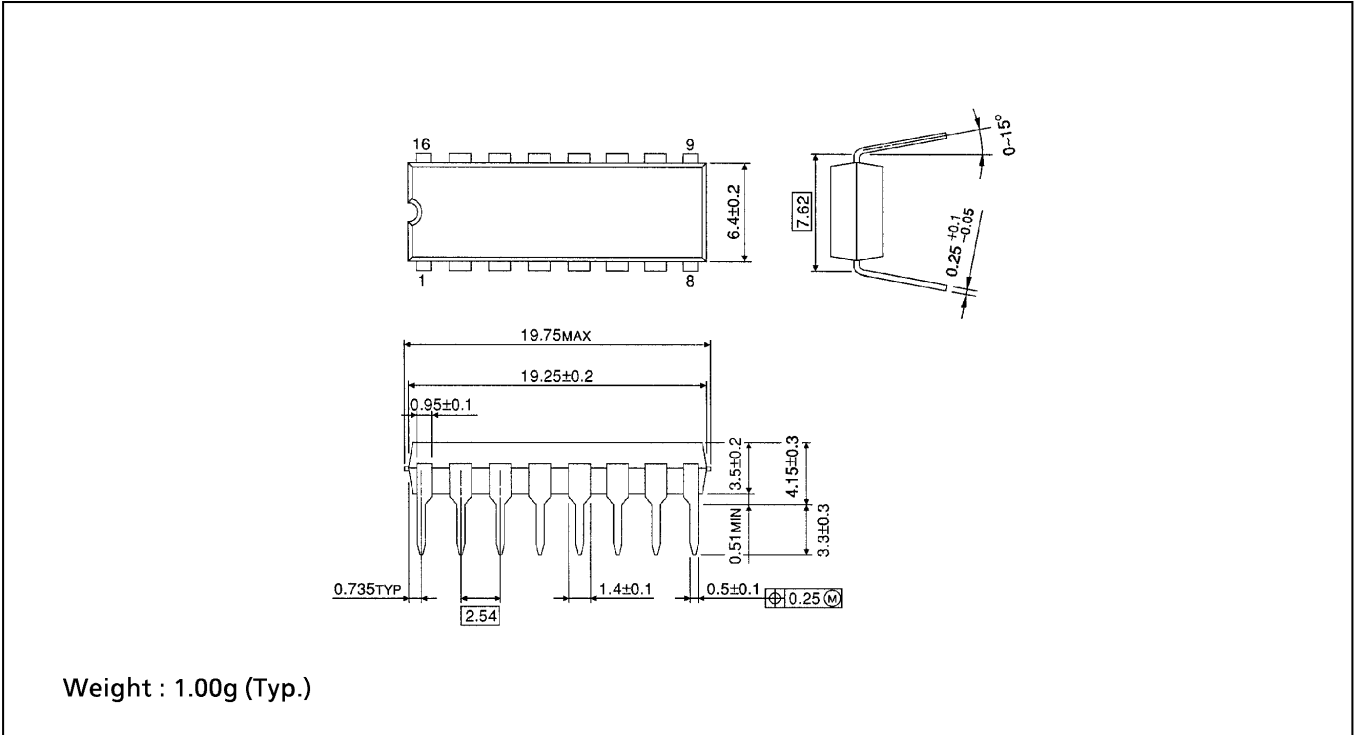
Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

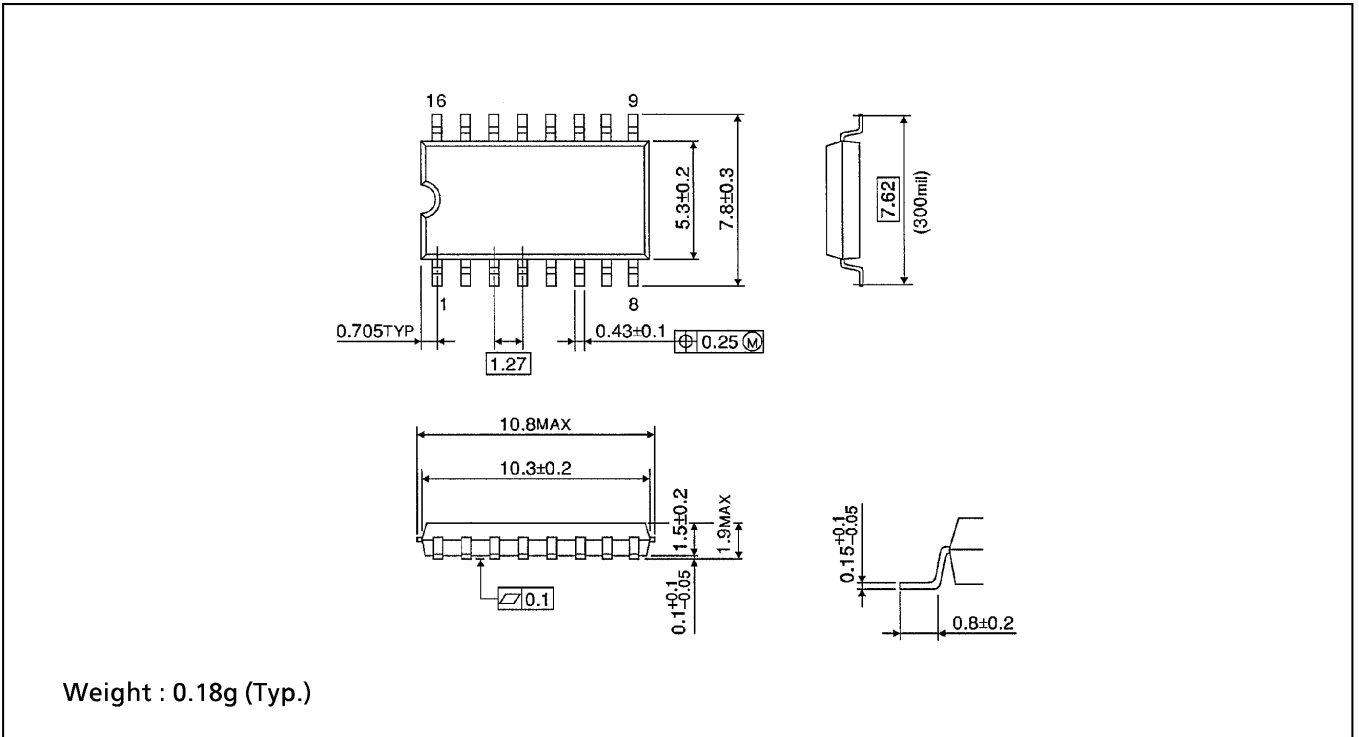
**DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)**

Unit in mm



**SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)**

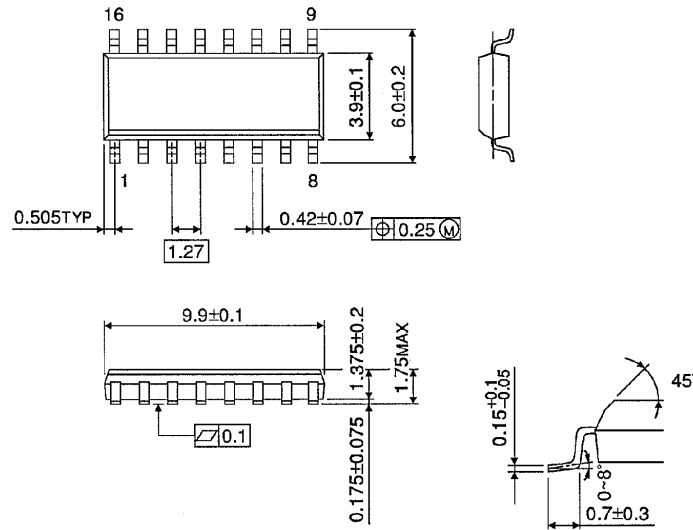
Unit in mm



SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)