15-W MONO CLASS-D AUDIO POWER AMPLIFIER

GENERAL DESCRIPTION

The TMPA401DM is a bridged-tied (BTL) Class-D audio amplifier for driving speakers with high power efficiency. It can drive 4Ω, 6Ω, 8Ω or 16Ω speakers. The output power can be up to 15W. No external heat-sink is necessary.

The gain of the amplifier is defined by input resistance. The internally fully differential input structure provides good common mode rejection and power supply rejection.

Thermal protection and short-circuit protection are integrated for safety purpose.

The internal de-pop circuitry eliminates pop noise at power-up & shutdown operations.

APPLICATIONS

LCD Monitors, TVs, DVD Players and Powered Speakers

FEATURES

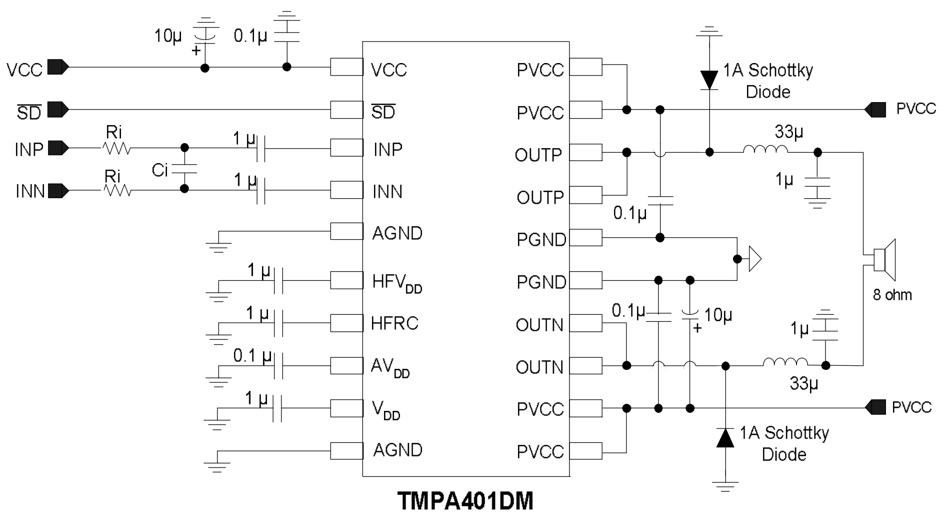
- 15-W Class-D Output
- Power efficiency is up to 82%
- Time delay for de-pop control
- Thermal Protection
- Output Pin Short-Circuit Protection (Short to Other Outputs, Short to VCC, Short to Ground)
- Differential / Single-Ended Input
- Low Supply Current (5mA Typical at 12V)
- Low Current in Shutdown Mode (<1μA Typical)
- Separate VCC & PVCC

PACKAGE

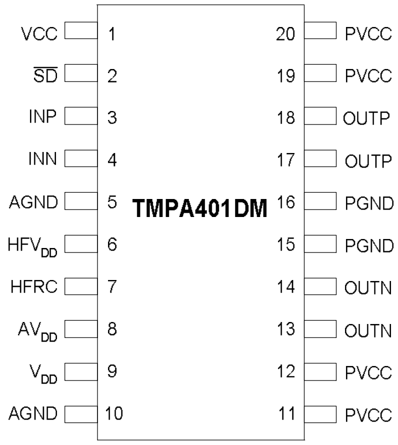
TSSOP20 available

For best performance, please refer to
http://www.taimec.com.tw/data/Tmpa401EVM/tmpa401dmEVM.pdf
for PCB layout.

REFERENCE CIRCUIT



TOP VIEW

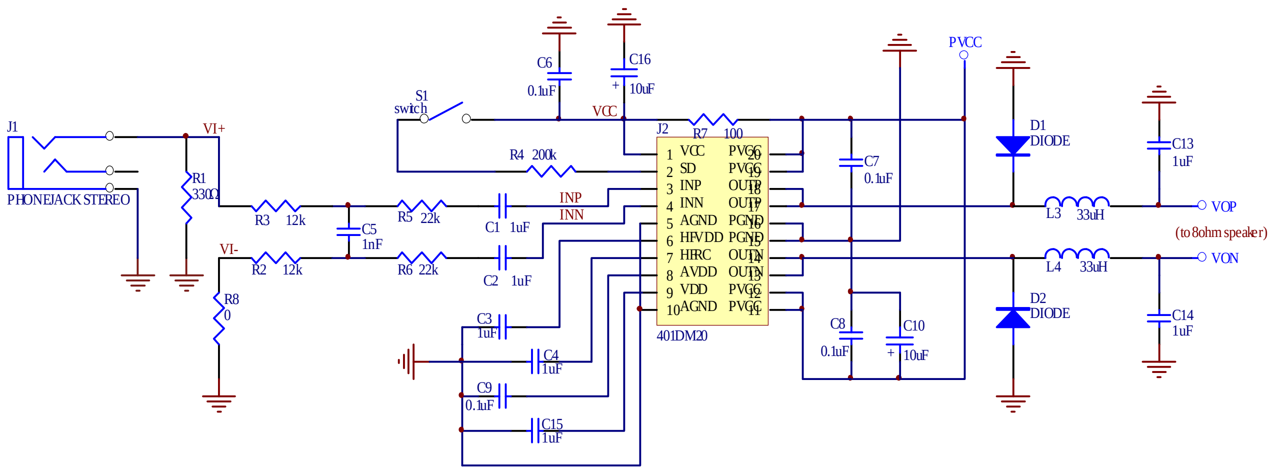


（Please email david@taimec.com.tw for complete datasheet.）

Tai-1 Microelectronics reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers are responsible for their products and applications using Tai-1 Microelectronics components.

Note that the external components or PCB layout should be designed not to generate abnormal voltages to the chip to prevent from latch up which may cause damage to the device.

Typical Application



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	PIN NO		
AGND	5,10	–	Analog ground
AV_{DD}	8	I	5-V analog power supply
HFRC	7	I	De-pop control
HFV_{DD}	6	O	2.5-V Reference for convenience of single-ended input
INN	4	I	Negative differential input
INP	3	I	Positive differential input
OUTN	13,14	O	Negative output
OUTP	17,18	O	Positive output
PGND	15,16	–	Power ground
PVCC	11,12,19,20	–	Power supply for output MOS (8V to 15V)
V_{CC}	1	–	High-voltage power supply (8V to 15V)
V_{DD}	9	O	5-V Reference output(25-mA)
$\overline{SD}$	2	I	Shutdown (Low valid)

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted(1)

Supply voltage, PVcc, Vcc	In normal mode	-0.3V to 18V	V
	In shutdown mode	-0.3V to 18V	V
Input voltage, $\overline{SD}$		-0.3V to Vcc+0.3V	V
Continuous total power dissipation		See package dissipation ratings	
Operating free-air temperature, T_A		-20 to 85	°C
Operating junction temperature, T_J		-20 to 150	°C
Storage temperature, T_{stg}		-40 to 150	°C

(1) Stresses beyond those listed under ”absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions “is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{CC}	PV_{CC}, V_{CC}	8	15	V
High-level input voltage, V_{IH}	$\overline{SD}$	2.0		V
Low-level input voltage, V_{IL}	$\overline{SD}$		0.8	V
Operating free-air temperature, T_A		-20	85	°C

PACKAGE DISSIPATION RATINGS

PACKGE	DERATING FACTOR	$T_A \leq 25$ °C POWER RATING	$T_A = 70$ °C POWER RATING	$T_A = 85$ °C POWER RATING
TSSOP20(FD)	30 mW/ °C	3.75W	2.4W	1.95W

DC CHARACTERISTICS

T_A=25 °C, V_{CC}=15V, R_L=8Ω speaker (unless otherwise noted)

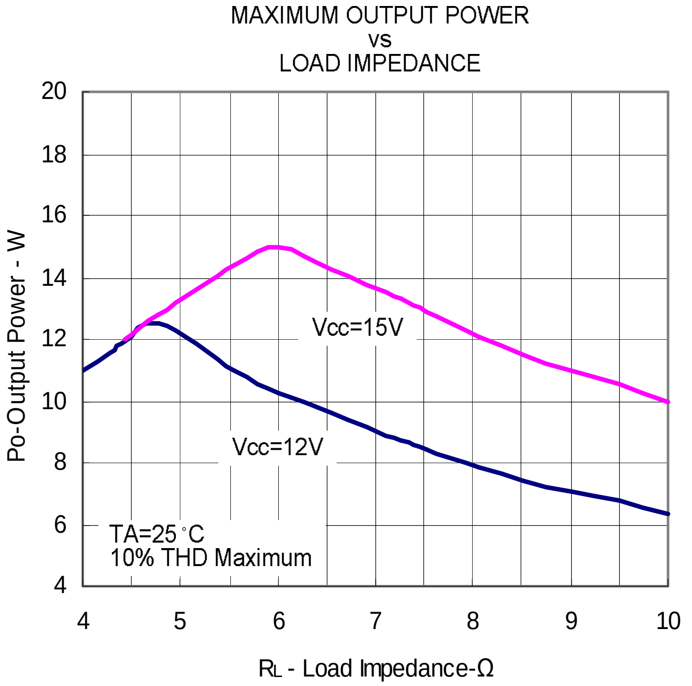
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	BTL Output offset voltage	INN and INP AC grounded Gain=20dB		25	100	mV
HFV_{DD}	Half V_{DD} reference output	No load		0.5x AV_{DD}		V
AV_{DD}/V_{DD}	5-V Regulated voltage	I_O=0 to 25mA, $\overline{SD}$ =High, V_{CC}=8V to 15V	4.5	5.0	5.5	V
I_{CC}	Quiescent current (no load)	$\overline{SD}$ =High, V_{CC}= 12V		5	10	mA
		$\overline{SD}$ =High, V_{CC}= 15V		8	16	
$I_{CC(SD)}$	Supply current in shutdown mode	$\overline{SD}$ =0V, V_{CC}= 12V		0.2	1	uA
		$\overline{SD}$ =0V, V_{CC}= 15V		0.2	1	
$r_{ds(on)}$	Drain-source on-state resistance	V_{CC}=15V I_O=1A, High side		600		mΩ
		Low side		500		
		Total		1100		
*Gain	Voltage Gain	Ri=40k		22		dB
		Ri=20k		25.5		
		Ri=10k		28		
		Ri= 0k		31.5		
I_{IH}	High-level input current	V_I =2V($\overline{SD}$), V_{CC}=8~15V			20	uA
I_{IL}	Low-level input current	V_I =0V($\overline{SD}$), V_{CC}=8~15V			1	uA
fosc	Oscillator frequency	V_{CC}=8~15V	200		300	kHz
Zi	Input resistance of INN/INP			20		kΩ

*Gain= $\frac{750k}{Ri+20K}$ (Vcc=15V) , Gain= $\frac{600k}{Ri+20K}$ (Vcc=12V), Ri：external input resistance of INP/INN inputs

AC CHARACTERISTICS

T_A=25 °C, V_{CC}=15V, R_L=8Ω speaker (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$P_{O(max)}$	Maximum continuous output power (r.m.s) at 1kHz	R_L=4Ω	15V		Not allowed		W
			12V		10.5		
		R_L=6Ω	15V		15		W
			12V		9.6		
		R_L=8Ω	15V		13		W
			12V		8.2		
		R_L=16Ω	15V		7.8		W
			12V		5		
THD+N	Total harmonic distortion plus noise	Vcc=12V, PO=7W, RL=6Ω, f=1kHz			0.4		%
		Vcc=15V, PO=12W, RL=6Ω, f=1kHz			0.47		
		Vcc=12V, PO=6W, RL=8Ω, f=1kHz			0.3		
		Vcc=15V, PO=9.5W, RL=8Ω, f=1kHz			0.42		
V_n	Output noise	Vcc=12V, Po at THD+N<0.5%, f=1kHz Gain=20dB			-70		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N＜0.5%, f=1kHz			85		dB
Crosstalk	Crosstalk between outputs	V_{CC}=12V, P_O=1W R_L=8Ω			-60		dB
	Thermal trip point				145		°C
	Thermal hysteresis				25		°C


MAXIMUM OUTPUT POWER
vs
LOAD IMPEDANCE
20
18
16
14
12
10
8
6
4
Po-Output Power - W
Vcc=15V
Vcc=12V
TA=25°C
10% THD Maximum
4
5
6
7
8
9
10
RL - Load Impedance-Ω

DETAILED DESCRIPTION

Efficiency

The output transistors of a class D amplifier act as switches. The power loss is mainly due to the turn on resistance of the output transistors when driving current to the load. As the turn on resistance is so small that the power loss is small and the power efficiency is high. With 8 ohm load the power efficiency can be better than 82%.

PCB layout for power dissipation

No heat sink is necessary for power dissipation. However the PCB layout should be well designed to dissipate heat for high output power. With 80% power efficiency the generated heat when driving 15 watts to the 8 ohm load is about 3.75 watts. The heat can be carried out through the thermal pad of the device to the PCB. To ensure proper dissipation of heat the PCB has to have heat path from the bottom of the device which is soldered to the PCB. The area of the metal on the PCB for heat dissipation should be big enough. It is suggested that both sides of the PCB are used for power dissipation.

Shutdown

The shutdown mode reduces power consumption. A LOW at shutdown pin forces the device in shutdown mode and a HIGH forces the device in normal operating mode. Shutdown mode is useful for power saving when not in use. This function is useful when other devices like earphone amplifier on the same PCB are used but class D amplifier is not necessary.

Pop-less

A soft start capacitor can be added to the HFRC pin. This capacitor introduces delay for the internal circuit to be stable before driving the load. The pop or click noise when power up/down or switching in between shutdown mode can be thus eliminated. The delay time is proportional to the value of the capacitance. It is about 300ms for a capacitor of 1uF.

Differential input VS single ended input

Differential input offers better noise immunity over single ended input. A differential input amplifier suppresses common noise and amplifies the difference voltage at the inputs. For single ended applications just tie the negative input end of the balanced input structure to ground. If external input resistors are used, the negative input has to be grounded with a series resistor of the same value as the positive input to reduce common noise.

Voltage gain

The voltage gain can be set through input resistance connecting to input pins. Lower input resistance can be used for higher gain. The voltage gain is defined by (800k ohms)/(Ri+20k ohms) at Vcc=15V without loading, where 20k ohms is internal resistance and Ri is external series resistance of the input pin. If Ri is not used (Ri=0 ohm) the voltage gain is (800k ohms)/(20k ohms) or 32dB. Insert Ri if lower gain is preferable. For example if Ri=30k ohms then voltage is (800k ohms)/(30k+20k ohms) or 24dB. For best result the input resistors should be well matched. Matched resistors are also required even for single ended input configuration for low noise.

Input filter

AC coupling capacitors are required to block the DC voltage from the device. They also define the –3db frequency at the low frequency side.

The –3db frequency of the low frequency side is

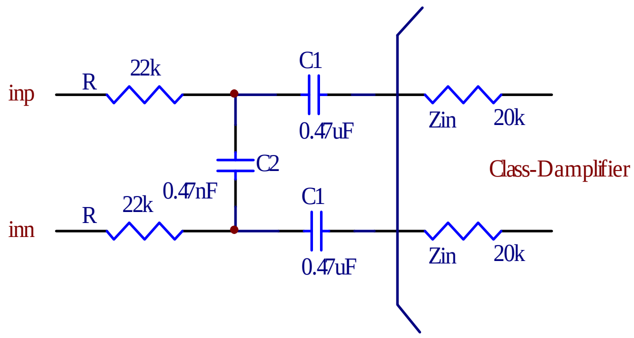
$$f\text{-}3db = 1/(2\pi R C)$$

where C is the AC coupling capacitance and R is the total resistance in series with C.

Note that R=Zin(internal resistance) + Rext(external resistance)

Also note that the internal input resistance of INN/INP is 20K ohms.

In the following diagram Rext=22k ohms, Zin=20k ohms and C=C1=0.47uF. Thus the –3db frequency at the low frequency side is about 8Hz.



A bypass capacitor placed in between the positive signal path and negative signal path is to attenuate the high frequencies. It defines the –3bd frequency at the high frequency side. The input filter becomes a band pass filter.

The –3db frequency of the high frequency side is

$$f\text{–}3db=1/(2\pi RC)$$

where C is the bypass capacitance and R is the total resistance in parallel with C.

In this example Rext=22k ohms, Zin=20k ohms and C=C2=0.47nF. Thus the –3db frequency at the high frequency side is about 16kHz.

Input filter

Since the input pins of the device have high impedance it is suggested that an input filter is incorporated as shown in the diagram. The AC coupling capacitors are used to block the DC voltage from the device. They also define the –3db frequency at the low frequency side. A bypass capacitor placed in between the positive signal path and negative signal path is to attenuate the high frequencies. It defines the –3db frequency at the high frequency side. The input filter becomes a band pass filter.

The –3db frequency of the low frequency side is

f-3db = 1/ 2 π R C

where C is the AC coupling capacitance(1uF) and R is the total resistance in series with C.

The –3db frequency of the high frequency side is

f-3db = 1/ 2 π R C

where C is the bypass capacitance(1nF) and R is the total resistance in parallel with C.

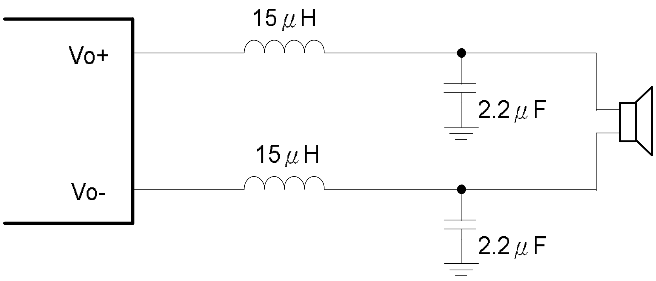
Note that there is 20K input resistor integrated in the chip for each input INP/INN.

Output filter

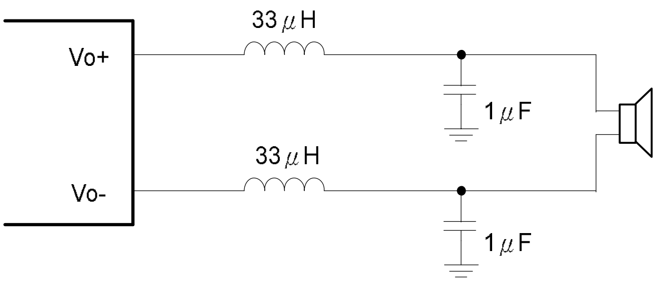
Ferrite bead filter can be used for EMI purpose. The ferrite filter reduces EMI around 1 MHz and higher（FCC and CE only test radiated emissions greater than 30 MHz）. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency（＜1 MHz）EMI sensitive circuits and/or there are long wires from the amplifier to the speaker. EMI is also affected by PCB layout and the placement of the surrounding components.

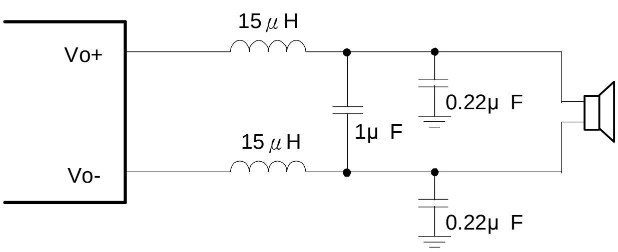
The suggested LC values for different speaker impendence are showed in following figures for reference.



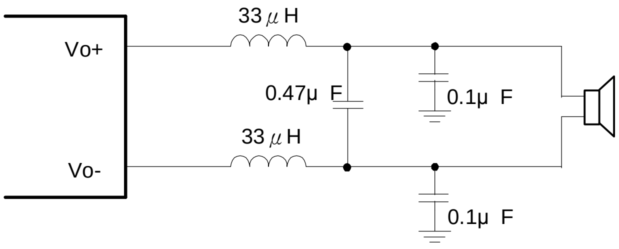
LC Output Filter(1), Speaker Impedance= 4Ω



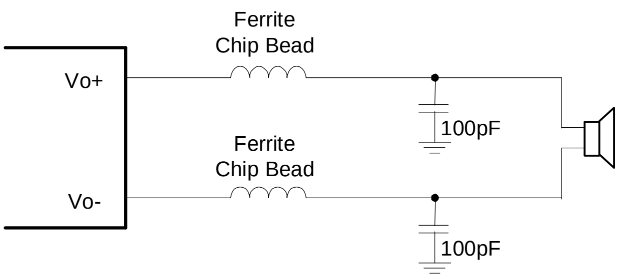
LC Output Filter(2), Speaker Impedance= 6Ω & 8Ω



LC Output Filter(3), Speaker Impedance= 4Ω



LC Output Filter(4), Speaker Impedance= 6Ω & 8Ω



Typical Ferrite Chip Bead Filter
（Chip bead example：遠越科技 KML2012Q102N
1kohms@100MHz, DCR=0.2ohms, I=1A）

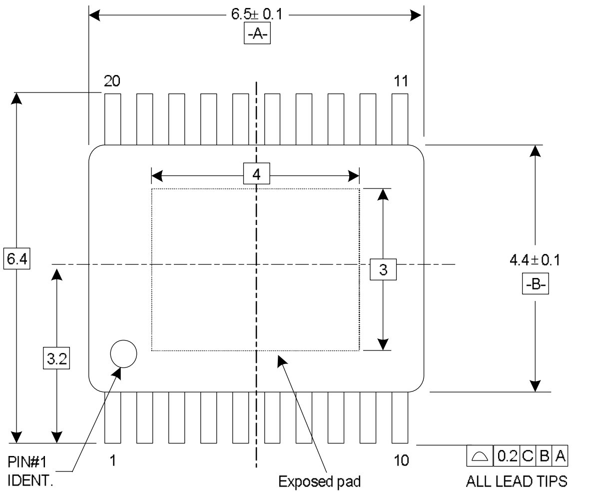
Over temperature protection

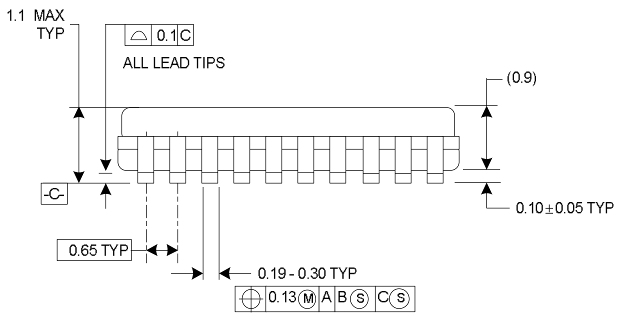
A temperature sensor is built in the device to detect the temperature inside the device. When a high temperature around 145oC and above is detected the switching output signals are disabled to protect the device from over temperature. Automatic recovery circuit enables the device to come back to normal operation when the internal temperature of the device is below around 120oC.

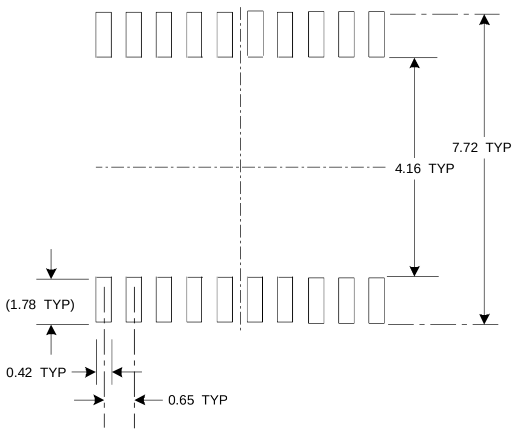
Over current protection

A current detection circuit is built in the device to detect the switching current of the output stages of the device. It disables the device when the current is beyond about 3.5amps. It protects the device when there is an accident short between outputs or between output and power/gnd pins It also protects the device when an abnormal low impedance is tied to the output. High current beyond the specification may potentially causes electron migration and permanently damage the device. Shutdown or power down is necessary to resolve the protection situation. There is no automatic recovery from over current protection.

Physical Dimensions (IN MILLIMETERS)







LAND PATTERN

TSSOP20

IMPORTANT NOTICE

Tai-1 Microelectronics Corp. reserves the right to make changes to its products and services and to discontinue any product or service without notice. Customers should obtain the latest relevant information for reference. Testing and quality control techniques are used to screen the parameters. Testing of all parameters of each product is not necessarily performed.

Tai-1 Microelectronics Corp. assumes no liability for applications assistance or customer product design. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

Reproduction of information in data sheets or related documentation is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Tai-1 Microelectronics Corp. is not responsible or liable for such altered documentation.

Resale of Tai-1 Microelectronics Corp. products or services with statements different from the parameters stated by Tai-1 Microelectronics Corp. for that product or service voids all express and any implied warranties. Tai-1 Microelectronics Corp. is not responsible or liable for any such statements.