FAIRCHILD
SEMICONDUCTOR™

January 1999
Revised June 2002

74LVT162245 • 74LVTH162245
Low Voltage 16-Bit Transceiver with 3-STATE Outputs and 25Ω Series Resistors in A Port Outputs

General Description

The LVT162245 and LVTH162245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The $T/\overline{R}$ inputs determine the direction of data flow through the device. The $\overline{OE}$ inputs disable both the A and B ports by placing them in a high impedance state.

The LVT162245 and LVTH162245 are designed with equivalent 25Ω series resistance in both the HIGH and LOW states on the A Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162245 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These non-inverting transceivers are designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162245 and LVTH162245 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH162245), also available without bushold feature (74LVT162245).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- A Port outputs include equivalent series resistance of 25Ω making external termination resistors unnecessary and reducing overshoot and undershoot
- A Port outputs source/sink ±12 mA.
  B Port outputs source/sink −32 mA/+64 mA
- Functionally compatible with the 74 series 162245
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human-body model > 2000V
  Machine model > 200V
  Charged-device model > 1000V
- Also packaged in plastic Fine Pitch Ball Grid Array (FBGA)

Ordering Code:

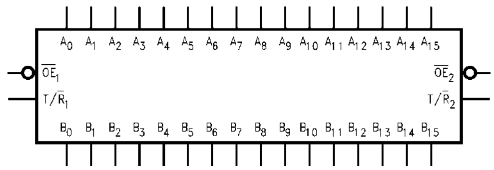
Order Number	Package Number	Package Description
74LVT162245G (Note 1)(Note 2)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVT162245MEA (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT162245MTD (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH162245G (Note 1)(Note 2)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVTH162245MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TUBE]
74LVTH162245MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LVTH162245MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBE]
74LVTH162245MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

Note 1: Ordering code “G” indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

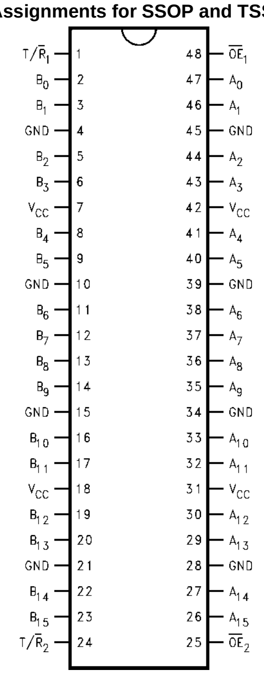
© 2002 Fairchild Semiconductor Corporation

Logic Symbol

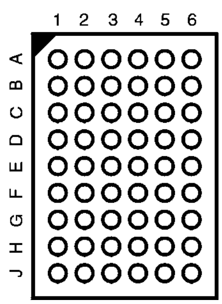


Connection Diagrams

Pin Assignments for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
$T/\overline{R}_n$	Transmit/Receive Input
A_0–A_{15}	Side A Inputs/3-STATE Outputs
B_0–B_{15}	Side B Inputs/3-STATE Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	B_0	NC	$T/\overline{R}_1$	$\overline{OE}_1$	NC	A_0
B	B_2	B_1	NC	NC	A_1	A_2
C	B_4	B_3	V_{CC}	V_{CC}	A_3	A_4
D	B_6	B_5	GND	GND	A_5	A_6
E	B_8	B_7	GND	GND	A_7	A_8
F	B_{10}	B_9	GND	GND	A_9	A_{10}
G	B_{12}	B_{11}	V_{CC}	V_{CC}	A_{11}	A_{12}
H	B_{14}	B_{13}	NC	NC	A_{13}	A_{14}
J	B_{15}	NC	$T/\overline{R}_2$	$\overline{OE}_2$	NC	A_{15}

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	$T/\overline{R}_1$	
L	L	Bus B_0–B_7 Data to Bus A_0–A_7
L	H	Bus A_0–A_7 Data to Bus B_0–B_7
H	X	HIGH-Z State on A_0–A_7, B_0–B_7

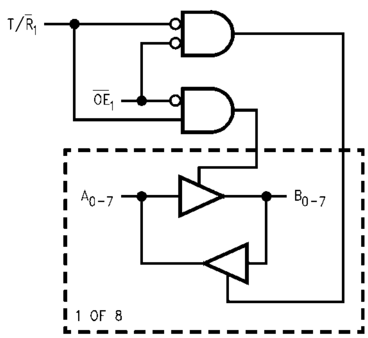
Inputs		Outputs
$\overline{OE}_2$	$T/\overline{R}_2$	
L	L	Bus B_8–B_{15} Data to Bus A_8–A_{15}
L	H	Bus A_8–A_{15} Data to Bus B_8–B_{15}
H	X	HIGH-Z State on A_8–A_{15}, B_8–B_{15}

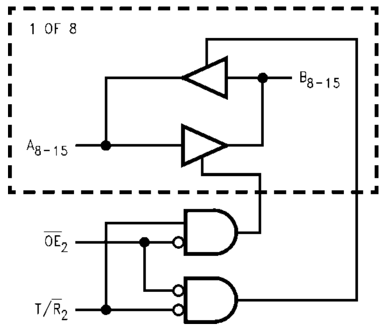
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Functional Description

The LVT162245 and LVTH162245 contain sixteen non-inverting bidirectional buffers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Logic Diagrams





Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	–0.5 to +4.6		V
V_I	DC Input Voltage	–0.5 to +7.0		V
V_O	Output Voltage	–0.5 to +7.0	Output in 3-STATE	V
		–0.5 to +7.0	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	–65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage		2.7	3.6	V
V_I	Input Voltage		0	5.5	V
I_{OH}	HIGH-Level Output Current	B Port		–32	mA
		A Port		–12	
I_{OL}	LOW-Level Output Current	B Port		64	mA
		A Port		12	
T_A	Free Air Operating Temperature		–40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	T_A = –40°C to +85°C Min	Max	Units	Conditions
V_{IK}	Input Clamp Diode Voltage		2.7		–1.2	V	I_I = –18 mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \leq$ 0.1V or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8	V	$V_O \geq V_{CC}$ – 0.1V
V_{OH}	Output HIGH Voltage	A Port	3.0	2.0		V	I_{OH} = –12 mA
			2.7–3.6	V_{CC}–0.2		V	I_{OH} = –100 µA
		B Port	2.7	2.4		V	I_{OH} = –8 mA
			3.0	2.0			I_{OH} = –32 mA
V_{OL}	Output LOW Voltage	A Port	3.0		0.8	V	I_{OL} = 12 mA
			2.7		0.2	V	I_{OL} = 100 µA
		B Port	2.7		0.5	V	I_{OL} = 24 mA
			3.0		0.4		I_{OL} = 16 mA
			3.0		0.5		I_{OL} = 32 mA
			3.0		0.55		I_{OL} = 64 mA
$I_{I(HOLD)}$ (Note 5)	Bushold Input Minimum Drive		3.0	75		µA	V_I = 0.8V
				–75			V_I = 2.0V
$I_{I(OD)}$ (Note 5)	Bushold Input Over-Drive Current to Change State		3.0	500		µA	(Note 6)
				–500			(Note 7)
I_I	Input Current		3.6		10	µA	V_I = 5.5V
		Control Pins	3.6		±1		V_I = 0V or V_{CC}
		Data Pins	3.6		–5		V_I = 0V
					1		$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current		0		±100	µA	0V $\leq V_I$ or $V_O \leq$ 5.5V

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$ Min	Max	Units	Conditions
$I_{PU/PD}$	Power Up/Down 3-STATE Current	0–1.5V		±100	µA	$V_O = 0.5V$ to $3.0V$ $V_I = GND$ to V_{CC}
I_{OZL}	3-STATE Output Leakage Current	3.6		–5	µA	$V_O = 0.5V$
I_{OZL} (Note 5)	3-STATE Output Leakage Current	3.6		–5	µA	$V_O = 0.0V$
I_{OZH}	3-STATE Output Leakage Current	3.6		5	µA	$V_O = 3.0V$
I_{OZH} (Note 5)	3-STATE Output Leakage Current	3.6		5	µA	$V_O = 3.6V$
$I_{OZH}+$	3-STATE Output Leakage Current	3.6		10	µA	$V_{CC} < V_O \leq 5.5V$
I_{CCH}	Power Supply Current	3.6		0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current	3.6		5	mA	Outputs LOW
I_{CCZ}	Power Supply Current	3.6		0.19	mA	Outputs Disabled
$I_{CCZ}+$	Power Supply Current	3.6		0.19	mA	$V_{CC} \leq V_O \leq 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 8)	3.6		0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 5: Applies to Bushold versions only (74LVTH162245).

Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 8: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 9)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Min	Typ	Max	Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 10)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		–0.8		V	(Note 10)

Note 9: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 10: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Data to A Port Output	1.0	4.0	1.0	4.6	ns
t_{PHL}		1.0	3.7	1.0	4.1	
t_{PLH}	Propagation Delay Data to B Port Output	1.0	3.5	1.0	3.9	ns
t_{PHL}		1.0	3.5	1.0	3.9	
t_{PZH}	Output Enable Time for A Port Output	1.0	5.3	1.0	6.3	ns
t_{PZL}		1.0	5.6	1.0	7.2	
t_{PZH}	Output Enable Time for B Port Output	1.0	4.6	1.0	5.4	ns
t_{PZL}		1.0	5.3	1.0	6.9	
t_{PHZ}	Output Disable Time for A Port Output	1.5	5.6	1.5	6.3	ns
t_{PLZ}		1.5	5.5	1.5	5.5	
t_{PHZ}	Output Disable Time for B Port Output	1.5	5.4	1.5	6.1	ns
t_{PLZ}		1.5	5.1	1.5	5.4	
t_{OSHL} t_{OSLH}	A Port Output to Output Skew (Note 11)		1.0		1.0	ns
t_{OSHL} t_{OSLH}	B Port Output to Output Skew (Note 11)		1.0		1.0	ns

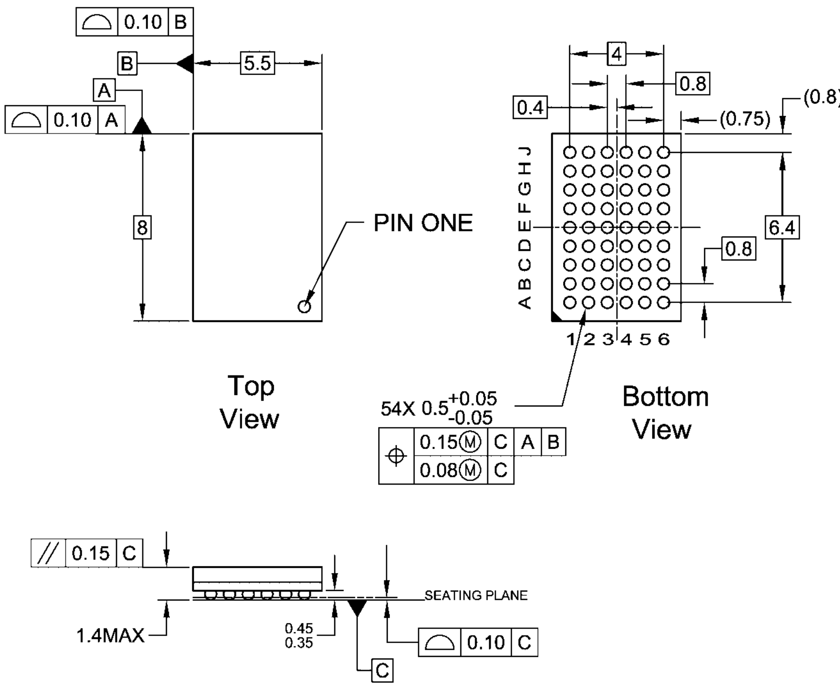
Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 12)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	8	pF

Note 12: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted

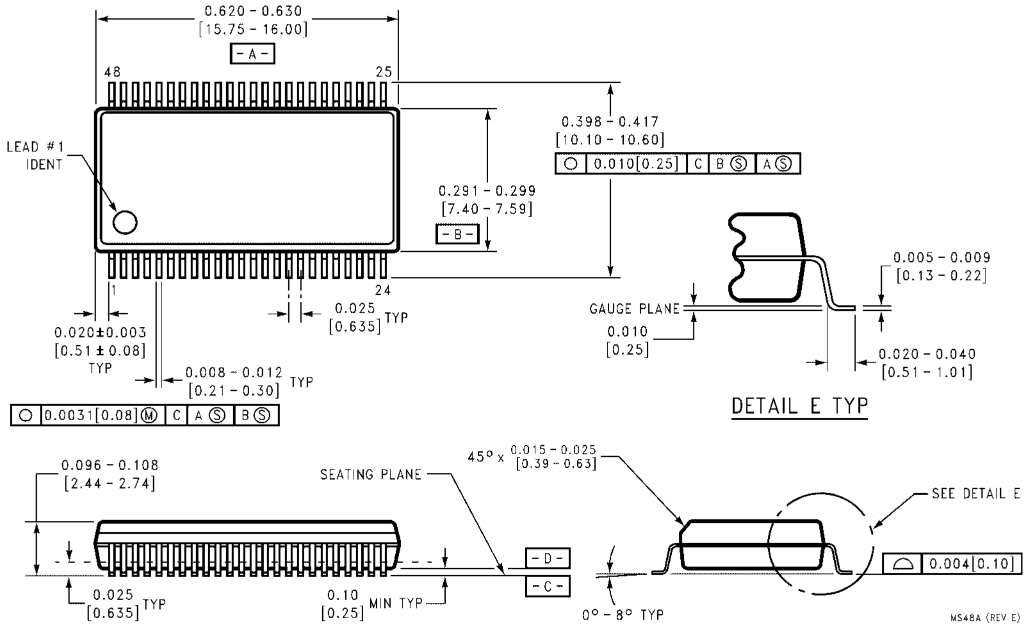


NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

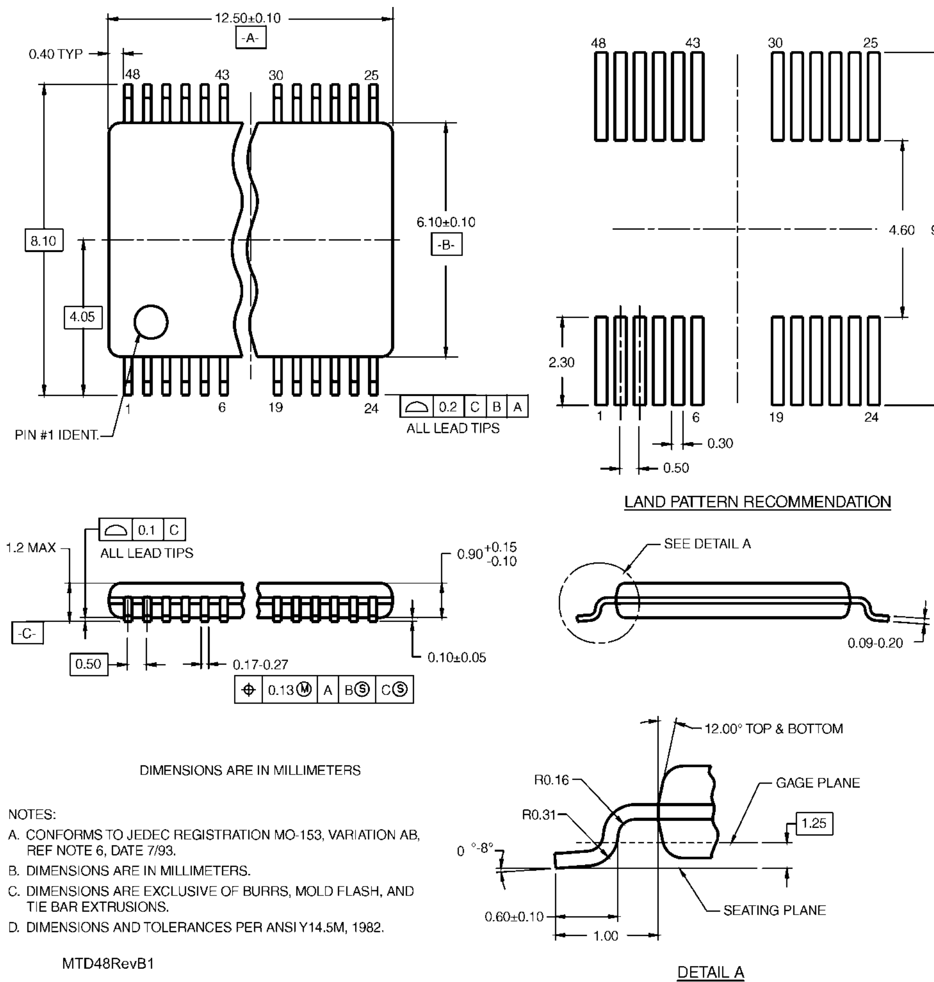
54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com