LT6552

3.3V Single Supply Video Difference Amplifier

July 2003

FEATURES

- **Differential or Single-Ended Gain Block**
- **Wide Supply Range 3V to 12.6V**
- **Output Swings Rail-to-Rail**
- **Input Common Mode Range Includes Ground**
- **600V/µs Slew Rate**
- **–3dB Bandwidth = 75MHz, $A_V = \pm 2$**
- CMRR at 10MHz: >60dB
- Output Swings Rail-to-Rail
- Specified on 3.3V, 5V and ±5V Supplies
- High Output Drive: ±70mA
- Power Shutdown to 300µA
- Operating Temperature Range: –40°C to 85°C
- Tiny 3mm x 3mm x 1mm DFN Package

APPLICATIONS

- Differential to Single-Ended Conversion
- Video Line Driver
- Automotive Displays
- RGB Amplifiers
- Coaxial Cable Drivers
- Low Voltage High Speed Signal Processing

DESCRIPTION

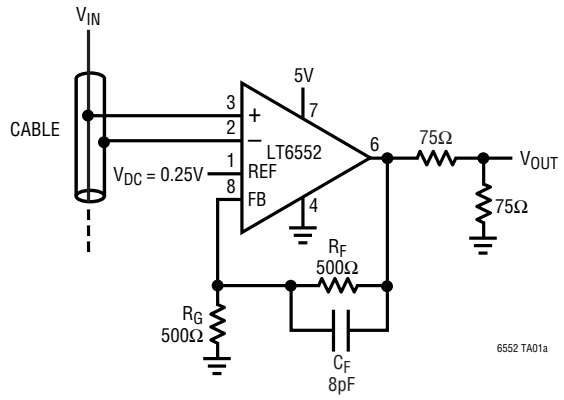
The LT®6552 is a video difference amplifier optimized for low voltage single supply operation. This versatile amplifier features uncommitted high input impedance (+) and (–) inputs and can be used in differential or single-ended configurations. A second set of inputs gives gain adjustment and DC control to the differential amplifier.

On a single 3.3V supply, the input voltage range extends from ground to 1.3V and the output can swing to within 400mV of the supply voltage while driving a 150Ω load. The LT6552 features 75MHz – 3dB bandwidth, 600V/µs slew rate, and ±70mA output current making it ideal for driving cables directly. The LT6552 maintains its performance for supplies from 3V to 12.6V and is fully specified at 3.3V, 5V and ±5V supplies. The shutdown feature reduces power dissipation to less than 1mW and allows multiple amplifiers to drive the same cable.

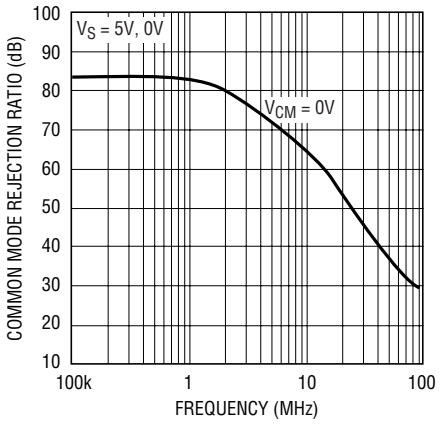
The LT6552 is available in the 8-pin SO package as well as a tiny, dual fine pitch leadless package (DFN). The device is specified over the commercial and industrial temperature range.

TYPICAL APPLICATION

Cable Sense Amplifier for Loop Through Connections with DC Adjust



Input Referred CMRR vs Frequency

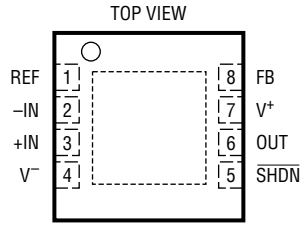


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to V^-) 12.6V
Input Current (Note 2) ..... ±10mA
Input Voltage Range ..... $\pm V_S$
Differential Input Voltage
+Input (Pin 3) to –Input (Pin 2) ..... $\pm V_S$
Output Short-Circuit Duration (Note 3) ..... Indefinite

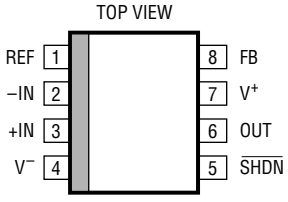
Operating Temperature Range (Note 4) ...–40°C to 85°C
Specified Temperature Range (Note 5) ....–40°C to 85°C
Maximum Junction Temperature ..... 150°C
(DD Package) ..... 125°C
Storage Temperature Range .....–65°C to 150°C
(DD Package) .....–65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 160°C/W (NOTE 3)
UNDERSIDE METAL INTERNALLY CONNECTED TO V^-
(PCB CONNECTION OPTIONAL)

ORDER PART NUMBER
LT6552CDD LT6552IDD
DD PART MARKING*
ADR



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT6552CS8 LT6552IS8
S8 PART MARKING
6552 6552I

*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

3.3V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3.3V, 0V. Figure 1 shows the DC test circuit, $V_{REF} = V_{CM}$ = 1V, V_{DIFF} = 0V, $V_{\overline{SHDN}} = V^+$, unless otherwise noted. $R_L = R_F + R_G$ = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs (Note 7)			5	20	mV
			●			25	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		40		µV/°C
I_B	Input Bias Current	Any Input	●		25	50	µA
I_{OS}	Input Offset Current	Either Input Pair	●		1	5	µA

3.3V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 3.3V, 0V. Figure 1 shows the DC test circuit, V_{REF} = V_{CM} = 1V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R_G = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
e_n	Input Noise Voltage Density	f = 10kHz			55		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz			0.7		pA/√Hz
R_{IN}	Input Resistance	Common Mode, V_{CM} = 0V to 1.3V			300		kΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 1.3V	●	58	75		dB
	Input Range		●	0		1.3	V
PSRR	Power Supply Rejection	V_S = 3V to 12V	●	48	54		dB
	Minimum Supply (Note 8)		●	3			V
G_E	Gain Error	V_O = 0.5V to 2V, R_L = 1k R_L = 150Ω	● ●		1 1	3 3	% %
V_{OH}	Swing High	(V_{DIFF} = 0.4V), V_{REF} (Pin 1) = 0V, A_V = 10 R_L = 1k R_L = 150Ω R_L = 75Ω	 ● ● 	 3.1 2.5 2	 3.2 2.9 2.5		 V V V
V_{OL}	Swing Low	(V_{DIFF} = –0.1V), V_{REF}(Pin 1) = 0V, A_V = 10 R_L = 1k I_{SINK} = 5mA I_{SINK} = 10mA	 ● ● ●	 	 8 65 40	 50 120 200	 mV mV mV
SR	Slew Rate	V_{OUT} = 0.5V to 2.5V Measure from 1V to 2V, R_L = 150Ω, A_V = 2			350		V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_O = $2V_{P-P}$			55		MHz
BW	Small-Signal –3dB Bandwidth	A_V = 2, R_L = 150Ω			65		MHz
t_r, t_f	Rise Time, Fall Time (Note 10)	A_V =50, V_O = 0.5V to 2.5V, 20% to 80%, R_L = 150Ω			125	175	ns
t_S	Settling Time to 3% Settling Time to 1%	A_V = 2, ΔV_{OUT} = 2V R_L = 150Ω			20 30		ns ns
	Differential Gain	A_V = 2, R_L = 150Ω, Black Level = 0.6V			0.4		%
	Differential Phase	A_V = 2, R_L = 150Ω, Black Level = 0.6V			0.15		Deg
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{DIFF} = 1V	 ●	35 25	50		mA mA
I_S	Supply Current		 ●		12	13.5 15	mA mA
	Supply Current Shutdown	$V_{\overline{SHDN}}$ = 0.5V	●		300	750	µA
V_L	Shutdown Pin Input Low Voltage		●			0.5	V
V_H	Shutdown Pin Input High Voltage		●	3			V
	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.5V $V_{\overline{SHDN}}$ = 3V	● ●		40 3	150 10	µA µA
t_{ON}	Turn On-Time	$V_{\overline{SHDN}}$ from 0.5V to 3V			250		ns
t_{OFF}	Turn Off-Time	$V_{\overline{SHDN}}$ from 3V to 0.5V			450		ns

5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V; Figure 1 shows the DC test circuit, V_{REF} = V_{CM} = 1V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R_G = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs (Note 7)			5	20	mV
			●			25	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		40		µV/°C
I_B	Input Bias Current	Any Input	●		25	50	uA
I_{OS}	Input Offset Current	Either Input Pair	●		1	5	uA
e_n	Input Noise Voltage Density	f = 10kHz			55		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz			0.7		pA/√Hz
R_{IN}	Input Resistance	Common Mode, V_{CM} = 0V to 3V			300		kΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 0V to 3V	●	58	75		dB
	Input Range		●	0		3	V
PSRR	Power Supply Rejection	V_S = 3V to 12V	●	48	54		dB
	Minimum Supply (Note 8)		●	3			V
G_E	Gain Error	V_O = 0.5V to 3.5V, R_L = 1k	●		1	3	%
		R_L = 150Ω	●		1	3	%
V_{OH}	Swing High	(V_{DIFF} = 0.6V), V_{REF}(Pin 1) = 0V, A_V = 10					
		R_L = 1k	●	4.8	4.875		V
		R_L = 150Ω	●	3.6	4.3		V
		R_L = 75Ω, 0°C ≤ T_A ≤ 70°C (Only)	●	2.75	3.4		V
V_{OL}	Swing Low	(V_{DIFF} = –0.1V), V_{REF} (Pin 1) = 0V, A_V = 10					
		R_L = 1k	●		8	50	mV
		I_{SINK} = 5mA	●		65	120	mV
		I_{SINK} = 10mA	●		110	200	mV
SR	Slew Rate	V_{OUT} = 0.5V to 3.5V Measure from 1V to 3V, R_L = 150Ω, A_V = 2			450		V/µs
FPBW	Full-Power Bandwidth (Note 9)	V_O = $2V_{P-P}$			70		MHz
BW	Small-Signal –3dB Bandwidth	A_V = 2, R_L = 150Ω			70		MHz
t_r, t_f	Rise Time, Fall Time	5V, 0V; A_V = 50, V_O = 0.5V to 3.5V, 20% to 80%, R_L = 1k			125	175	ns
t_S	Settling Time to 3% Settling Time to 1%	A_V = 2, ΔV_{OUT} = 2V R_L = 150Ω			20 30		ns ns
	Differential Gain	A_V = 2, R_L = 150Ω, Black Level = 1V			0.25		%
	Differential Phase	A_V = 2, R_L = 150Ω, Black Level = 1V			0.04		Deg
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{DIFF} = 1V		50	70		mA
		0°C ≤ T_A ≤ 70°C	●	45			mA
		–40°C ≤ T_A ≤ 85°C	●	35			mA
I_S	Supply Current				13	14.5	mA
			●			16	mA
	Supply Current Shutdown	$V_{\overline{SHDN}}$ = 0.5V	●		400	900	µA
V_L	Shutdown Pin Input Low Voltage		●			0.5	V
V_H	Shutdown Pin Input High Voltage		●	4.7			V
	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 0.5V	●		70	200	µA
		$V_{\overline{SHDN}}$ = 4.7V	●		4	10	µA

5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, 0V. Figure 1 shows the DC test circuit, V_{REF} = V_{CM} = 1V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R_G = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ from 0.5V to 4.7V			250		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ from 4.7V to 0.5V			450		ns

±5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V. Figure 2 shows the DC test circuit, V_{REF} = V_{CM} = 0V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R_G = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs (Note 7)	 ●		10	25 30	mV mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		50		µV/°C
I_B	Input Bias Current	Any Input	●		25	50	µA
I_{OS}	Input Offset Current	Either Input Pair	●		1	5	µA
e_n	Input Noise Voltage Density	f = 10kHz			55		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz			0.7		pA/√Hz
R_{IN}	Input Resistance	Common Mode, V_{CM} = –5V to 3V			300		kΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = –5V to 3V	●	58	75		dB
	Input Range		●	–5		3	V
PSRR	Power Supply Rejection	V_S = ±2V to ±6V, V_{CM} = 0V	●	48	54		dB
G_E	Gain Error	V_O = –3V to 3V, R_L = 1k R_L = 150Ω	● ●		1 1	3 3	% %
	Output Voltage Swing	(V_{DIFF} = ± 0.6V), V_{REF} (Pin 1) = 0V, A_V = 10 R_L = 1k R_L = 150Ω R_L = 75Ω, 0°C ≤ T_A ≤ 70°C (Only)	 ● ● ●	 ±4.8 ±3.6 ±2.75	 ±4.875 ±4.3 ±3.4		 V V V
SR	Slew Rate	V_{CM} = 0V, V_{DIFF} = –1.5V to +1.5V, V_O = –5V to 5V Measure from –2V to 2V, R_L = 150Ω		400	600		V/µs
FPBW	Full-Power Bandwidth	V_O = $6V_{P-P}$ (Note 9)			30		MHz
BW	Small-Signal –3dB Bandwidth				75		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 50, V_O = –3V to 3V, 20% to 80%			125	175	ns
t_S	Settling Time to 3% Settling Time to 1%	A_V = 2, ΔV_{OUT} = 6V R_L = 150Ω			25 35		ns ns
	Differential Gain	A_V = 2, R_L = 150Ω			0.2		%
	Differential Phase	A_V = 2, R_L = 150Ω			0.15		Deg
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{DIFF} = ±1V 0°C ≤ T_A ≤ 70°C –40°C ≤ T_A ≤ 85°C	 ● ●	50 45 35	70		mA mA mA
	Supply Current Shutdown	$V_{\overline{SHDN}}$ = –4.5V	●		650	1400	µA
I_S	Supply Current		 ●		14	16.5 18.5	mA mA
V_L	Shutdown Pin Input Low Voltage		●			–4.5	V
V_H	Shutdown Pin Input High Voltage		●	4.7			V

±5V ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = ±5V. Figure 2 shows the DC test circuit, V_{REF} = V_{CM} = 0V, V_{DIFF} = 0V, $V_{\overline{SHDN}}$ = V^+, unless otherwise noted. R_L = R_F + R6 = 1k. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Shutdown Pin Current	$V_{\overline{SHDN}}$ = –4.5V $V_{\overline{SHDN}}$ = 4.7	● ●		85 3	250 10	µA µA
t_{ON}	Turn-On Time	$V_{\overline{SHDN}}$ from –4.5V to 4.7V			200		ns
t_{OFF}	Turn-Off Time	$V_{\overline{SHDN}}$ from 4.7V to –4.5V			400		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The inputs are protected from ESD with diodes to the supplies.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT6552C/LT6552I are guaranteed functional over the temperature range of –40°C to 85°C.

Note 5: The LT6552C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet specified performance from –40°C to 85°C, but is not tested or QA sampled at these temperatures. The LT6552I is guaranteed to meet specified performance from – 40°C to 85°C.

Note 6: When R_L = 1k is specified, the load resistor is R_F + R_G, but when R_L = 150Ω or R_L = 75Ω is specified, then an additional resistor of that value is added to the output.

Note 7: V_{OS} measured at the output (Pin 6) is the contribution from both input pairs and is input referred.

Note 8: Minimum supply is guaranteed by the PSRR test.

Note 9: Full power bandwidth is calculated from the slew rate.

FPBW = SR/2πVp

Note 10: V_S = 3.3V limits are guaranteed by correlation to V_S = 5V and ±5V tests.

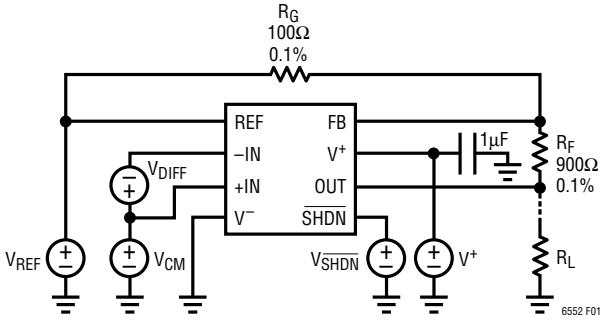


Figure 1. 3.3V, 5V DC Test Circuit

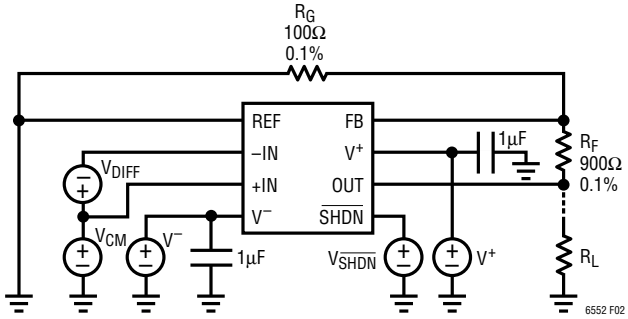


Figure 2. ±5V DC Test Circuit

APPLICATIONS INFORMATION

The LT6552 is a video difference amplifier with two pairs of high impedance inputs. The primary purpose of the LT6552 is to convert high frequency differential signals into a single-ended output, while rejecting any common mode noise. In the simplest configuration, one pair of inputs are connected to the incoming differential signal, while the other pair of inputs are used to set the amplifier gain and DC level. The device will operate on either single or dual supplies and has an input common mode range which includes the negative supply. The common mode rejection ratio is greater than 60dB at 10MHz.

Figure 3 shows the single supply connection. The amplifier gain is set by a feedback network from the output to Pin 8 (FB). A DC signal applied to pin 1 (REF) establishes the output quiescent voltage and the differential signal is applied to Pins 2 and 3.

Figure 4 shows several other connections using dual supplies. In each case, the amplifier gain is set by a feedback network from the output to Pin 8 (FB).

APPLICATIONS INFORMATION

Amplifier Characteristics

Figure 5 shows a simplified schematic of the LT6552. There are two input stages, the first one consists of transistors Q1 to Q8 for the (+) and (–) inputs while the second input stage consists of transistors Q9 to Q16 for the reference and feedback inputs. This topology provides high slew rates at low supply voltages. The input common mode range extends from ground to typically 1.75V from V_{CC}, and is limited by 2 $V_{BE's}$ plus a saturation voltage of current sources I1-I4. Each input stage drives the degeneration resistors of PNP and NPN current mirrors, Q17 to Q20, that convert the differential signals into a single-ended output. The complementary drive generator supplies current to the output transistors that swing from rail-to-rail.

The current generated through R1 or R2, divided by the capacitor CM, determines the slew rate. Note that this current, and hence the slew rate are proportional to the magnitude of the input step. The input step equals the output step divided by the closed loop gain. The highest slew rates are therefore obtained in the lowest gain configurations.

ESD

The LT6552 has reverse-biased ESD protection diodes on all inputs and outputs, as shown in Figure 5. If these pins are forced beyond either supply, unlimited current will flow through these diodes. If the current is transient in nature and limited to 100mA or less, no damage to the device will occur.

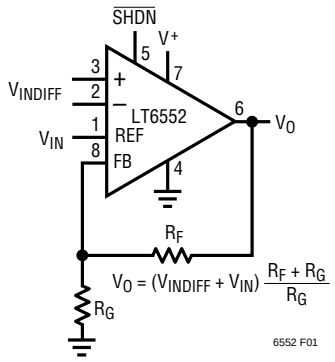


Figure 3

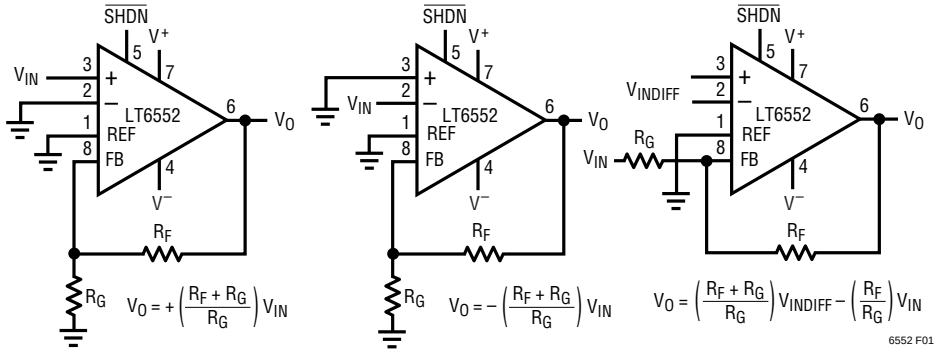


Figure 4

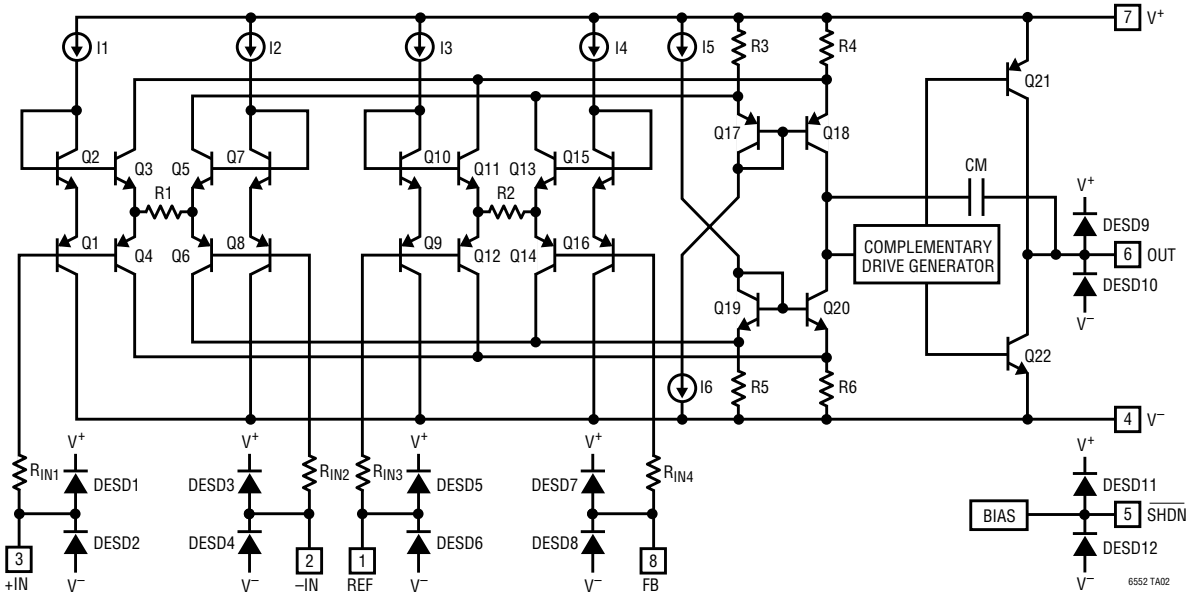
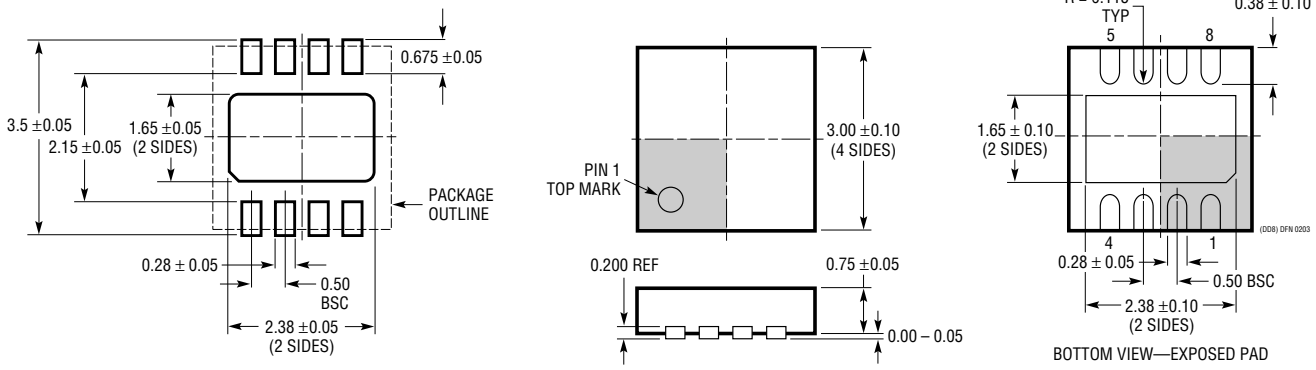


Figure 5. Simplified Schematic

PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

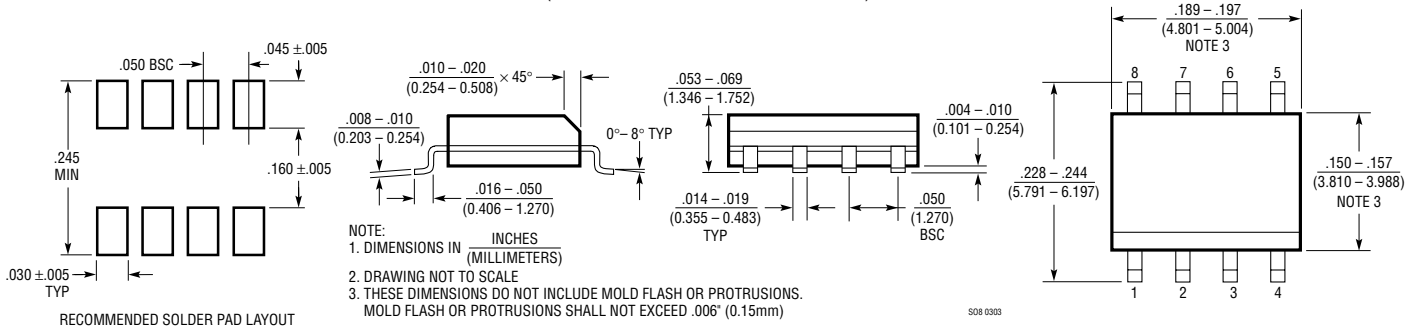


RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



RECOMMENDED SOLDER PAD LAYOUT

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1193	Av = 2 Video Difference Amp	80MHz BW, 500V/µs, Shutdown
LT1675	RGB Multiplexer with Current Feedback Amplifiers	–3dB Bandwidth = 250MHz, 100MHz Pixel Switching
LT1809/LT1810	Single/Dual 180MHz, Rail-to-Rail Input and Output Amplifiers	350V/µs Slew Rate, Shutdown, Low Distortion –90dBc at 5MHz
LT6550/LT6551	3.3V Triple and Quad Video Amplifiers	Internal Gain of 2, 110MHz –3dB Bandwidth, Input Common Modes to Ground

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT/TP 0703 1K • PRINTED IN USA