

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N-Channel Enhancement-Mode Silicon Gate

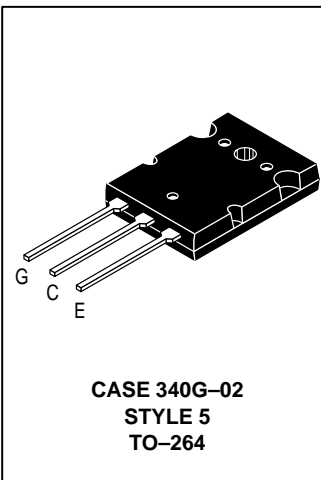
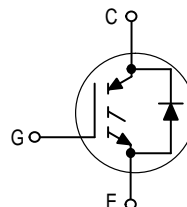
MGY25N120D

Motorola Preferred Device

IGBT & DIODE IN TO-264
25 A @ 90°C
38 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co-packaged with a soft recovery ultra-fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies. Co-packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO-264 Package (TO-3PBL)
- High Speed E_{off} : 216 μ J/A typical at 125°C
- High Short Circuit Capability – 10 μ s minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA



MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	1200	Vdc
Collector-Gate Voltage ($R_{GE} = 1.0 \text{ M}\Omega$)	V_{CGR}	1200	Vdc
Gate-Emitter Voltage — Continuous	V_{GE}	± 20	Vdc
Collector Current — Continuous @ $T_C = 25^\circ\text{C}$ — Continuous @ $T_C = 90^\circ\text{C}$ — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	38 25 76	Adc Adc Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	212 1.69	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	°C
Short Circuit Withstand Time ($V_{CC} = 720 \text{ Vdc}$, $V_{GE} = 15 \text{ Vdc}$, $T_J = 125^\circ\text{C}$, $R_G = 20 \Omega$)	t_{sc}	10	μ s
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	0.6 0.9 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	°C
Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Collector-to-Emitter Breakdown Voltage (V _{GE} = 0 Vdc, I _C = 25 μAdc) Temperature Coefficient (Positive)	V _{(BR)CES}	1200 —	— 960	— —	Vdc mV/°C
Zero Gate Voltage Collector Current (V _{CE} = 1200 Vdc, V _{GE} = 0 Vdc) (V _{CE} = 1200 Vdc, V _{GE} = 0 Vdc, T _J = 125°C)	I _{CES}	— —	— —	100 2500	μAdc
Gate-Body Leakage Current (V _{GE} = ± 20 Vdc, V _{CE} = 0 Vdc)	I _{GES}	—	—	250	nAdc

ON CHARACTERISTICS (1)

Collector-to-Emitter On-State Voltage (V _{GE} = 15 Vdc, I _C = 12.5 Adc) (V _{GE} = 15 Vdc, I _C = 12.5 Adc, T _J = 125°C) (V _{GE} = 15 Vdc, I _C = 25 Adc)	V _{CE(on)}	— — —	2.37 2.15 2.98	3.24 — 4.19	Vdc
Gate Threshold Voltage (V _{CE} = V _{GE} , I _C = 1.0 mAdc) Threshold Temperature Coefficient (Negative)	V _{GE(th)}	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V _{CE} = 10 Vdc, I _C = 20 Adc)	g _{fe}	—	12	—	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{CE} = 25 Vdc, V _{GE} = 0 Vdc, f = 1.0 MHz)	C _{ies}	—	1859	—	pF
Output Capacitance		C _{oes}	—	198	—	
Transfer Capacitance		C _{res}	—	30	—	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V _{CC} = 720 Vdc, I _C = 25 Adc, V _{GE} = 15 Vdc, L = 300 μH R _G = 20 Ω) Energy losses include "tail"	t _{d(on)}	—	91	—	ns
Rise Time		t _r	—	124	—	
Turn-Off Delay Time		t _{d(off)}	—	196	—	
Fall Time		t _f	—	310	—	mJ
Turn-Off Switching Loss		E _{off}	—	2.44	4.69	
Turn-On Switching Loss		E _{on}	—	3.14	5.22	
Total Switching Loss		E _{ts}	—	5.58	9.91	
Turn-On Delay Time	(V _{CC} = 720 Vdc, I _C = 25 Adc, V _{GE} = 15 Vdc, L = 300 μH R _G = 20 Ω, T _J = 125°C) Energy losses include "tail"	t _{d(on)}	—	88	—	ns
Rise Time		t _r	—	126	—	
Turn-Off Delay Time		t _{d(off)}	—	236	—	
Fall Time		t _f	—	640	—	mJ
Turn-Off Switching Loss		E _{off}	—	5.40	—	
Turn-On Switching Loss		E _{on}	—	5.03	—	
Total Switching Loss		E _{ts}	—	10.43	—	
Gate Charge	(V _{CC} = 720 Vdc, I _C = 25 Adc, V _{GE} = 15 Vdc)	Q _T	—	62	—	nC
		Q ₁	—	22	—	
		Q ₂	—	25	—	

DIODE CHARACTERISTICS

Diode Forward Voltage Drop (I _{EC} = 12.5 Adc) (I _{EC} = 12.5 Adc, T _J = 125°C) (I _{EC} = 25 Adc)	V _{FEC}	— — —	2.89 1.75 3.65	3.50 — 4.45	Vdc
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(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	$(I_F = 25 \text{ Adc}, V_R = 720 \text{ Vdc}, dI_F/dt = 150 \text{ A}/\mu\text{s})$	t_{rr}	—	114	—	ns
		t_a	—	71	—	
		t_b	—	43	—	
Reverse Recovery Stored Charge	Q_{RR}	—	0.65	—	μC	
Reverse Recovery Time	$(I_F = 25 \text{ Adc}, V_R = 720 \text{ Vdc}, dI_F/dt = 150 \text{ A}/\mu\text{s}, T_J = 125^\circ\text{C})$	t_{rr}	—	226	—	ns
		t_a	—	165	—	
		t_b	—	61	—	
Reverse Recovery Stored Charge	Q_{RR}	—	1.90	—	μC	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)	L_E	—	13	—	nH	

TYPICAL ELECTRICAL CHARACTERISTICS

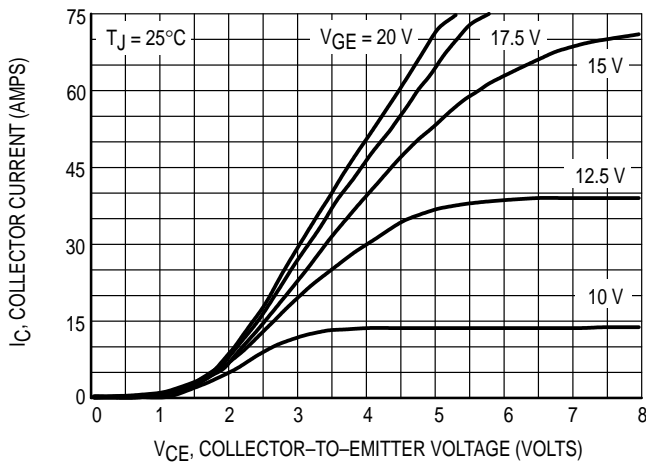


Figure 1. Output Characteristics

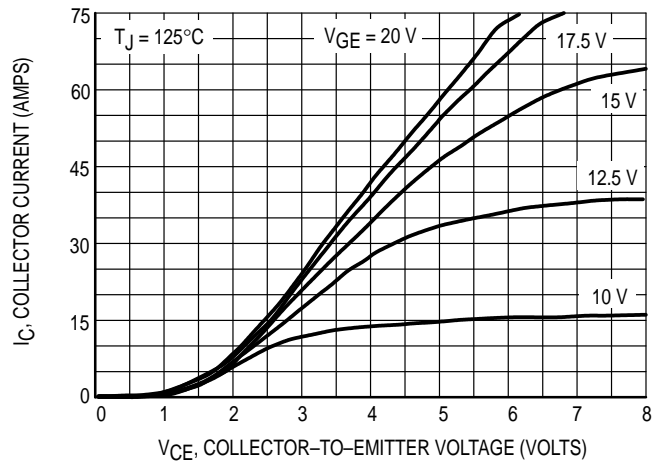


Figure 2. Output Characteristics

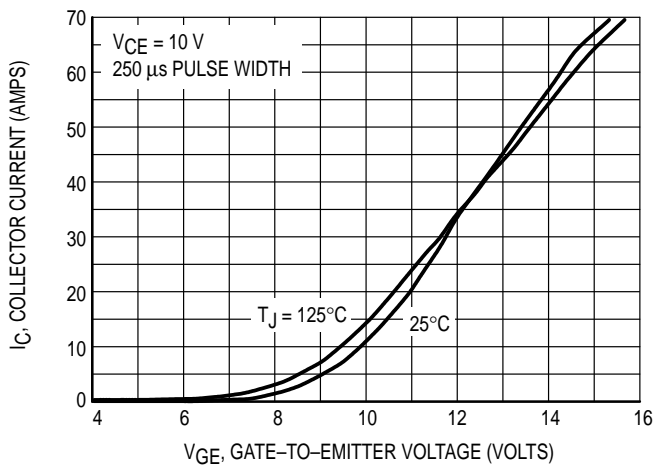


Figure 3. Transfer Characteristics

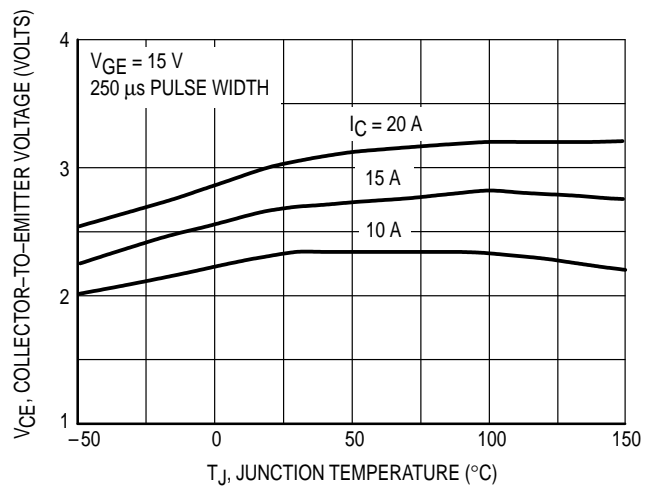


Figure 4. Collector-to-Emitter Saturation Voltage versus Junction Temperature

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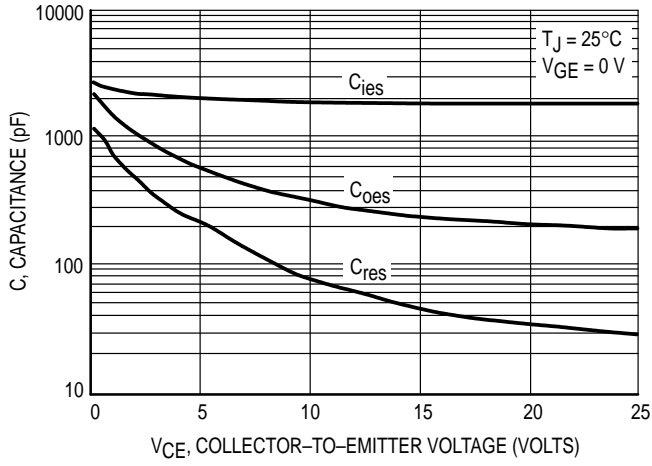


Figure 5. Capacitance Variation

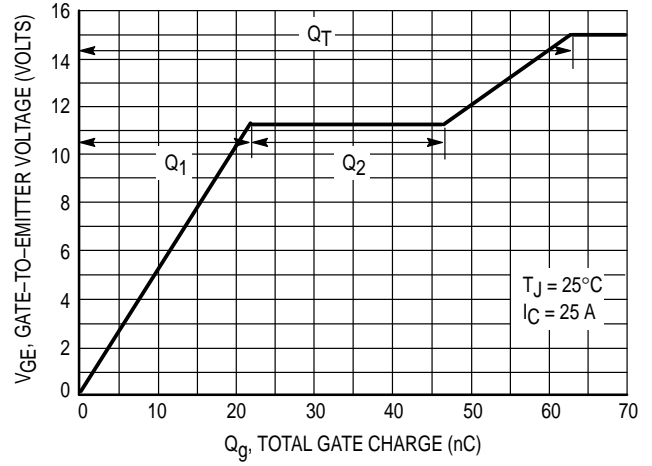


Figure 6. Gate-to-Emitter Voltage versus Total Charge

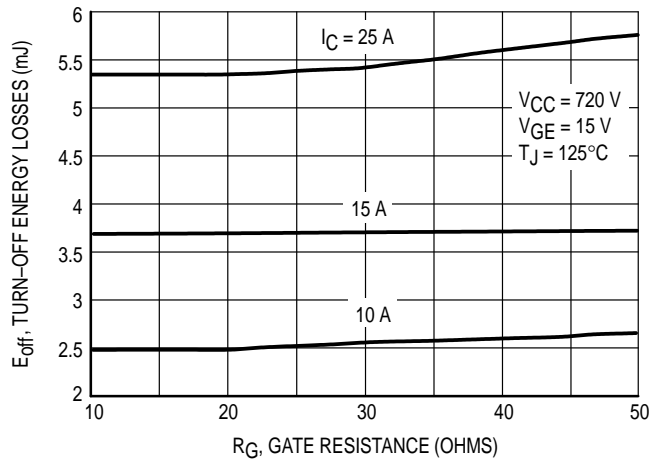


Figure 7. Turn-Off Losses versus Gate Resistance

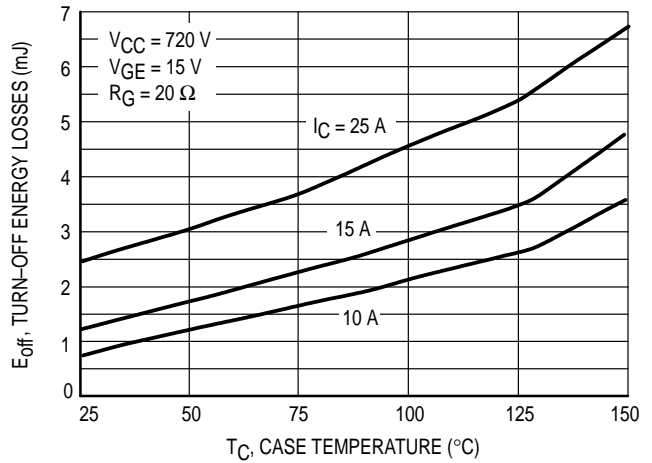


Figure 8. Turn-Off Losses versus Case Temperature

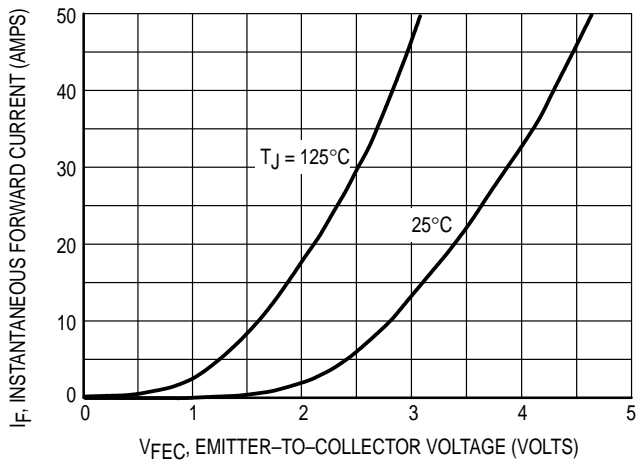


Figure 9. Diode Forward Voltage Drop

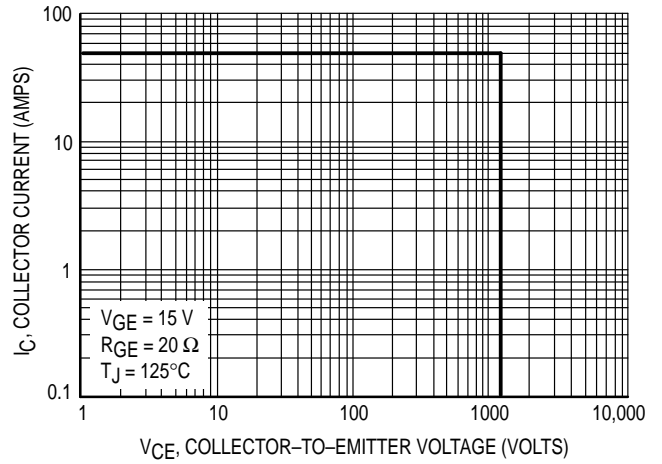


Figure 10. Reverse Biased Safe Operating Area

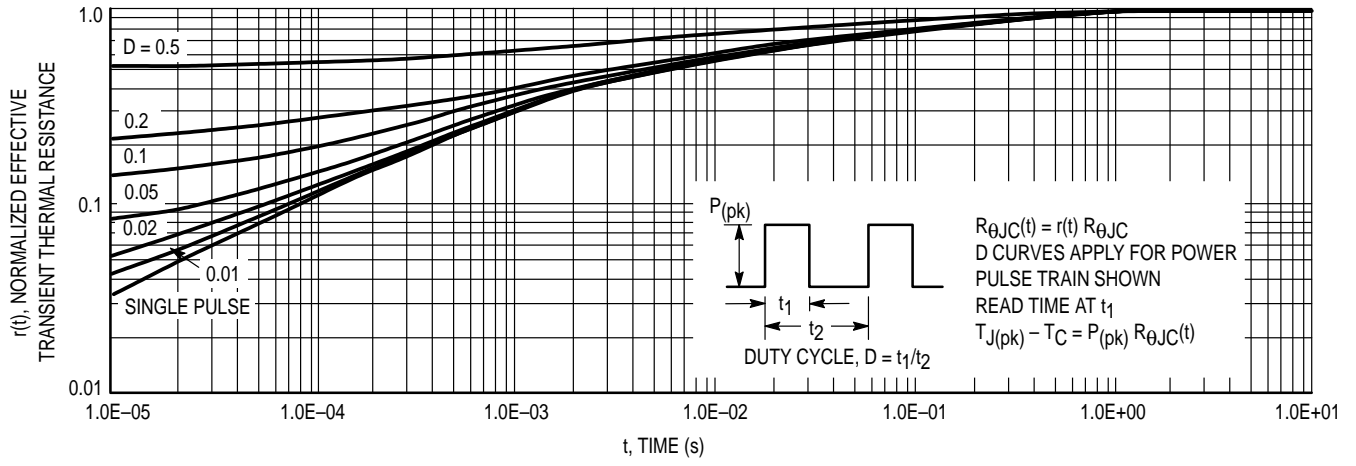
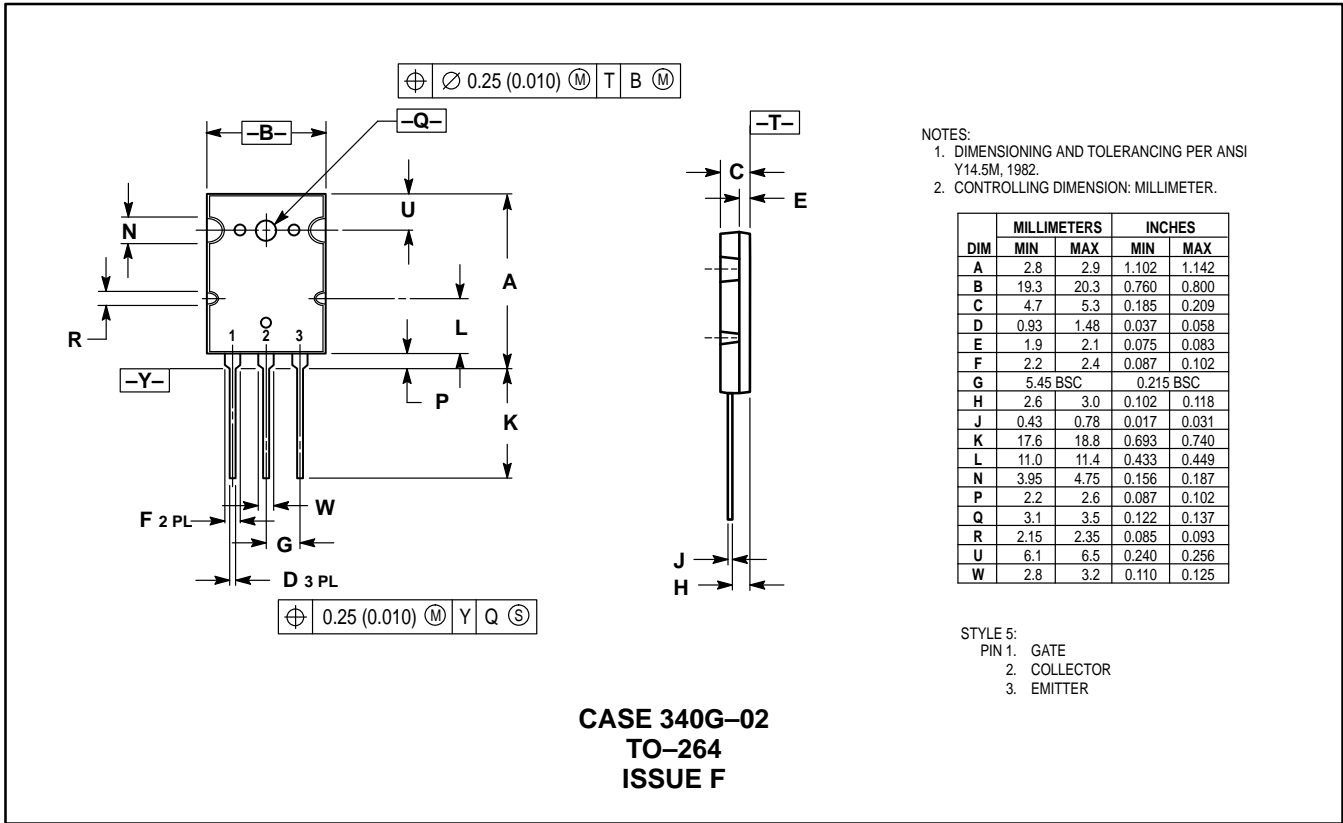


Figure 11. Thermal Response

PACKAGE DIMENSIONS



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