PDSP16488A

Single Chip 2D Convolver with Integral Line Delays

Advance Information

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The PDSP16488A is a fully integrated, application specific, image processing device. It performs a two dimensional convolution between the pixels within a video window and a set of stored coefficients. An internal multiplier accumulator array can be multi-cycled at double or quadruple the pixel clock rate. This then gives the window size options listed in Table 1.

An internal 32kbit RAM can be configured to provide either four or eight line delays. The length of each delay can be programmed to the users requirement, up to a maximum of 1024 pixels per line. The line delays are arranged in two groups,which may be internally connected in series or may be configured to accept separate pixel inputs. This allows interlaced video or frame to frame operations to be supported.

The 8-bit coefficients are also stored internally and can be downloaded from a host computer or from an EPROM. No additional logic is required to support the EPROM and a single device can support up to 16 convolvers.

The PDSP16488A contains an expansion adder and delay network which allows several devices to be cascaded. Convolvers with larger windows can then be fabricated as shown in Table 2.

Intermediate 32-bit precision is provided to avoid any danger of overflow, but the final result will not normally occupy all bits. The PDSP16488A thus provides a gain control block in the output path, which allows the user to align the result to the most significant end of the 32-bit word.

Pixel size	Window size		Maximum pixel rate (MHz)	Line delays
	Width	Depth		
8	4	4	20	431024
8	8	4	20	431024
8	8	8	10	83512
16	4	4	20	43512
16	8	4	10	43512

Table 1 Single PDSP16488A configurations

Max. pixel rate (MHz)	Pixel size	No. of PDSP16488As for N3N window size						
		3 3 3	5 3 5	7 3 7	9 3 9	11 3 11	15 3 15	23 3 23
10	8	1	1	1	4	4	4	9
10	16	1	2	2	-	-	-	-
20	8	1	2	2	6	6	8	-
20	16	1	4	4	-	-	-	-
40	8	1	4*	4*	-	-	-	-
40	16	2	-	-	-	-	-	-
*Maximum rate is limited to 30MHz by line store expansion delays								

Table 2 PDSP16488As needed to implement typical window sizes

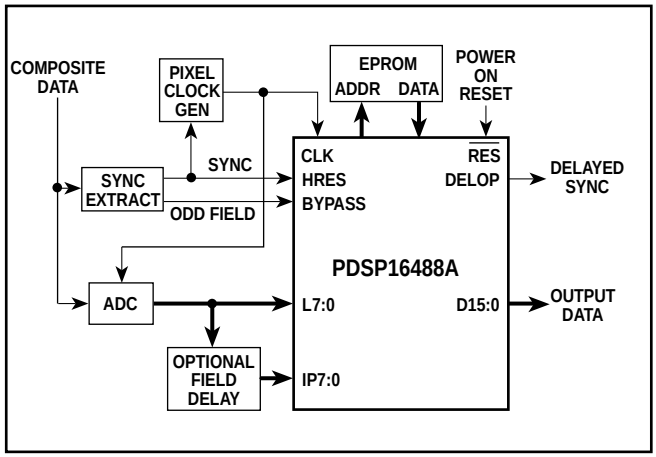


Fig. 1 Typical stand-alone real time system

FEATURES

- The PDSP16488A is a replacement for the PDSP16488 (see Note below)
- 8 or 16-bit Pixels with rates up to 40 MHz
- Window Sizes up to 838 with a Single Device
- Eight Internal Line Delays
- Supports Interlace and Frame-to-Frame Operations
- Coefficients Supplied from an EPROM or Remote Host
- Expandable in both X and Y for Larger Windows
- Gain Control and Pixel Output Manipulation
- 84-pin PGA or 132-pin QFP Package Options

Note: *PDSP16488A devices are not guaranteed to cascade with PDSP16488 devices. Zarlink Semiconductor do not recommend that PDSP16488A be mixed with PDSP16488 devices in a single equipment design. The PDSP16488A requires external pullup resistors in EPROM Mode (see Static Electrical Characteristics).*

ORDERING INFORMATION

Commercial (0°C to 170°C)
PDSP16488A / C0 / AC (PGA)
Industrial (240°C to 185°C)
PDSP16488A / B0 / AC (PGA)
PDSP16488A / B0 / GC (QFP)
Military (255°C to 1125°C)
PDSP16488A / A0 / AC (PGA)
PDSP16488A / A0 / GC (QFP)
PDSP16488A / MA / ACBR (PGA) MIL-STD-883 Class B*
PDSP16488A / MA / GCPR (QFP) MIL-STD-883 Class B*
**See Notes following Static Electrical CharacteristicsTable*

Signal	Type	Description
IP7:0	Input	Pixel data input to the first line delay (most significant byte in 16-bit mode).
L7:0	I/O	Pixel data input to the second group of line delays. (least significant byte in 16-bit mode). Alternatively an output from the last line delay when the appropriate mode bit is set.
BYPASS	Input	The first line delay in the first group is bypassed when this input is high. No internal pullup resistor.
HRES	Input	Resets the line delay address pointers when high. Normally the composite sync signal in real time applications. In non real time systems it defines a frame store update period, when low.
X15:0	Dual function	Address/data connections from a Master or Single device to the external coefficient source, with X15 defining EPROM or Host support. Otherwise they provide the expansion data input.
D15:0	Output	Signed 16-bit scaled data or multiplexed 32-bit intermediate data. During intermediate transfers the most significant half is valid when the clock is low, and the least significant half when clock is high.
$\overline{PC1}$	Output	During programming a Master device outputs a timing strobe on this pin. This is passed down the chain in a multiple device system, using the $\overline{PC0}$ input on the next device.
$\overline{PC0}$	Input	This pin is used in conjunction with $\overline{PC1}$ in multiple device systems. It terminates the write strobe from a Master device which is EPROM supported.
DELOP	Output	This output provides a version of the HRES input which has been delayed by an amount defined by the user.
$\overline{DS}$	I/O	The data strobe from a host computer, active low. This pin will be an output from an EPROM supported Master device which provides strobes to the remaining devices.
$\overline{CE}$	Input	An active low enable which is internally gated with R/$\overline{W}$ and $\overline{DS}$ to perform reads or writes to the internal registers. In a Single or Master device, which is supported from an EPROM, the bottom 72 addresses are always used and $\overline{CE}$ is not needed. $\overline{CE}$ can then be used to initiate a new register load sequence after the power on load sequence.
R/$\overline{W}$	Input	Read / not write line from the host CPU. When an EPROM is used this pin should be tied low.
$\overline{PROG}$	I/O	This pin is normally an input which signifies that registers are to be changed or examined. It is, however, an output from an EPROM supported Single or Master device indicating to the rest of the system that registers are being updated.
CLK	Input	Clock. All events are triggered on the rising edge of CLK, except the latching of least significant expansion inputs . Internally the clock can be multiplied by two or four in order to increase the effective number of multipliers.
BIN	Output	This output indicates the result from the internal comparison. A high value indicates that the pixel was greater than the internal threshold. The output is only valid from the last device in a chain.
OVR	Output	When high this output indicates that there has been a gain control overflow.
$\overline{RES}$	Input	Active low power on reset signal.
$\overline{SINGLE}$	Input	Tied to ground to indicate a Single device system. Internal pullup resistor.
$\overline{MASTER}$	Input	Tied to ground to indicate the Master device in a multiple device system. Must be left open circuit in a Single device system. Internal pullup resistor.
$\overline{OEN}$	Input	Output enable signal. Active low.
CS3:0	Outputs	Four address bits from a Master specifying one of sixteen devices in a multiple device system. Must be externally decoded to provide chip enables for the additional devices.
F1:0	Outputs	These bits indicate the field selection given by the gain control auto select logic. The same coding as that used for Control Register bits C5:4 is used.
V_{DD}	Power	15V supply. All V_{DD} pins must be connected.
GND	Power	0V supply. All GND pins must be connected.

Table 3 Signal descriptions

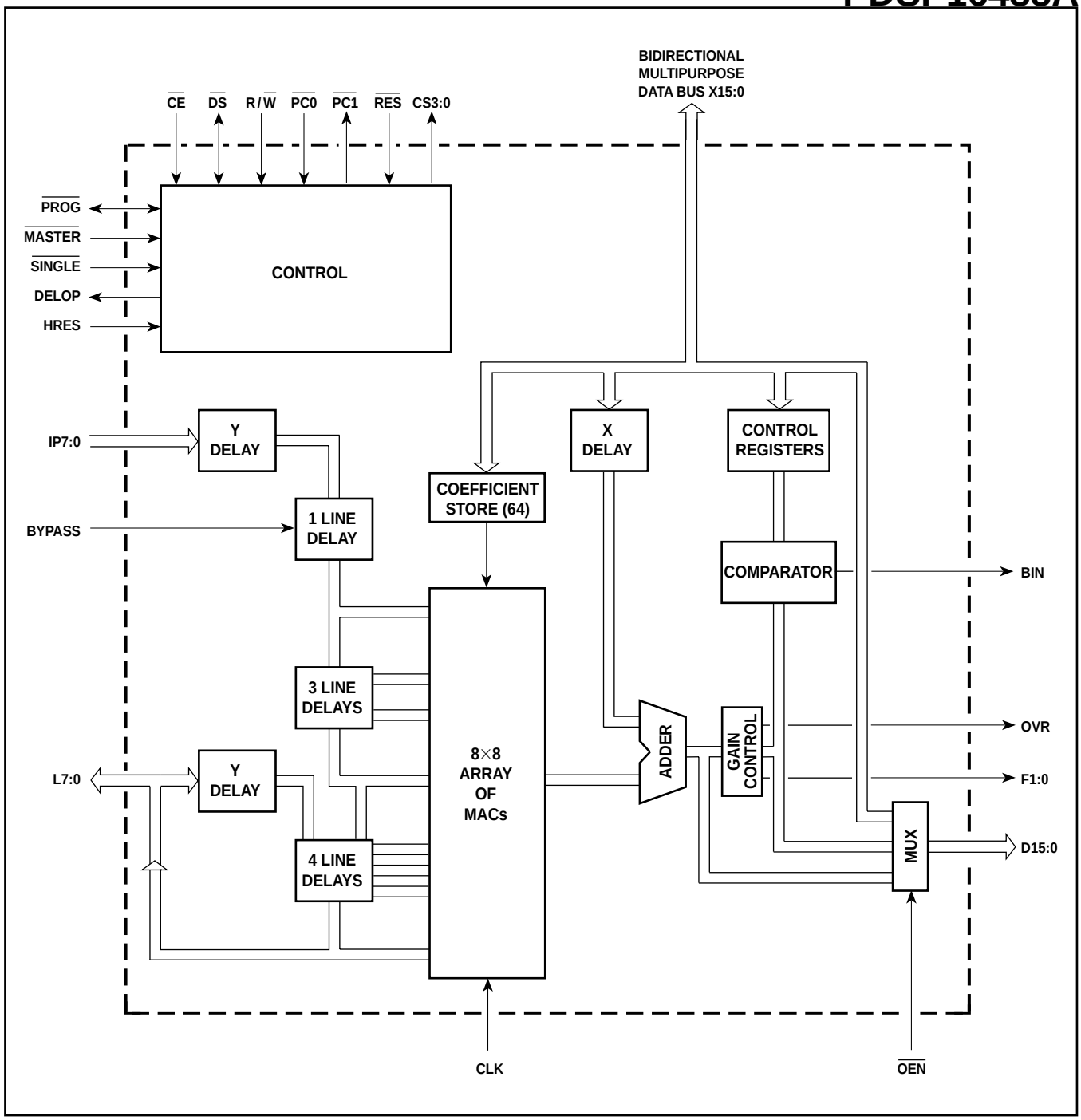


Fig. 2 Functional block diagram

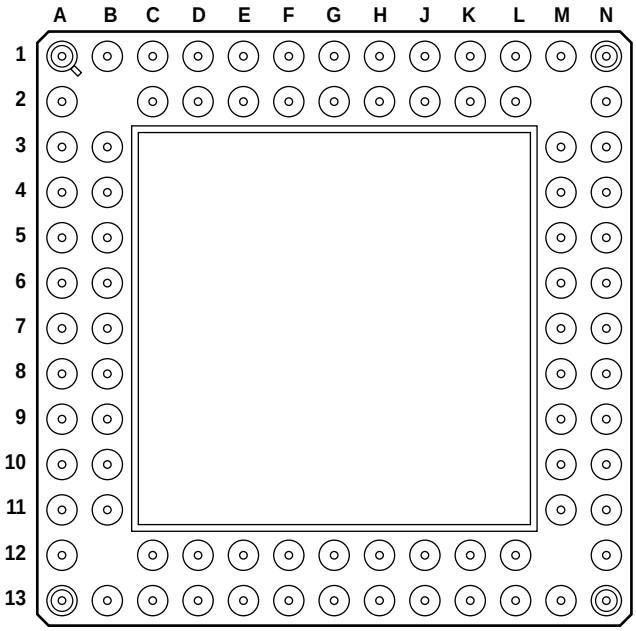


Fig. 3a Pin connections for 84 I/O pin grid array package - AC84 (Power) (bottom view)

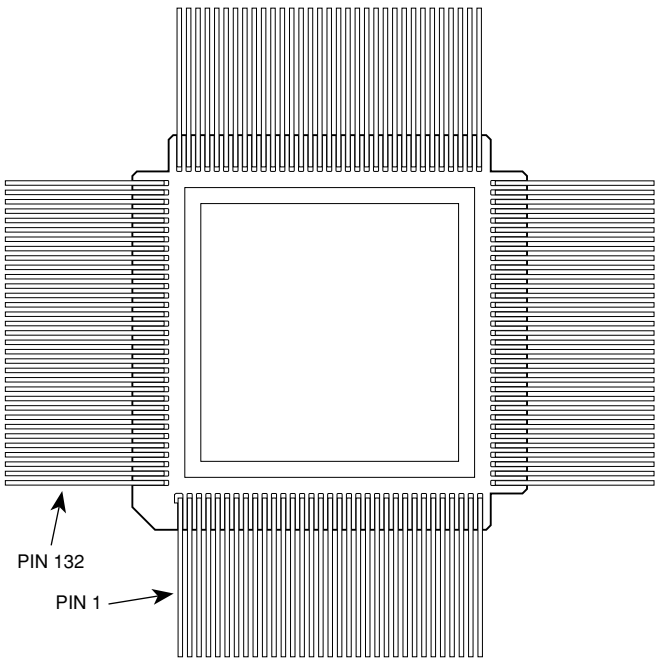


Fig 3b Pin connections for 132 I/O ceramic power flatpack - GC132 (Power) (top view)

Fig 3 Pin connection diagrams (not to scale). See Table 3 for signal descriptions and Tables 4 and 5 for pinouts.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	L0	L2	IP2	M10	X5	E12	HRES	B6	D10
B1	F1	M1	IP1	N11	X4	D13	OVR	A5	D11
C2	L1	N1	IP0	M11	X3	D12	$\overline{PC1}$	B5	N/C
C1	L2	N2	BYPASS	N12	X2	C13	BIN	A4	D12
D2	L3	M3	X15	N13	X1	C12	$\overline{OEN}$	B4	D13
D1	N/C	N3	X14	M13	X0	B13	D0	A3	D14
E2	L4	M4	X13	L12	DELOP	A13	D1	B3	D15
E1	L5	N4	N/C	L13	$\overline{PC0}$	A12	D2	A2	F0
F2	L6	M5	$\overline{SINGLE}$	K12	$\overline{RES}$	B11	D3	F1	V_{DD} 1
G2	L7	N5	X12	K13	CS0	A11	D4	N6	V_{DD} 2
G1	IP7	M6	X11	J12	CS1	B10	D5	F13	V_{DD} 3
H2	N/C	M7	$\overline{MASTER}$	J13	CS2	A10	D6	A6	V_{DD} 4
J1	IP6	N7	X10	H12	CS3	B9	D7	H1	GND1
J2	IP5	M8	X9	G12	$\overline{PROG}$	A9	D8	N8	GND2
K1	IP4	N9	X8	G13	$\overline{DS}$	B8	CLK	H13	GND3
K2	N/C	M9	X7	F12	$\overline{CE}$	B7	N/C	A8	GND4
L1	IP3	N10	X6	E13	R/$\overline{W}$	A7	D9		

Table 4 Pin connections for AC84 (power) package. See Fig. 3a.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	N/C	34	N/C	67	N/C	100	N/C
2	D0	35	X2	68	IP1	101	V_{DD}
3	$\overline{OEN}$	36	X3	69	GND	102	F0
4	BIN	37	X4	70	IP2	103	D15
5	$\overline{PC1}$	38	N/C	71	N/C	104	N/C
6	V_{DD}	39	X5	72	V_{DD}	105	D14
7	GND	40	GND	73	IP3	106	D13
8	OVR	41	X6	74	V_{DD}	107	GND
9	N/C	42	X7	75	IP4	108	D12
10	HRES	43	N/C	76	GND	109	GND
11	R/$\overline{W}$	44	X8	77	IP5	110	V_{DD}
12	$\overline{CE}$	45	X9	78	GND	111	V_{DD}
13	N/C	46	V_{DD}	79	IP6	112	D11
14	N/C	47	V_{DD}	80	V_{DD}	113	D10
15	GND	48	V_{DD}	81	IP7	114	D9
16	N/C	49	X10	82	V_{DD}	115	GND
17	$\overline{DS}$	50	$\overline{MASTER}$	83	N/C	116	CLK
18	GND	51	N/C	84	L7	117	CLK
19	V_{DD}	52	X11	85	GND	118	CLK
20	$\overline{PROG}$	53	X12	86	L6	119	GND
21	GND	54	$\overline{SINGLE}$	87	GND	120	GND
22	CS3	55	GND	88	L5	121	D8
23	CS2	56	GND	89	V_{DD}	122	V_{DD}
24	CS1	57	N/C	90	L4	123	D7
25	CS0	58	X13	91	V_{DD}	124	D6
26	V_{DD}	59	X14	92	L3	125	D5
27	$\overline{RES}$	60	N/C	93	V_{DD}	126	D4
28	$\overline{PC0}$	61	X15	94	L2	127	GND
29	N/C	62	V_{DD}	95	GND	128	D3
30	DELOP	63	BYPASS	96	L1	129	N/C
31	X0	64	IP0	97	F1	130	D2
32	X1	65	V_{DD}	98	L0	131	D1
33	N/C	66	N/C	99	N/C	132	N/C

Table 5 Pin connections for GC132 (power) package. See Fig 3b.

BASIC OPERATION

The PDSP16488A convolver performs a weighted sum of all the pixels within an N3N two dimensional window. Each pixel value is multiplied by a signed coefficient, or weight, and the products are summed together. In practice positive weights would be used to produce averaging effects, with various distribution laws, and negative weights would be used for edge enhancement. The window is moved continuously over the video frame, and for real time operation a new result must be obtained for every pixel clock. In most applications odd sized windows will be used, resulting in a centre pixel whose value is modified by the surrounding pixels.

Output Accuracy

With 8 bit pixels, and an 838 window, it is possible for the accumulated sum to grow to 22 bits within a single device. With 16-bit pixels, and an 834 window (the maximum possible), the sum can grow to 29 bits. The PDSP16488A actually allows for word growth up to 32 bits, and thus allows several devices to be cascaded without any danger of overflow. Since coefficients can be negative, the final result is a 32-bit signed two's complement number.

In a particular application the desired output will lie somewhere within these 32 bits, the actual position being dependent on the coefficient values used. This causes problems in physically choosing which output pins to connect to the rest of the system. To overcome this problem the PDSP16488A contains a gain control block, which allows the final result to be aligned to the most significant end of the 32-bit internal result. The provision of the gain control block, rather than a simple shifter, allows the gain to be defined more accurately.

The sixteen most significant bits of the adjusted result are available on output pins D15:0, which contains a sign bit.

Output Saturation

If the output from the convolver is driving a display, negative pixels will give erroneous results. An option is thus provided (register bits C7:6) that forces all negative results to zero, which are then interpreted as black by the display. At the same time positive results, which overflow the gain control, are forced to saturate at the most positive number, i.e. peak white. In this mode the output sign bit is always zero,and should not be connected to an A-D converter.

A separate option forces both negative and positive overflows to saturate at their respective maximum values, but in scale negative results remain valid. A gain control overflow warning flag (OVR) is also available, which can be used in a host CPU supported system to change the gain parameters if overflows are not acceptable.

Binary Output

The PDSP16488A contains a 16-bit arithmetic comparator which allows the output from the gain control block to be compared with a previously programmed value. An output flag allows the user to detemine if the result was above or below a value contained within an internal register.

Multiplier Array

The PDSP16488A contains sixteen 838 multipliers each producing a 16-bit result. Internally the pixel clock supplied by the user can be multiplied by two or four, which together with the proprietary architecture, allows each multiplier to be used several times within a pixel clock period. This increases the effective number of multipliers, which are available to the user, from 16 to 32 or 64 respectively. This architecture produces a very efficient utilization of chip area, and allows the line delays to be accommodated on the same device.

The sixteen multipliers are arranged in a 4 deep by 4 wide array, resulting in effective arrays of 4 by 8 or 8 by 8 with the multicycling options. The multiplier array can also be configured to handle 16-bit signed pixels; the effective number of available multipliers is then halved.

Line Delay Operation

Internal RAM is arranged in two separate groups, and can be configured to provide line delays to match the chosen size of the convolver. When a four deep arrangement is used, with 8-bit pixels, four line delays are available, and each can be programmed to contain up to 1024 pixels. In an eight deep array, or if 16-bit pixels are needed, each line can contain up to 512 pixels. Fig. 4 illustrates the options available.

The first line delay in one of the groups can optionally be switched in or out under the control of an input pin. It is used to delay the pixel input when data is obtained from another convolver in a multiple device system, or it is used to support interlaced video.

Signals L7:0 may be used as pixel inputs or outputs. They are configured as inputs at power-on to avoid possible bus conflicts, but by setting a mode control bit can become outputs. They can then be used to drive another device when multiple PDSP16488As are required.

Interlaced Video

When using real time interlaced video, a picture or frame is composed from two fields, with odd lines in one field and even lines in the other. An external field delay is thus required to gather information from adjacent lines, and the convolver needs two input buses. The bus providing the delayed pixels has an extra internal line delay. This is only used in the field containing the upper line in any pair of lines, and must be bypassed in the other field. It ensures that data from the previous field always corresponds to the line above the present active line, and avoids the need to change the position of the coefficients from one field to the next.

Fig. 5 shows the translation from physical to internal line positions, for single device interlaced systems. Line N is the line presently being convolved, which is either one or two lines previous to the line presently being produced.

When windows requiring four or more lines are to be implemented, the first line delay, in the group supplied from the L7:0 pins, must always be bypassed. This bypass option is controlled by register B, bit 7 and is not effected by the BYPASS input pin.. The coefficients must be loaded into the locations shown, which match the translated line positions, with unused coefficients, shown shaded, loaded with zeros.

Defining the Length of the Line Delay

Fig. 5 defines the maximum line lengths available in each of the window size options. The actual line lengths can be defined in one of three ways, to support both real time applications, taking pixels directly from a camera, and also use in systems supported by a frame store. In the former case the line delays must be referenced to video synchronization pulses. In the latter case the line lengths are well defined, and the horizontal flyback 'dead times' will have been removed.

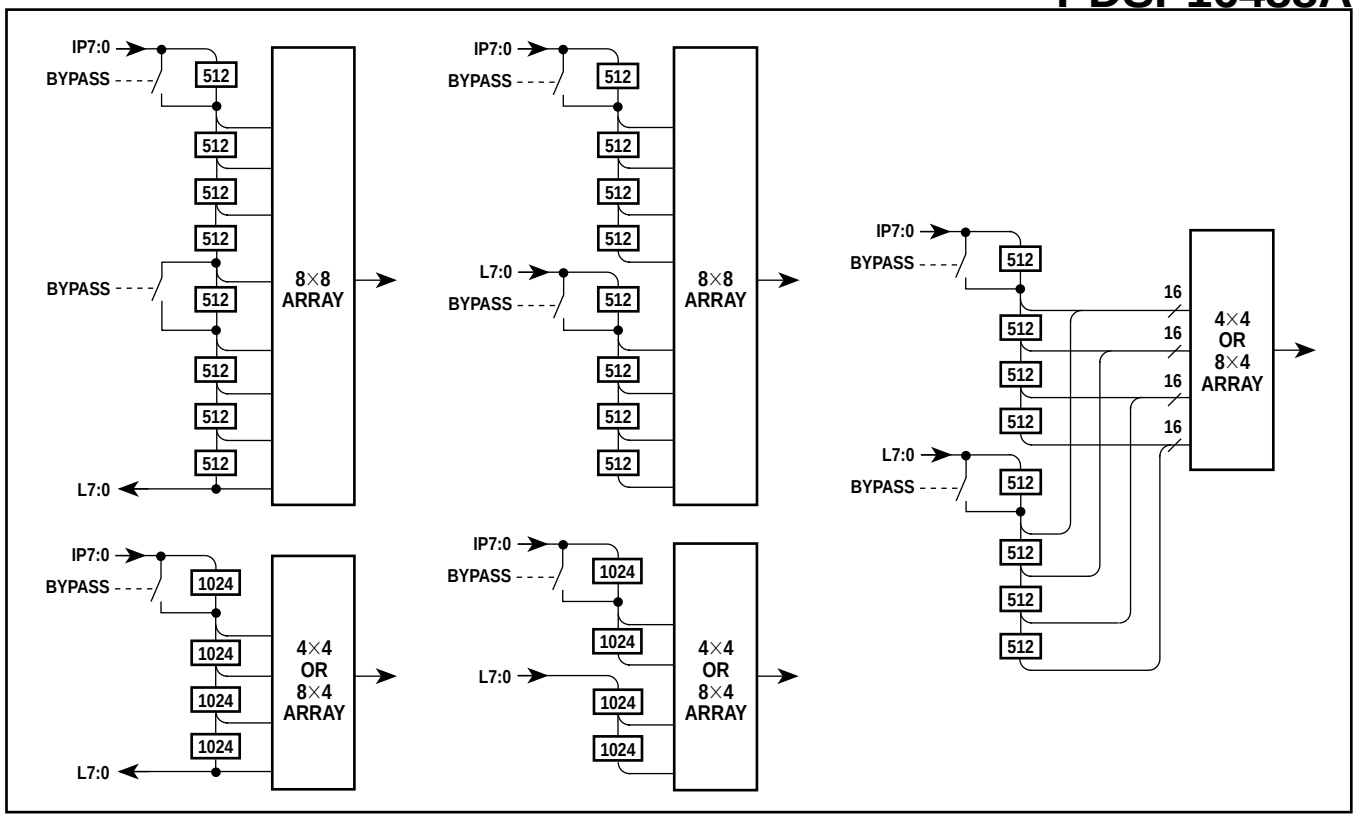


Fig. 4 Line delay configurations

To support real time applications an option is provided in which the length of the line delay is defined by the number of clocks obtained while the HRES input is low. HRES would normally be composite sync when the convolver is directly attached to an NTSC or PAL video input.

The line delay is achieved by reading the previous contents of a RAM-based line store, and then writing new information to the same address. When HRES is high, write operations are inhibited, and the address counter is reset. During an active line the counter is incremented by the pixel clock. If the maximum count is reached before the end of a line, then write operations are terminated and wraparound effects avoided.

The rising edge of HRES, marking the end of a line, is normally asynchronous to the pixel clock, and it is possible for an additional pixel to be stored on some lines. This has no effect on the convolver operation, and will not cause a cumulative shift in the pixel position from line to line.

An alternative means of defining the line length is, however, provided when an exact number of pixels is needed. HRES going low then starts the delay operation for every line, but it ceases when the 10-bit value contained in two registers is reached. This method can avoid the need to store blank pixels at the end of a line before HRES goes high. With this method the line must contain an even number of pixels but the value loaded into the control registers, defining the line length, must be one less than the even number required.

In an image processing system, the pixel clock is often re-synchronized, or even inhibited, during blanking or sync. The next line is then started with a precise time interval from the end of sync (falling edge of HRES) to the first pixel clock edge. This avoids any visible pixel jitter at the beginning of the line, which would otherwise be present since pixel clock is asynchronous with respect to video sync pulses.

When using the PDSP16488A the pixel clock should not be inhibited, or re-synchronized, until the delayed version of the HRES input goes active. This is present on the DELOP output pin. This will ensure that no pixels on the right hand edge are lost due to the internal pipeline delay. If the pixel clock is a continuous signal, the user must ensure that the HRES high to low transition meets the timing requirements defined in Fig. 10. The HRES rising edge at the end of a line need not be synchronized.

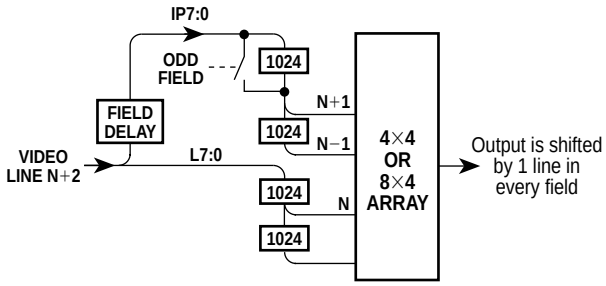
When pixels are read or written to a frame store, an alternative line delay configuration is needed. Within the frame store lines would be stored in contiguous locations, with no gaps caused by the flyback period between the lines. This method of use makes the HRES defined line delay operation difficult to use, and an alternative mode of operation is provided. The HRES input is then driven by a system-provided signal, which defines a complete frame store update period. It is not a line defining signal. The high to low transition of this signal will initiate the line store update sequence and allow the internal address pointers to increment. These pointers will be synchronously reset at the end of a line, when they reach the pre-programmed value. They will then immediately start a new operation using address zero. The actual line delay must be pre-loaded into two control registers as described previously.

Write operations back to the frame store must allow for the total pipeline delay. This can be achieved by inhibiting write operations until DELOP goes low. Write operations then continue until it goes back high. The PDSP16488A assumes that data is valid when a clock signal is applied, and that it also meets the set up and hold requirements given in Fig. 10. If data is not valid due, for example, to a frame store DRAM refresh cycle, then the user must externally inhibit the clock. The clock supplied to the convolver will in this mode be a signal which defines a frame store cycle time.

The use of the convolver in a line scan system is similar to its use with a frame store. These systems have no flyback period, and the address counter must be synchronously reset at the end of the line and then allowed to continue.

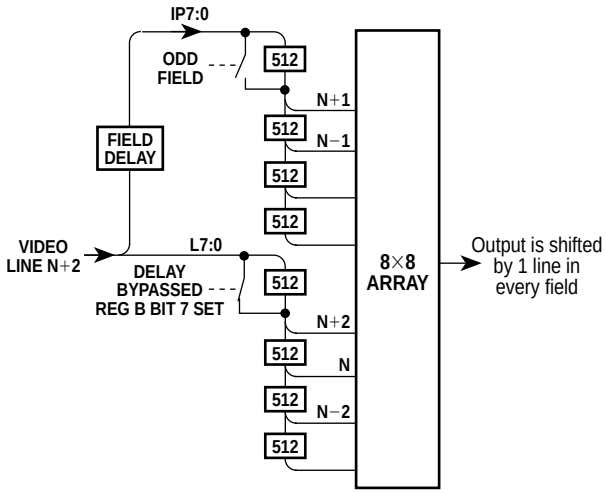
3×3 WINDOW

LINE N−1	C4	C5	C6	
LINE N	C8	C9	C10	
LINE N+1	C0	C1	C2	



5×5 WINDOW

LINE N−2	C48	C49	C50	C51	C52			
LINE N−1	C8	C9	C10	C11	C12			
LINE N	C40	C41	C42	C43	C44			
LINE N+1	C0	C1	C2	C3	C4			
LINE N+2	C32	C33	C34	C35	C36			



8×8 WINDOW

LINE N−3	C24	C25	C26	C27	C28	C29	C30	C31
LINE N−2	C56	C57	C58	C59	C60	C61	C62	C63
LINE N−1	C16	C17	C18	C19	C20	C21	C22	C23
LINE N	C48	C49	C50	C51	C52	C53	C54	C55
LINE N+1	C8	C9	C10	C11	C12	C13	C14	C15
LINE N+2	C40	C41	C42	C43	C44	C45	C46	C47
LINE N+3	C0	C1	C2	C3	C4	C5	C6	C7
LINE N+4	C32	C33	C34	C35	C36	C37	C38	C39

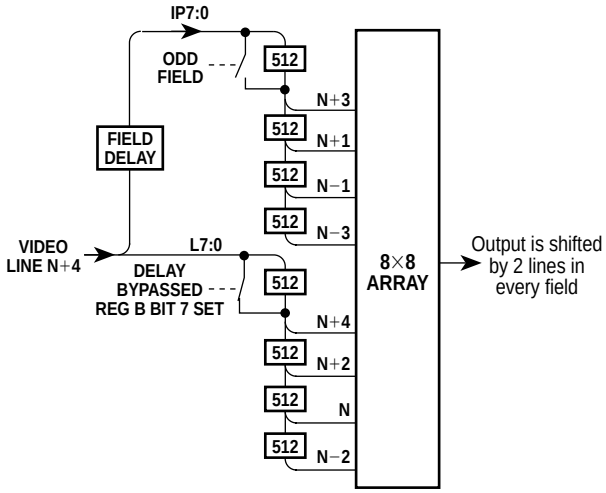


Fig. 5 Line delay allocations in SINGLE device interlaced systems

Gain Control Block

This block is provided as an aid to locating the bits of interest in the 32-bit internal result. The magnitude of the largest convolved output will depend on the size of the window, and the coefficient values used. The function of the gain control block is then to produce an output, which is accurate to 16 bits, and which is aligned to the most significant end of this 32-bit word. The sixteen most significant bits of the word are available on D15:0 and the largest number need only have one sign bit if the gain control is correctly adjusted.

Fig. 6 indicates the mechanism employed with the required function implemented in two steps. Two mode control bits, register C, bits 5:4, allow one of four 20 bit fields to be selected from the final 32-bit value. These four fields are positioned with the first at the most significant end, and then at four bit displacements down to the least significant end.

By setting an enabling bit, register C, bit 0, the field selection can optionally be done automatically. This feature should only be used in the real time operating mode, when HRES defines video lines. Internal logic examines the most significant 13, 9, or 5 bits from the 32-bit result, and makes a field selection dependent on which group does not contain identical sign bits. If less than five sign bits are obtained, the logic will select the field containing the most significant 20 bits. The selection is indicated by F1:0.

The automatic field selection is particularly useful when a fixed scene is being processed. The selection is reset when any internal register is updated (i.e. $\overline{\text{PROG}}$ has been low) and is then held high for ten further occurrences of the HRES input. This allows the internal multiplier/accumulator array to be completely flushed before a field selection is made. As convolver outputs of greater magnitude are produced the field selection logic will respond by selecting a more significant field. The most significant field found necessary remains selected until $\overline{\text{PROG}}$ again goes low. Even if the automatic field selection is not enabled, F1:0 will still indicate which field would have been selected. These are coded in the same way as register C, bits 5:4.

Having chosen a field, either manually or automatically, it is then multiplied by a 4-bit unsigned integer. This is contained within the user-programmed gain control register, and the multiplication will produce a 24-bit result . The middle 16 bits of this result contain the required output bits. The gain control multiplier can overflow in to the unused most significant four bits if the parameters are chosen wrongly. This condition is flagged by pin OVR.

By setting appropriate mode control bits, further manipulation of the gain control output is possible. One option, register C, bits 7:6 = 11, allows all negative outputs to be forced to zero, and at the same time positive gain control overflows will saturate at the maximum positive number. Register C, bits 7:6 = 10 will saturate positive and negative overflows at their respective maximum values, but otherwise leaves them unchanged. Occasional overflows can be tolerated in some systems, and this option prevents any gross errors.

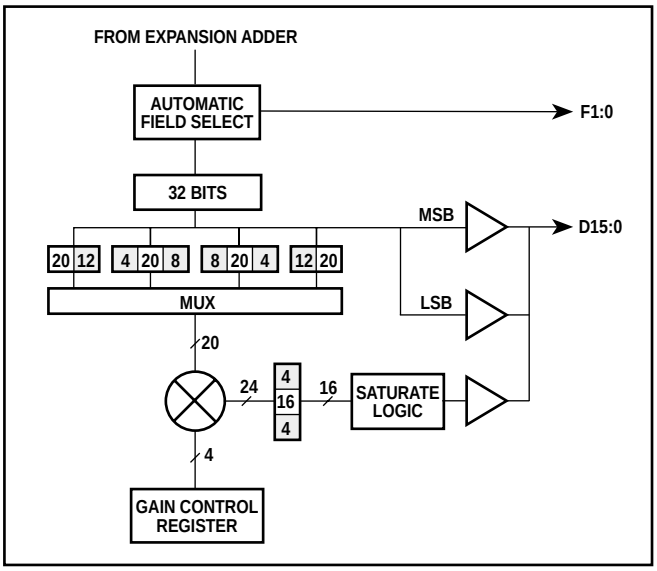


Fig. 6 Gain control block

Expansion

Multiple devices can be connected in cascade in order to obtain window sizes larger than those provided by a single PDSP16488A. This requires an additional adder in each device which is fed from expansion data inputs. This adder is not used by a Single device or the first device in a cascaded system, and is enabled or disabled by register B, bit 4.

The first device in the cascaded system must be designated as a Master device by $\overline{\text{MASTER}}$ tying low. Its expansion input bus is then used as the source of data for the coefficient and control registers in all devices in the system.

In order to reduce the pin count required for 32-bit buses, both expansion in and data out are time-multiplexed with the phases of the pixel clock. When the clock is high the least significant half will be valid, and when the clock is low the most significant half will be valid.

In practice this multiplexing is only possible with pixel clocks up to 20MHz. Above these frequencies the multiplexing must be inhibited by setting register A, bit 7. The intermediate data accuracy will then be reduced, since only the lower 16 bits of the internal 32-bit intermediate sum are available on the D15:0 output pins. In such systems the coefficients must be scaled down in order to keep the intermediate and final results down to 16 bits. The final device should not use the gain control block but instead should simply output the non-multiplexed 16-bit result. The OVR flag and pixel saturation options will not be available.

Pixel Input and Output Delays

In a real time system, when line delays are referenced to video sync pulses present on the HRES input, the first pixel from the last line delay does not appear on the L7:0 pins until the fifth active pixel clock edge after HRES has gone low. This is illustrated in Fig. 8. In a vertically expanded system, this output provides the input to the first line delays in the vertically displaced devices. The internal logic is thus designed to always expect this five clock delay. Compensation must thus be applied to the devices which are directly connected to the video source, such that the first pixel is not valid until the fifth clock rising edge.

For this reason the PDSP16488A contains an optional four clock pipeline delay on each of the pixel data inputs, as shown in Fig. 7. When the delay is used the first pixel in a video line must be available on the input pins after the first pixel clock edge. This would be so if the device were connected to an A-D converter, since that would introduce a one pixel pipeline delay. If the system introduces any further external pipeline delays, then the internal delay should be bypassed, and the user should ensure that the first pixel is valid after the fifth clock edge.

The use of this four clock delay is controlled by register B, bit 3. This delay is in addition to the delays which are provided to support expansion in both the X and Y directions, and are controlled by register D, bits 3:2. Both delays are in fact simply added together in the device, but are separately defined since they add delays for different system reasons.

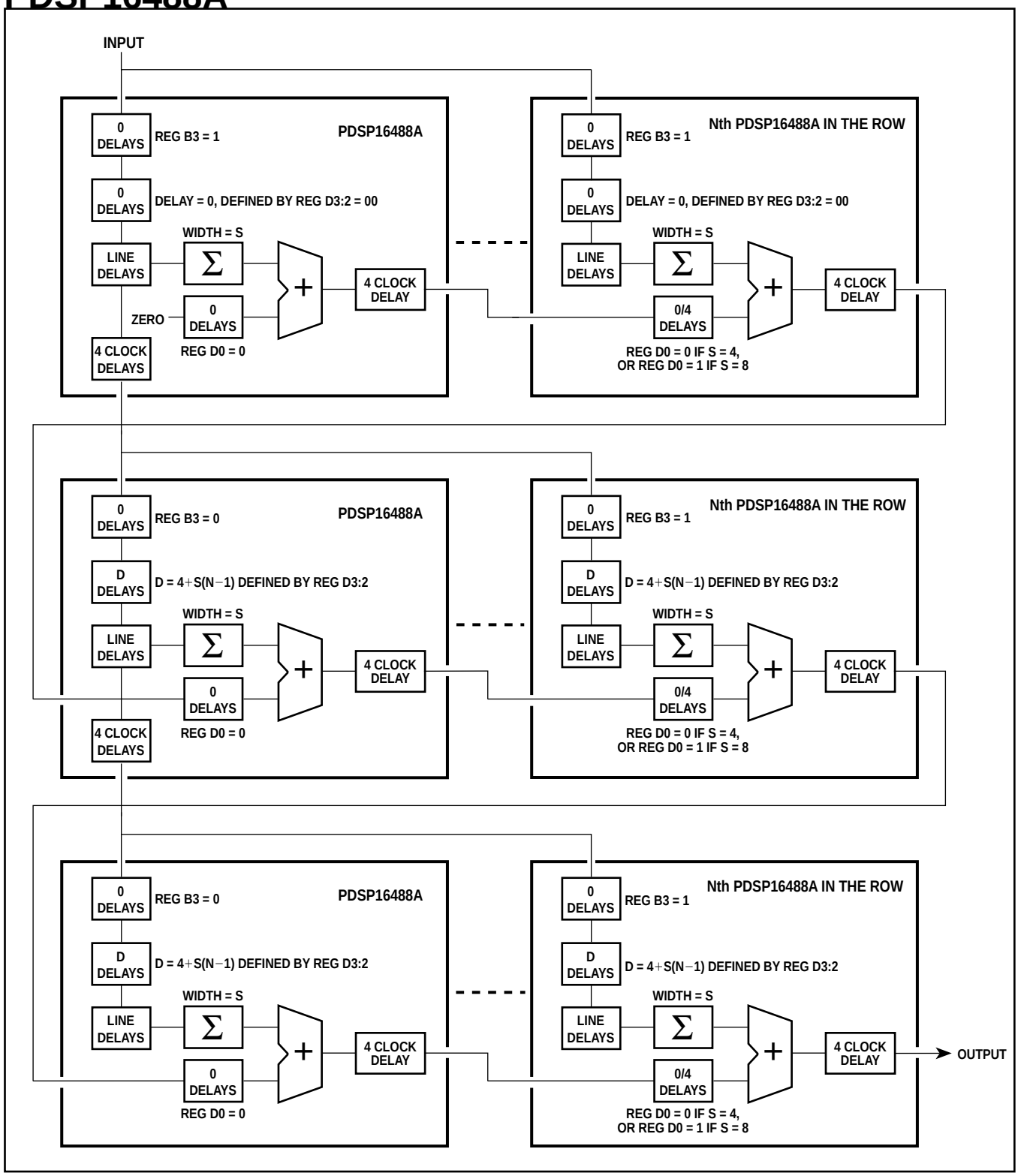


Fig. 7 Multi-device delay paths

Delay Compensation for Large Windows

A large window is composed of several partial windows each of which is implemented in an individual device. If necessary the partial window must be padded with zero coefficients to become one of the standard sizes. When constructing a large window it is necessary to delay the expansion data inputs in order to compensate for growth in the horizontal direction. Delays in the partial sums are also necessary to compensate for the total pipeline delay needed to produce the previous complete horizontal stripe.

Within each device in a horizontal stripe, apart from the first, the expansion input must be delayed by the width of the partial window, before it is added to the internal sum. Since partial windows can only be 4 or 8 pixels wide, a delay of 4 or 8 pixel clocks is needed. There is, however, an in-built delay of 4 pixels in the inter device connection, and the PDSP16488A thus only needs an option to delay the expansion input by an additional four pixels.

The data from the last device in a horizontal row of convolvers feeds the expansion input of the first device in the next row. This is shown in Fig. 7. With this arrangement, the position of the partial window as illustrated, is the inverse of its vertical position on a normal TV screen. Thus the top left hand device corresponds to the bottom left hand portion of the complete window.

The output from the last device in the row is delayed with respect to the original data input by an amount given by the formula;

DELAY = 41S(N21), where N is the number of devices in a row and S is the partial window width, i.e. 4 or 8.

The internal convolver sums, in each of the devices in the next row, must be delayed by this amount before they are added to results from the previous row. This is more conveniently achieved by delaying data going into the line stores. The required cumulative delay with respect to the first horizontal stripe is then automatically obtained when more than two rows of devices are needed.

Register D, bits 3:2 are used to define one of four delay options. These delays have been selected to support systems needing from two to eight devices and are described in the applications section.

Coefficients

Sixty-four coefficients are stored internally and must be initially loaded from an external source. Table 5 gives the coefficient addresses within a device, with coefficient C0 specified by the least significant address and C63 by the most significant address. Fig. 9 shows the physical window position within the device that is allocated to each coefficient in the various modes of operation. Horizontally the coefficient positions correspond to the convolution process as if it were observed on a viewing screen, i.e. the left hand pixel is multiplied with C0. In the vertical direction the lines of coefficients are inverted with respect to a visual screen, i.e. the line starting with C0 is actually at the bottom of the visualized window.

The coefficients may be provided from a Host CPU using conventional addressing, a read/not write line, data strobe, and a chip enable. Alternatively, in stand alone systems, an EPROM may be used. A single EPROM can support up to 16 devices with no additional hardware.

When windows are to be fabricated which are smaller than the maximum size that the device will provide in the required configuration, then the areas which are not to be used must contain zero coefficients. The pipeline delay will then be that of a completely filled window.

Function	Hex address
Mode Reg A	00
Mode Reg B	01
Mode Reg C	02
Mode Reg D	03
Comparator LSB	04
Comparator MSB	05
Scale value	06
Pixels/line LSB	07
Pixels/line MSB	08
C0-C15	40-4F
C16-C31	50-5F
C32-C47	60-6F
C48-C63	70-7F
Unused	09-3F

Table 5 Internal register addressing

Data size	Window size	Pipeline delay
8	434	34
8	834	30
8	838	26
15	434	28
16	834	26

Table 6 Pipeline delays

Total Pipeline Delay

The total pipeline delay is dependent on the device configuration and the number of devices in the system. Table 6 gives the delays obtained with the various single device configurations when the gain control is used. These delays are the internal processing delays and do not include the delays needed to move a given size window completely into a field of interest. When multiple devices are needed, additional delays are produced which must be calculated for the particular application. These delays are discussed in the applications section.

The PDSP16488A contains facilities for outputting a delayed version of HRES (DELOP) to match any processing delay. Register C. bits 3:1 allow this delay to be selected from any value between 29 and 92 pixel clocks as detailed in Table 9.

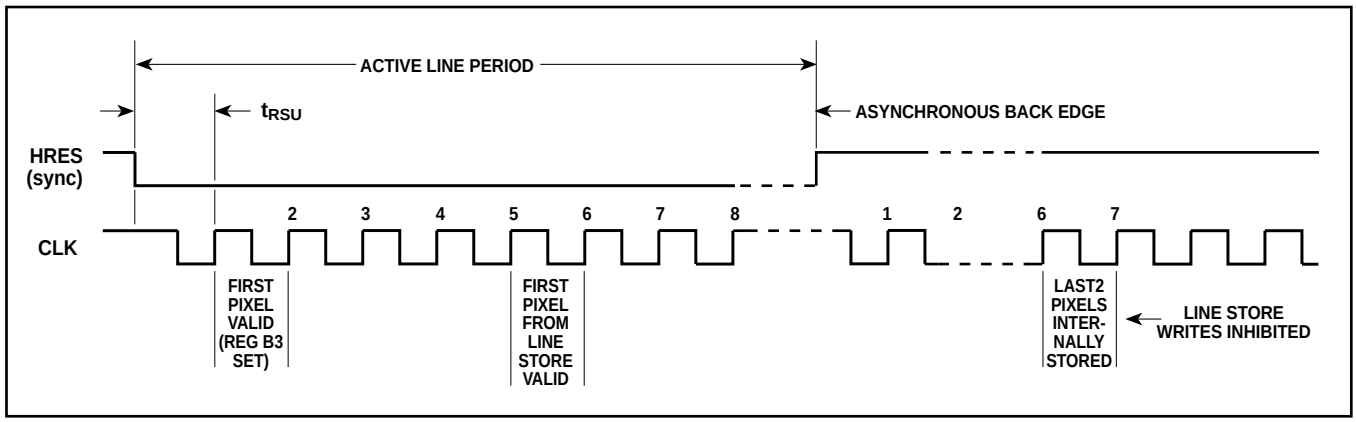
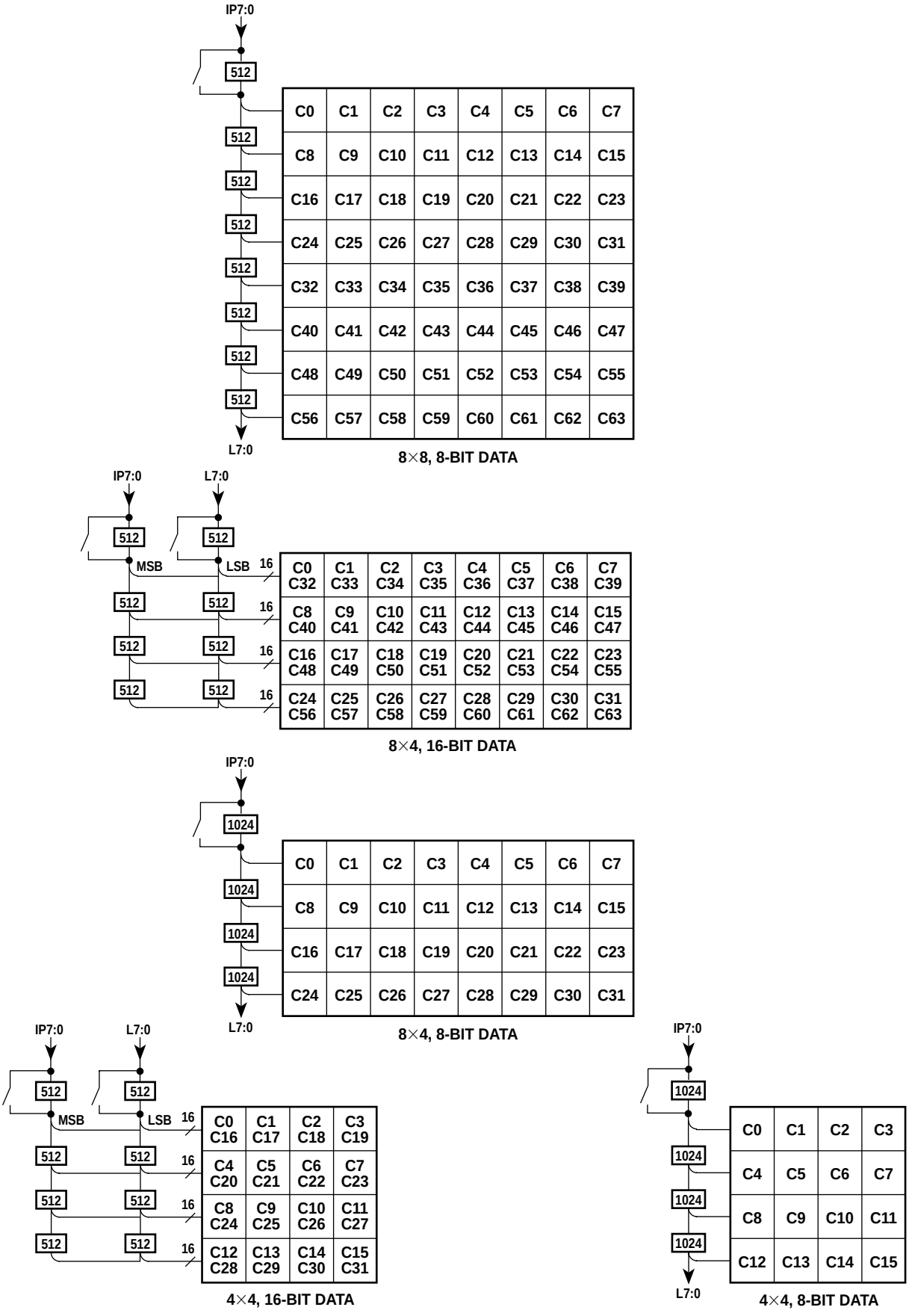


Fig.8 Pixel input delays



NOTE: Two coefficients occurring in the same box have identical values

Fig. 9 Physical coefficient positions

Loading Registers from a Host CPU

The X14:0 expansion data inputs on a single or master device are connected to the host bus to provide address and data for the internal registers. In a multiple device system the remaining devices receive addresses and data which have been passed through the expansion connection between earlier devices in the cascade chain. Each device needs an individual chip enable ($\overline{CE}$) plus a global data strobe ($\overline{DS}$), a read/ not write (R/$\overline{W}$) line, and $\overline{PROG}$ signal from the host.

Registers are individually addressed and can be loaded in any sequence once the global $\overline{PROG}$ signal has been produced by the host. The latter would normally be produced from an address decoder encompassing all the necessary device addresses.

If a self-timed system is to be implemented, a timing strobe must be passed down the expansion chain through the $\overline{PC0}$/$\overline{PC1}$ connections. The $\overline{PC0}$ output from the final device is used as a host REPLY signal, and indicates that the last device has received data after the propagation delay of previous devices. The timing strobe is produced in the Master device from the host data strobe, and will appear on the $\overline{PC0}$ output. This feature allows the user to cascade any number of devices without having to know the propagation delay through each device. The timing information for this mode of operation is given in Fig. 10.

The host can also read the data contained in the internal registers. The required device is selected using chip enable with the R/$\overline{W}$ line high, indicating a read operation. Single device systems output the data read on X7:0, but in multiple device systems data is read from the D7:0 outputs on the final device in the chain. These must be connected back to the host data bus through tristate drivers, whose tristate control must be generated externally (see Figs. 14 and 15). When earlier devices in the chain are addressed, the register contents are transferred through the expansion connections down to the final device. In the self timed configuration the data will be valid when $\overline{REPLY}$ is taken low by $\overline{PC1}$, as shown in Fig. 10.

If REPLY is not to be used, the $\overline{PC0}$/$\overline{PC1}$ connections are not necessary, and the host data strobe for a write operation must be wide enough to allow for the worst case propagation delay through all the devices (t_{DEL}). If the data or address from the host does not meet the set up time given in Fig. 8, the width of the data strobe can be simply extended to compensate for the additional delay. When reading data the access time required is $t_{ACC}1t_{DEL}$(N21), using the maximum times given in the Host Mode Switching Characteristics.

Host control lines

X7:0 — 8-bit data bus. In a Single device system this bus is bidirectional; in other configurations it is an input. Only a Single or Master device is connected directly to the host. Other devices receive data from the output of the previous device in the chain.

X14:8 — 7-bit address bus which is used to identify one of the 73 internal registers. Connected in the same manner as X7:0.

X15 — X15 must be open circuit on the Master device

$\overline{PC0}$ — An input from the previous $\overline{PC1}$ output in a multiple device chain. Not needed on a Single device or if the self timed feature is not used.

$\overline{PC1}$ — Reply to the host from a Single device or from the last device in a cascade chain. It indicates that the write strobe can be terminated. Connected to $\overline{PC0}$ input of the next device at intermediate points in the chain if the self timed feature is used.

R/$\overline{W}$ — Read/Not Write line from the host CPU which is connected to all devices in the system.

$\overline{CE}$ — An active low enable which is normally produced from a global address decode for the particular device. This must encompass all internal register addresses.

$\overline{DS}$ — An active low host data strobe which is connected to all devices in the system.

$\overline{PROG}$ — An active low global signal, produced by the host, which is connected to all devices in the system. Together with a unique chip enable for every device, it allows the internal registers to be updated or examined by the host $\overline{PROG}$ and $\overline{CE}$ should be tied together in a Single device system.

Loading Registers from an EPROM

In the EPROM mode, one device has to assume the role of a host computer. If more than one device is present, this must be the first component in the chain, which must have its $\overline{MASTER}$ pin tied low.

The Master device contains internal address counters which allow the registers in up to 16 cascaded PDSP16488As to be specified. It also generates the $\overline{PROG}$ signal and a data strobe on the pins which were previously inputs. These outputs must be connected to the other devices in the system, which still use them as inputs. The R/$\overline{W}$ input should be tied low on all devices.

The width of the data strobe is determined by the feedback connection from the $\overline{PC1}$ output on the last device to the $\overline{PC0}$ input on the Master. The $\overline{PC0}$/$\overline{PC1}$ connections must be made between devices in a multiple device system; in a single device system the connection is made internally.

The available EPROM access time is determined by an internal oscillator and does not require the pixel clock to be present during the programming sequence. Any pixel clock resynchronization in a real time system will thus not affect the coefficient load operation. The relevant EPROM timing information is shown in Fig. 11.

The load procedure will commence after $\overline{RES}$ has gone from low to high, and will be indicated by the $\overline{PROG}$ output going low. The data from 73 EPROM locations will be loaded into the internal registers using addresses corresponding to those in Table 5. Within a particular page of 128 EPROM locations, the first nine locations supply control register information, and the top 64 supply coefficients. The middle 55 locations are not used. If the window size is 834, the top 32 locations will also contain redundant data, and if the size is 434 the top 48 will be redundant.

In a multiple device system the load sequence will be repeated for every device, and four additional address bits will be generated on the CS3:0 pins. These address bits provide the EPROM with a page address, with one page allocated to each device in the system. Within each page only 73 locations provide data for a convolver, the remainder are redundant as in the single device system. The CS3:0 outputs must also be decoded in order to provide individual chip enables for each device. These can readily be derived by using an AS138 TTL decoder. Bits in an internal control register determine the number of times that the sequence is repeated.

If changes to the convolver operation are to be made after power-on, activating the $\overline{CE}$ input on the Master or Single device will instigate the load procedure. Additional EPROM address bits supplied from the system will allow different filter coefficients to be used.

EPROM control lines

X7:0 8 bit data from the EPROM to the Master or Single device. Otherwise data is received from the previous device in the chain.

X14:8 Lower 7 address bits to the EPROM from a Master or Single device. Otherwise an input from the data output of the previous device.

X15 Tied to ground on a Master device to indicate the EPROM mode.

R/$\overline{W}$ Tied low on all devices.

$\overline{DS}$ An output from a Master or Single device which provides a data strobe for the other devices. A pullup resistor is required on this pin in EPROM mode

CS3: 0 Four additional address bits for the EPROM which are provided by the Master device. They allow 16 additional devices to be used and must be externally decoded to provide chip enables.

$\overline{PC0}$ An input on the Master device which is driven from the $\overline{PC1}$ output of the last device in the chain. Used internally to terminate the write strobe. Connected to previous $\overline{PC1}$ outputs at intermediate points in the chain. Not needed for a Single device.

$\overline{PC1}$ An output connected to the $\overline{PC0}$ input of the next device in the chain. The last device feeds back to the Master. Not needed for a Single device.

$\overline{CE}$ An enable which is produced by decoding CS3:0 from the Master. It is not needed for a Master or Single device which will always use the bottom block of addresses with internally generated write strobes. It can, however, be used on these devices to initiate a new load procedure after the initial power-on sequence.

$\overline{PROG}$ An active low signal produced by an EPROM supported Master or Single device. An input to all other devices. It indicates that a register load sequence is occurring, either after power on, or as the result of $\overline{CE}$ as explained above. It remains active until register 73 in the final device has been loaded. Register A, bits 3:0 define the number of cascaded devices. A pullup resistor is required on this pin in EPROM mode.

System Configuration

The device is configured using a combination of the state of the $\overline{SINGLE}$ and $\overline{MASTER}$ pins, and the contents of the four Mode Control registers. In a Master or Single device the state of the X15 pin is used to define whether the system is EPROM or Host supported, as described above.

Mode Control Registers

Register A bit allocation (Table 8)

BITS 3:0 These bits are 'don't care' when using a host computer but to a Master device, in an EPROM supported system, they define the number of interconnected chips. The EPROM must contain contiguous 128 byte blocks for each of the devices in the system and a 4-bit counter in the Master device will sequence through up to 16 block reads. An internal comparator in the Master causes the loading of the internal registers to cease when the value in the counter equals that contained in these bits. The bits are redundant in a Single device which only uses one 128-byte block.

BITS 6:4 These bits define one of the five basic configurations. The line delays will automatically be configured to match the chosen window size and pixel accuracy. The maximum clock rate that is available to the user reflects the internal multiplication factor.

BIT 7 This bit must be set if the pixel clock is greater than 20MHz. It disables the output and input time multiplexing, and instead outputs the least significant half of the 32-bit intermediate sum for the complete clock cycle. When the gain control is used, the output multiplexing will automatically be disabled.

Bit	Code	Function
3:0	XXXX	Number of extra devices from 1-15
6:4	000	8-bit, 838 window, 10MHz max., 83512 line delays.
6:4	001	16-bit, 834 window, 10MHz max., 43512 line delays.
6:4	010	16-bit, 434 window, 20MHz max., 43512 line delays.
6:4	011	8-bit, 834 window, 20MHz max., 431024 line delays.
6:4	101	8-bit, 434 window, 40MHz max., 431024 line delays
7	0	Multiplexed exp. data
7	1	Non-multiplexed exp. data

Table 8 Register A bit functions

Register B bit allocation (Table 9)

BIT 0 This bit defines the input for the second group of line delays. It must be set in the 16-bit pixel modes, and is set by power on reset.

BIT 2:1 These bits control the mode of operation of the line stores. In real time systems pixels can be stored either until HRES (sync) goes high , or until a pre-determined count is reached. In the frame store mode line store operations are continuous, with a pre-determined line length.

BIT 3 When this bit is set four pipeline delays are added to the pixel inputs to compensate for the internal/ external delays between line stores. The extra delay is only necessary when a device supplied with system video in which the first pixel in a line is valid in the period following the first active clock edge. See Fig 7. The delay is not necessary if the device is fed from the output of another convolver. When set this bit will add four additional delays to those defined by register D, bits 4: 2.

BIT 4 When this bit is set the expansion adder will not be used. It is automatically set in a Master or Single device.

BIT 7 This bit controls the bypass option on the first line delay on the L7:0 inputs. It is only effective when an 8 bit pixel mode is selected, which also needs more than four line delays. When L7:0 are used as outputs it should always be reset. In the 16-bit modes the bypass function is only controlled by the BYPASS pin, and the bit is redundant.

Bit	Code	Function
0	0	Second line delay group fed from the first group
0	1	Second line delay group fed from L7:0 which become inputs
2:1	00	Store pixels to end of line
2:1	01	Store pixels till count is reached
2:1	10	Frame store operation
2:1	11	Not Used
3	0	No delays on pixel inputs
3	1	4 delays on both pixel inputs
4	0	Use expansion adder
4	1	Expansion adder disabled
6:5		Not used
7	0	Use first delay in second group
7	1	Bypass first delay in second group

Table 9 Register B bit functions

Register C bit allocation (Table 10)

BIT 0 If this bit is set, the 20-bit field selected from the 32-bit result, is defined automatically by internal logic.

BITS 3:1 These bits are in conjunction with register D, bits 7:5 to define the pixel delay from the HRES input to the DELOP output. They are used to match the appropriate processing delay in a particular system. The minimum delay is 29 pixel clocks.

BITS 5:4 These bits define which of the four 20-bit fields out of the 32-bit final result is selected as the input to the gain control. They are redundant when the gain control is not used, or if register C, bit 0, is set.

BITS 7:6 These bits define the use of the gain control as given in Table 10. Intermediate devices in a multiple device system *must* bypass the gain control block, otherwise the additional pipeline delays will affect the result. Disabling the gain control block will reduce the device pipeline by 13 CLK cycles from the delays shown in Table 6.

Bit	Code	Function
0	0	Field selection defined by C5:4
0	1	Automatic field selection
3:1	000	DELOP = 2910 clocks
3:1	001	DELOP = 2918 clocks
3:1	010	DELOP = 29116 clocks
3:1	011	DELOP = 29124 clocks
3:1	100	DELOP = 29132 clocks
3:1	101	DELOP = 29140 clocks
3:1	110	DELOP = 29148 clocks
3:1	111	DELOP = 29156 clocks
5:4	00	Select upper 20 bits
5:4	01	Select next 20 bits
5:4	10	Select next 20 bits
5:4	11	Select bottom 20 bits
7:6	00	By-pass the gain control
7:6	01	Normal gain control output
7:6	10	Saturate at max.1ve and 2ve values.
7:6	11	Force 2ve to zero.Sat.1ve values.

Table 10 Register C bit functions (continues…)

Table 10 Register C bit functions (continued)

Register D bit allocation (Table 11)

BIT 0 If this bit is set the expansion data input is delayed by four pixel clocks before it is added to the present convolver output. It is used in multiple device systems when the partial window width is 8 pixels.

BIT 1 When this bit is set the internal sum is shifted to the left by 8 places before being added to the expansion input. It is used when two devices are used, each in an 8-bit pixel mode, to construct a 16-bit pixel mode.

BITS 3:2 These bits define the delays on both sets of pixel inputs before entering the line stores. The delays are always identical on both sets.

BIT 4 When this bit is set the convolver interprets 8 or 16-bit pixels as 2's complement signed numbers

BIT 7:5 These bits add 0 to 7 additional clock delays to those selected by Register C, bits 3:1.

Bit	Code	Function
0	0	X15:0 Not delayed
0	1	X15:0 Delayed
1	0	Internal sum not shifted
1	1	Internal sum multiplied by 256
3:2	00	Input to line stores not delayed
3:2	01	Input to line stores delayed by 4
3:2	10	Input to line stores delayed by 8
3:2	11	Input to line stores delayed by 12
4	0	Unsigned pixel data input
4	1	2's complement pixel data input
7:5	XXX	Add 0 to 7 clock delays to DELOP

Table 11 Register D bit functions

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions, unless otherwise stated:

V_{DD} = 15V±10%, GND = 0V, T_{AMB} (Commercial) = 0°C to170°C, T_{AMB} (Industrial) = 240°C to 185°C, T_{AMB} (Military) = 255°C to 1125°C

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2·4		-	V	I_{OH} = 4mA
Output low voltage	V_{OL}	-		0·4	V	I_{OL} = 28mA
Input high voltage	V_{IH}	2·0		-	V	
Input low voltage	V_{IL}	-		0·8	V	
Input leakage current	I_{IN}	2 1 0		1 1 0	µA	GND < V_{IN} < V_{DD}, no internal pullup
Input capacitance	C_{IN}		10		pF	
Output leakage current	I_{OZ}	2 5 0		1 5 0	µA	GND < V_{OUT} < V_{DD}, no internal pullup
Output short circuit current	I_{OS}	10		300	mA	V_{DD} = 15·5V
Current at full speed	I_{SP}			Max.	mA	

NOTE: Signal pins $\overline{PC0}$, X15, $\overline{MASTER}$, $\overline{SINGLE}$ and OVR have pullup resistors in the range 15kΩ to 200kΩ. BYPASS, $\overline{PROG}$ and $\overline{DS}$ have no internal pullup resistors. When the device is used in EPROM mode, external pullup resistors should be connected to the $\overline{PROG}$ and $\overline{DS}$ pins.

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply voltage, V_{DD}	20·5V to 17·0V
Input voltage, V_{IN}	20·5V to V_{DD} 10·5V
Output voltage, V_{OUT}	20·5V to V_{DD} 10·5V
Clamp diode current per pin, I_K (see note 2)	18mA
Static discharge voltage (HBM)	500V
Storage temperature, T_S	265°C to1150°C
Maximum junction temperature, T_{JMAX}	
Commercial grade	195°C
Industrial grade	1110°C
Military grade	1150°C
Package power dissipation	2000mW
Thermal resistance, junction-to-case, θ_{JC}	5°C/W

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation should not be exceeded for more than1 second, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliablity.
4. Current is defined as negative into the device.

PDSP16488A MA ACBR and PDSP16488A MA GCPR (MIL-STD-883 CLASS B PARTS)

Polyimide is used as an inter-layer dielectric and as glassification. Polymeric material is also used for die attach which, according to the requirements in paragraph 1.2.1, precludes categorising these devices as fully compliant. In every other respect, these devices are manufactured and screened in full accordance with MIL-STD-883 (latest revision).

The PDSP16488A MA ACBR (PGA packge) is subject to the constant acceleration test, Method 2001, Test Condition A (5kg).

Life test/burn-in connections are given in Tables 12 and 13 on the following page.

Change Notification

The change notification requirements of MIL-PRF-38535 will be implemented on MIL-STD-883 grade devices. Known customers will be notified of any changes since the last buy when ordering further parts if significant changes have been made.

Rev.	A	B	C	D
Date	MAR 1993	JUL 1996	NOV 1997	

Pin	Voltage	Pin	Voltage	Pin	Voltage	Pin	Voltage	Pin	Voltage
A1	GND	L2	GND	M10	N/C	E12	15·0V	B6	N/C
B1	N/C	M1	GND	N11	N/C	D13	N/C	A5	N/C
C2	GND	N1	GND	M11	N/C	D12	N/C	B5	N/C
C1	GND	N2	GND	N12	N/C	C13	N/C	A4	N/C
D2	GND	M3	N/C	N13	N/C	C12	15·0V	B4	N/C
D1	N/C	N3	N/C	M13	N/C	B13	N/C	A3	N/C
E2	GND	M4	N/C	L12	N/C	A13	N/C	B3	N/C
E1	GND	N4	N/C	L13	N/C	A12	N/C	A2	N/C
F2	GND	M5	15·0V	K12	GND	B11	N/C	F1	15·0V
G2	GND	N5	N/C	K13	N/C	A11	N/C	N6	15·0V
G1	15·0V	M6	N/C	J12	N/C	B10	N/C	F13	15·0V
H2	N/C	M7	15·0V	J13	N/C	A10	N/C	A6	15·0V
J1	15·0V	N7	N/C	H12	N/C	B9	N/C	H1	GND
J2	15·0V	M8	N/C	G12	GND	A9	N/C	N8	GND
K1	15·0V	N9	N/C	G13	15·0V	B8	15·0V	H13	GND
K2	N/C	M9	N/C	F12	15·0V	B7	N/C	A8	GND
L1	GND	N10	N/C	E13	GND	A7	N/C		

Table 12 Life test/burn-in connections for PDSP16488A MA ACBR (PGA). NOTE: PDA is 5% and based on groups 1 and 7

Pin	Voltage	Pin	Voltage	Pin	Voltage	Pin	Voltage
1	N/C	34	N/C	67	N/C	100	N/C
2	N/C	35	N/C	68	GND	101	15·0V
3	15·0V	36	N/C	69	N/C	102	N/C
4	N/C	37	N/C	70	GND	103	N/C
5	N/C	38	N/C	71	N/C	104	N/C
6	15·0V	39	N/C	72	15·0V	105	N/C
7	GND	40	GND	73	GND	106	N/C
8	N/C	41	N/C	74	15·0V	107	GND
9	N/C	42	N/C	75	15·0V	108	N/C
10	15·0V	43	N/C	76	GND	109	GND
11	GND	44	N/C	77	15·0V	110	N/C
12	15·0V	45	N/C	78	GND	111	15·0V
13	N/C	46	15·0V	79	15·0V	112	N/C
14	N/C	47	N/C	80	15·0V	113	N/C
15	N/C	48	15·0V	81	15·0V	114	N/C
16	N/C	49	N/C	82	15·0V	115	GND
17	15·0V	50	15·0V	83	N/C	116	N/C
18	GND	51	N/C	84	GND	117	N/C
19	N/C	52	N/C	85	GND	118	N/C
20	GND	53	N/C	86	GND	119	GND
21	GND	54	15·0V	87	GND	120	GND
22	N/C	55	GND	88	GND	121	N/C
23	N/C	56	GND	89	15·0V	122	15·0V
24	N/C	57	N/C	90	GND	123	N/C
25	N/C	58	N/C	91	15·0V	124	N/C
26	N/C	59	N/C	92	GND	125	N/C
27	GND	60	N/C	93	15·0V	126	N/C
28	N/C	61	N/C	94	GND	127	GND
29	N/C	62	N/C	95	GND	128	N/C
30	N/C	63	GND	96	GND	129	N/C
31	N/C	64	GND	97	N/C	130	N/C
32	N/C	65	N/C	98	GND	131	N/C
33	N/C	66	N/C	99	N/C	132	N/C

Table 13 Life test/burn-in connections for PDSP16488A MA GCPR (QFP). NOTE: PDA is 5% and based on groups 1 and 7

Switching Characteristics for Host mode

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
$\overline{DS}$ hold time after $\overline{REPLY}$ low	t_{DSH}	20		ns	Only applicable for Read ops and if $\overline{REPLY}$ is used
Host address/data setup time	t_{HSU}	0		ns	Only applicable if $\overline{REPLY}$ is used (Note 1)
Read setup time to prevent Write	t_{RA}	5		ns	
Host signal hold time	t_{HH}	10		ns	Must always be guaranteed
Expansion in to data out in $\overline{PROG}$ mode	t_{DEL}		30	ns	No clocks are needed in $\overline{PROG}$ mode
Delay from $\overline{DS}$ low to $\overline{PC1}$ low (Note 2)	t_{EXP}		50	ns	Greater than t_{DEL} under all conditions
$\overline{CE}$ setup time	t_{CSU}	0		ns	
$\overline{CE}$ hold time	t_{CH}	0		ns	
$\overline{PROG}$ setup time	t_{PSU}	0		ns	
$\overline{PROG}$ hold time	t_{PH}	0		ns	
$\overline{PC1}$ high delay after $\overline{DS}$ high	t_{PCH}		50	ns	Defines $\overline{DS}$ high time
Coefficient read time	t_{ACC}		50	ns	From Master or Single device
Coefficients valid time before $\overline{REPLY}$	t_{RSU}	5		ns	

NOTES

1. If $\overline{REPLY}$ is not used, time is referenced to the rising edge of $\overline{DS}$ and when set up must be $N \times t_{DEL}$ for N devices.
2. Equivalent to $\overline{PC0}$ to $\overline{PC1}$ delay

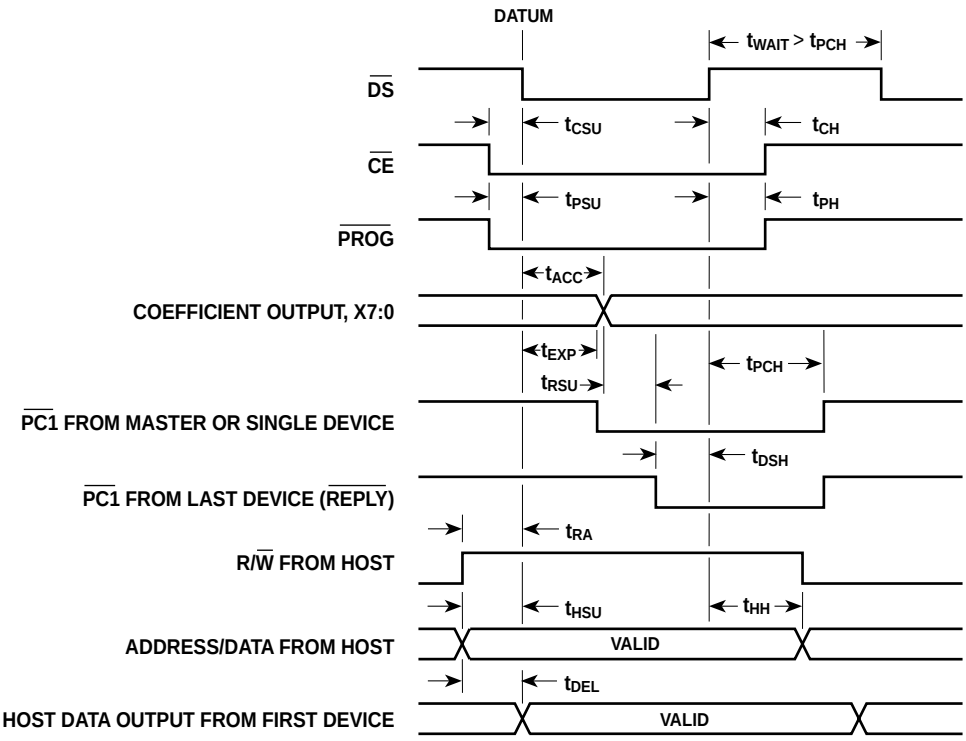


Fig. 10 Host timing

Switching Characteristics for EPROM mode

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Delay from $\overline{DS}$ low to Master $\overline{PC1}$	t_{PCD}		50	ns	
Delay from $\overline{PC0}$ low to $\overline{DS}$ high	t_{WH}	5		ns	
Delay from $\overline{DS}$ high to $\overline{PC1}$ high	t_{PCH}		50	ns	
$\overline{DS}$ high time	t_{WW}	250		ns	
$\overline{DS}$ high to new EPROM address	t_{AD}		30	ns	
EPROM data setup time	t_{DS}	20		ns	
$\overline{DS}$ low time	t_{RW}	10		ns	Single device
$\overline{CE}$ setup time	t_{CSU}	0		ns	
$\overline{CE}$ hold time	t_{CH}	0		ns	
EPROM data access time	t_{DA}	200		ns	
Expansion in to data out	t_{DEL}		30	ns	
$\overline{PC0}$ to $\overline{PC1}$ delay	t_{EXP}		50	ns	Greater than t_{DEL} at all temperatures

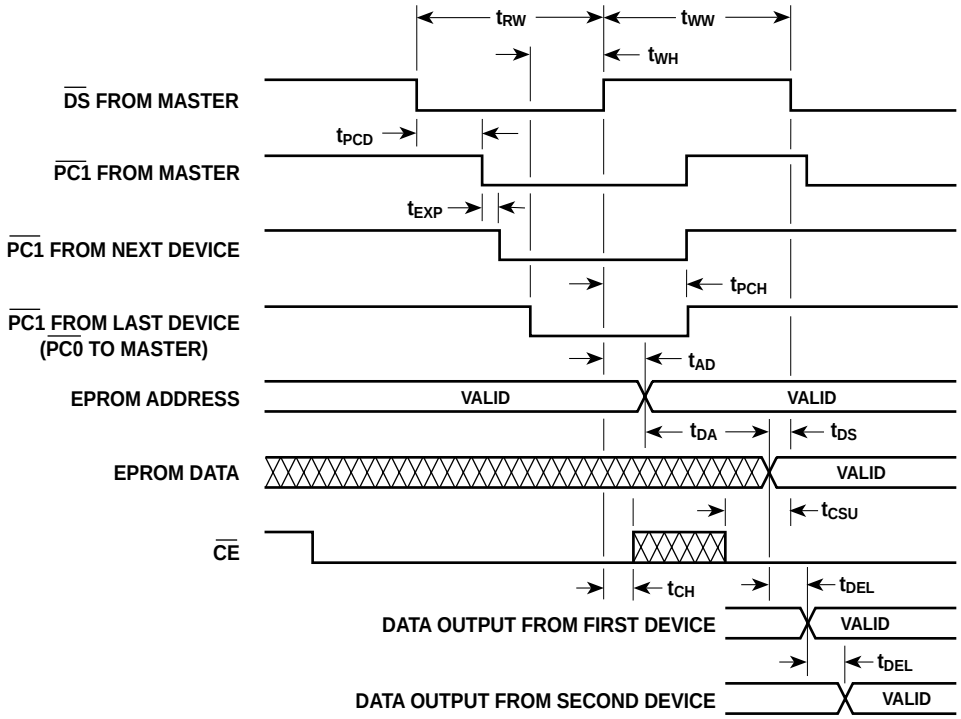


Fig. 11 EPROM timing

Switching Characteristics, operational timings

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
CLK low time	t_{CL}	25		ns	32-bit multiplexed output
		10		ns	16-bit output
CLK high time	t_{CH}	25		ns	32-bit multiplexed output
		10		ns	16-bit output
Data in setup time	t_{DSU}	10		ns	
Data in hold time	t_{DH}	0		ns	
CLK rising to output delay	t_{RD}		21	ns	Increase to 24ns for DELOP output
L7:0 output delay	t_{LD}		20	ns	
HRES low setup time	t_{RSU}	10		ns	
Output enable time	t_{DLZ}		15	ns	Measured with a 15kΩ series resistor and 30pF load capacitance
Output disable time	t_{DHZ}		15	ns	
X15:0 Expansion setup time	t_{XSU}	5		ns	
X15:0 Expansion hold time	t_{XDH}	7		ns	

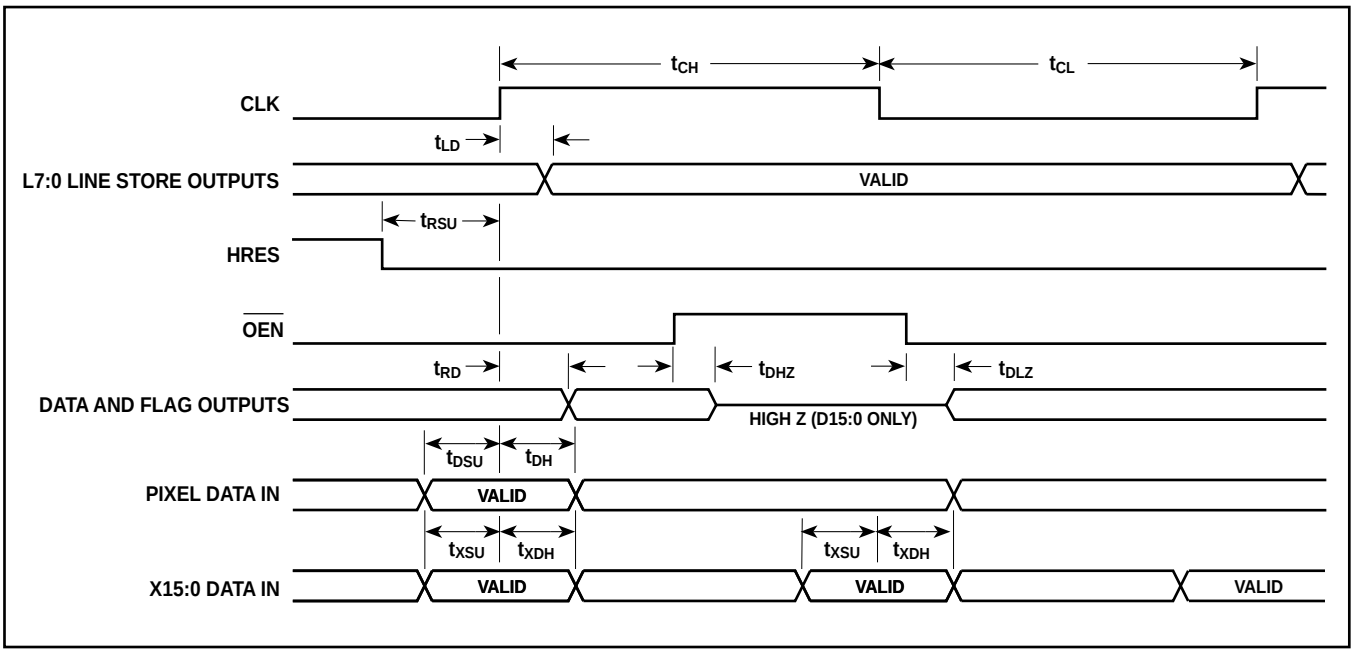


Fig. 12 Operational timing

APPLICATIONS INFORMATION

Device Requirements

The number of devices required to implement a given convolver window depends on the size of the window, the required pixel rate, and whether the pixel accuracy is to be 8 or 16 bits. In practice the PDSP16488A supports windows requiring one, two, four, six, or eight devices without additional logic. Table 2 gives typical window sizes which may be obtained with the above number of devices.

Figs. 13 through 20 show system interconnections for these arrangements. Other configurations are possible but may need the support of additional pixel/line delays and/or expansion adders. Although not necessarily shown, all configurations can be supported by either an EPROM or a Host computer. Interlaced or non-interlaced video may also be used, unless explicitly stated otherwise in the text.

Expansion with 8-bit pixels is a straightforward process and the number of devices needed is easily deduced from the window sizes available in a single device. At pixel rates above 20MHz it may not be practical to use more than four devices, since the full 32-bit intermediate precision is not available. The lack of expansion multiplexing reduces the intermediate precision to 16 bits. The partial sum outputs must thus not overflow these 16 bits; this will require the coefficients to be scaled down appropriately with a resulting loss in accuracy.

Expansion with 16-bit pixels can be achieved in several ways. The simplest way is to use two devices, each working with 8-bit pixels. One device handles the least significant part of the data, and its output feeds the expansion input of a second device. This performs the most significant half of the calculation. The least significant half is then added to the most significant sum, after the latter has been multiplied by 256, i.e. shifted by eight places. This shift is done internally and controlled by Register D, bit 1. The internal 32-bit accuracy prevents any loss in precision due the shift and add operation.

The window size with this arrangement is restricted to that available in a single device, at the required pixel rate but with 8-bit pixels. Thus two devices can be used, for example, to provide an 838 window with 16-bit pixels and 10MHz rates.

If a larger extended precision window is needed, it is possible to use four devices. Each device is then programmed to be in a 16-bit data mode, but should be restricted to rates below 20MHz, if the 32-bit intermediate precision is to be maintained. In the 16-bit modes, however, the output from the last line delay is not available due to pin limitations. This is not a problem in a four device interlaced system, since half of the devices will be fed from an external field delay. In non interlaced systems additional external line delays would be needed. An alternative approach would be to configure all the devices in the appropriate 8-bit mode, do separate least significant and most significant calculations, and then combine the results in an external adder after a wired-in shift.

Single device configuration

Fig.13 illustrates both EPROM and Host supported single device systems, with or without interlaced video. In both cases the Single and X15 pins must be tied low, and the $\overline{PC0}$, $\overline{PC1}$, and $\overline{DS}$ pins are redundant. The $\overline{PROG}$ pin becomes an output and indicates that a register load sequence is occurring. The first line delay must always be bypassed in a non interlaced system, however, since an internal pullup is not provided, the BYPASS pin should be tied to V_{CC} for the correct operation. With interlaced video the BYPASS input is used to distinguish between the odd and even fields.

The $\overline{CE}$ input may be left open circuit if coefficients are to be simply loaded after a power on reset signal; the latter being applied to the $\overline{RES}$ input. Alternatively the $\overline{CE}$ input may be used to change the coefficients at any time after power on reset; the EPROM would then need additional address bits for the extra sets of coefficients that are to be stored.

In an interlaced system the pixels from the previous field must use the IP7:0 inputs, and the live pixels must use the L7:0 inputs. Interlaced systems requiring extended precision pixels are non-supported with a single device, since the L7:0 inputs are then use for the least significant 8 bits, and the IP7:0 inputs for any more significant bits.

If the X15 pin is left open circuit, an internal pullup will configure the device in the host supported mode. The host must then supply a data strobe and an R/$\overline{W}$ control line. The X7:0 pins must be connected to the host data bus, and are used to both load and read back register values. The $\overline{PROG}$ and $\overline{CE}$ pins may be connected together, and then driven by a host address decode. The output on $\overline{PC1}$, which provides a $\overline{REPLY}$ to the host, need not be used if the width of the data strobe is greater than the maximum t_{EXP} value given in Fig. 10.

The configuration bits 6:4 in register A define the window size, maximum pixel rate, and pixel resolution. Window sizes smaller than the maximum in any configuration are implemented by filling in the window with zero coefficients. Bits 3:0 are irrelevant in the Single mode, as is bit 7 if the gain control is used.

The result would be expected to lie in either the bottom 20 bits of the 32-bit result , or possibly in the next 20-bit field displaced by four bits. Register C, bits 5:4, must thus select one of these fields for subsequent use by the gain control. The gain is then adjusted such that the 16 outputs available on pins D15:0 are in fact the 16 most significant bits of the result. The gain needed is application specific, but if too much gain is used the OVR pin will go high to indicate an overflow.

Register B, bits 2:1, must be set to select the required method of defining the length of the line delays, and the use of bit 3 is dependent on any external pixel delays before the convolver input. No additional delays are needed on the pixel inputs in a single device system, and register D, bits 4:2, should be reset. The pipeline delay in the DELOP output path should match one of those in Table 6, and is window size dependent.

Dual device configurations

Two devices, each configured with 8-bit pixels and 8W34D windows, can be used to provide an 838 window at up to 20MHz pixel rates. Fig. 14 shows both the non-interlaced and interlaced arrangements.

Video lines containing up to 1024 pixels are possible in both configurations, since each device only needs four line delays. One device is configured as the Master by grounding the $\overline{MASTER}$ pin; the other then receives control signals in the normal way and has its $\overline{MASTER}$ and $\overline{SINGLE}$ pins left open circuit.

The internal convolver sum, in the device producing the final result, must be delayed by 4 pixels to match the inherent delay in the expansion output from the other device. This is actually achieved by delaying the pixel inputs to the line stores (register D, bits 3:2, = 01). No additional delay in the expansion input is needed, but the pipeline delay used to produce DELOP must be four clocks greater than that given in Table 6 for a single device. The DELOP output is redundant in one of the two devices.

Two devices can also be used to support systems requiring 16-bit pixels. With this approach the 1638 multiplication is realised as two 838 operations, with the results added together after the most significant half has been shifted by 8 places to the most significant end. This shift operation is controlled by register D, bit 1. Both convolvers are programmed to contain the same coefficients. The convolved output can theoretically grow to 30 bits, and the appropriate field must be selected before using the gain control.

Examples of this operating mode are shown in Fig. 15. Each device must be configured in the same 8-bit pixel operating mode, but the device producing the final result must use the 8 place shift option on its internal sum.

The least significant 8 bits of the pixel are connected to the Master device and the most significant 8 bits are connected to the device producing the final result.. The internal sum in this device must be delayed by four pixels to match the delay in the expansion output from the first device. This is actually achieved by delaying the pixel inputs to the line stores (register D, bits 4:2, = 001). The expansion input needs no additional delay (register D, bits 1:0, = 10).

The actual pixel precision can be any number of pixels between 8 and 16, and may be a signed or unsigned number. Any unused, more significant bits, must respectively be either sign extended or be tied low.

DELOP must have four additional pipeline delays in order to match the total processing delay. This output can be obtained from either device.

Four device systems

Four devices, each in the 838 mode, can be used to provide a 16316 window, with 8-bit pixel resolution and 10MHz clock rates. The partial sum from the first device in each row must be delayed by eight pixel clocks before it is added to the result from the next device. This provides the eight pixel displacement to match the width of the window. The delay is actually provided by four additional delays in the expansion input to the next device, plus the inherent four clock delays in outputting results from the first device. Register D, bit 0 controls the additional delay.

The internal convolver sums, in the two devices in the second row, must be delayed by 12 clocks before they are added to the result from the first row. This twelve clock delay is necessary because of the combination of the eight pixel horizontal displacement delay, and the four clock delay in outputting the result from the last device in the top row. It is actually achieved by delaying the pixel inputs to the line stores (register D, bits 3:2, = 11).

The DELOP output must have 20 delays additional to those in a single device. This compensates for the twelve delays added to the convolver sums in the second row, plus an additional eight delays to compensate for the partial width of the first device in the second row.

Four devices can also be used to give an 838 window, but with a 30MHz pixel clock. Each device is configured to provide a 434 partial window, but the maximum pixel rate is reduced from 40 to 30MHz because of the response of the line delay expansion circuitry. Intermediate precision is restricted to 16 bits, since time multiplexed data outputs cannot be used above 20MHz.

This configuration requires no additional delay in the expansion inputs, and the inputs to the line stores both devices in the second row must be delayed by 8 clock cycles (register D, bits 3:2, = 10). The DELOP output needs twelve additional clock delays to match the processing delay.

Figs. 16 and 17 show non-interlaced and interlaced versions of the above 838 and 434 arrangements

Fig. 18 shows how four devices can also be used to provide an 838 window, with 16-bit pixels and 20MHz clock rates. The expansion data from a previous device needs no additional delay since the partial window size in each device is only 434. The internal convolver sums from third and fourth devices must be delayed by 8 clocks and the DELOP output must have 12 additional delays. If this arrangement is to be used in a non-interlaced application, the field store must be replaced by four line delays.

Six device systems

As shown in Fig. 19, six devices, each in an 8W34D mode using 8-bit pixels, can provide a 16W312D window at 20MHz clock rates. Expansion inputs from previous devices in a row (but not the first device in each row) need an extra 4 clocks of delay since the partial window is eight pixels wide. Internal convolver sums need a differential delay of 12 clock cycles from row to row (register D, bits 3:2, = 11).

The DELOP output must have 32 additional delays to match the total processing delay.

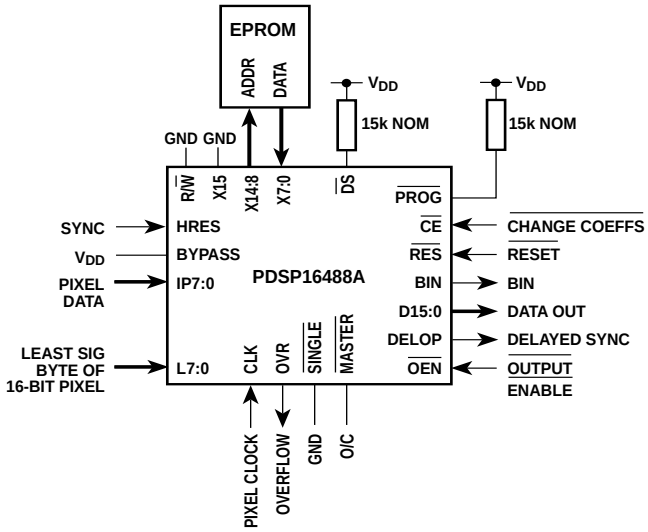
Eight device systems

Two additional chips will extend the above six device configuration to a 16316 window. Internal convolver sums must have differential delays of 12 clock cycles between rows, as in the six device system. The DELOP output needs 44 additional clock delays.

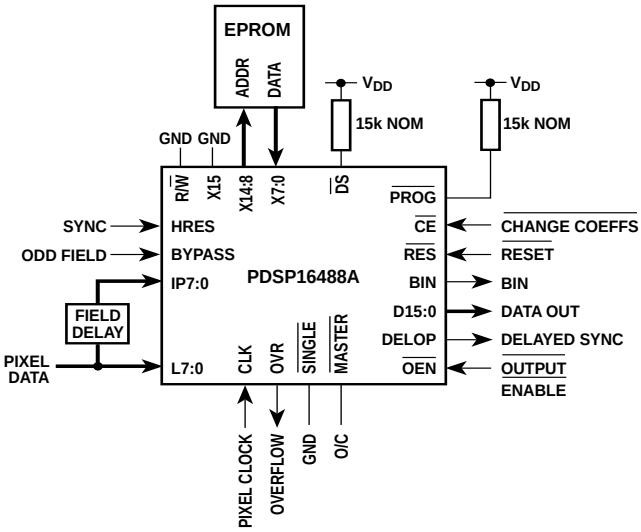
Nine device systems

Nine devices each in the 838 mode will provide a 24324 window with 8- bit data and 10MHz pixel clocks. This is shown in Fig. 20. Expansion data inputs from previous devices in a row (but not the first device in each row) need an extra 4 clocks of delay, controlled by register D, bit 0 The internal convolver sums need differential delays of 20 clock cycles between rows. Sixteen of the latter delays can be provided internally by setting register B, bit 3 and also register D, bits 3:2. The four extra delays must be provided externally.

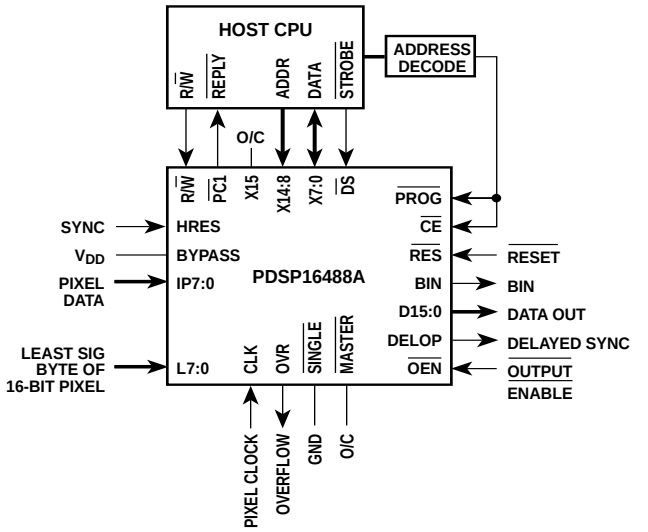
The DELOP output needs 56 clock delays in addition to the 29 required for the 838 single device configuration.



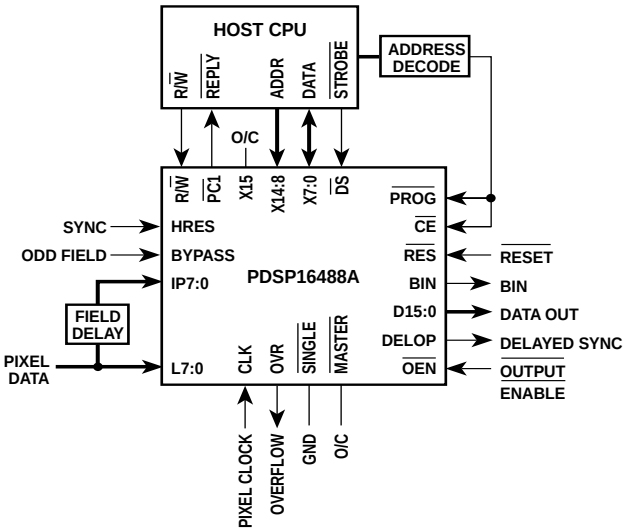
Non-interlaced EPROM mode



Interlaced EPROM mode

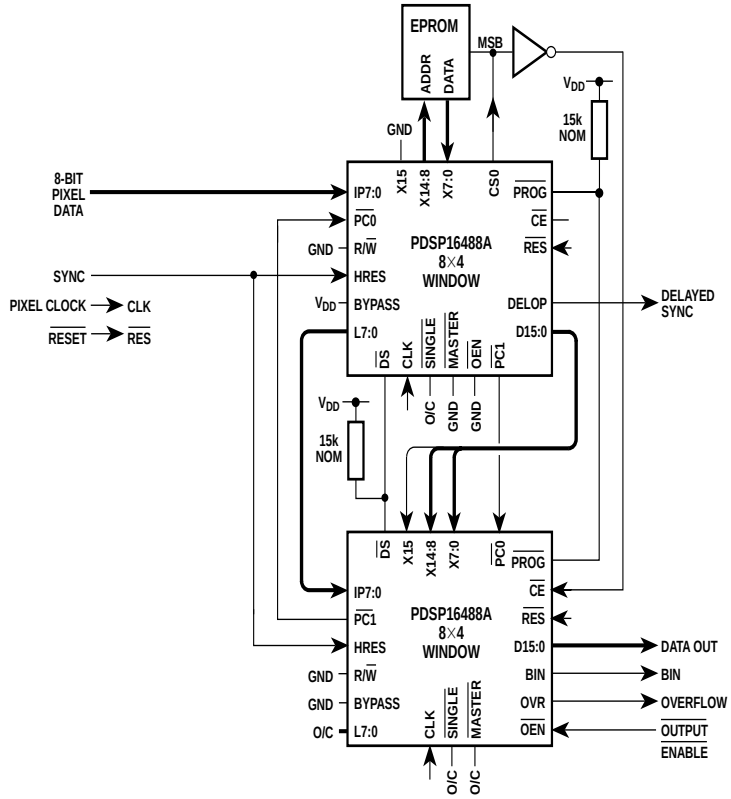


Non-interlaced 16-bit Host loaded

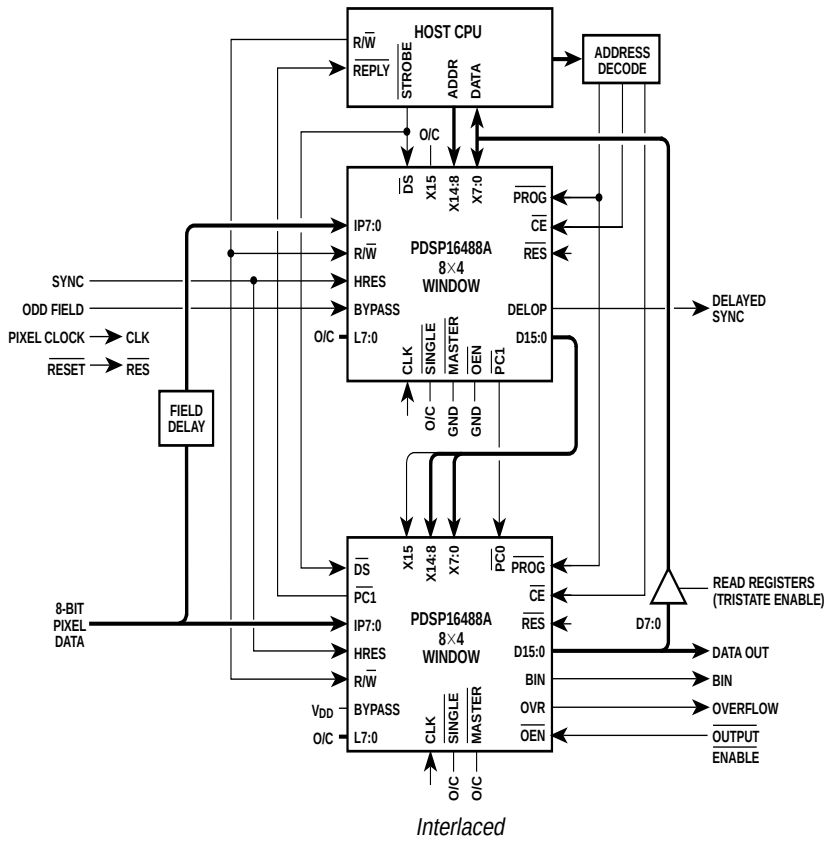


Interlaced 16-bit Host loaded

Fig. 13 Single device systems

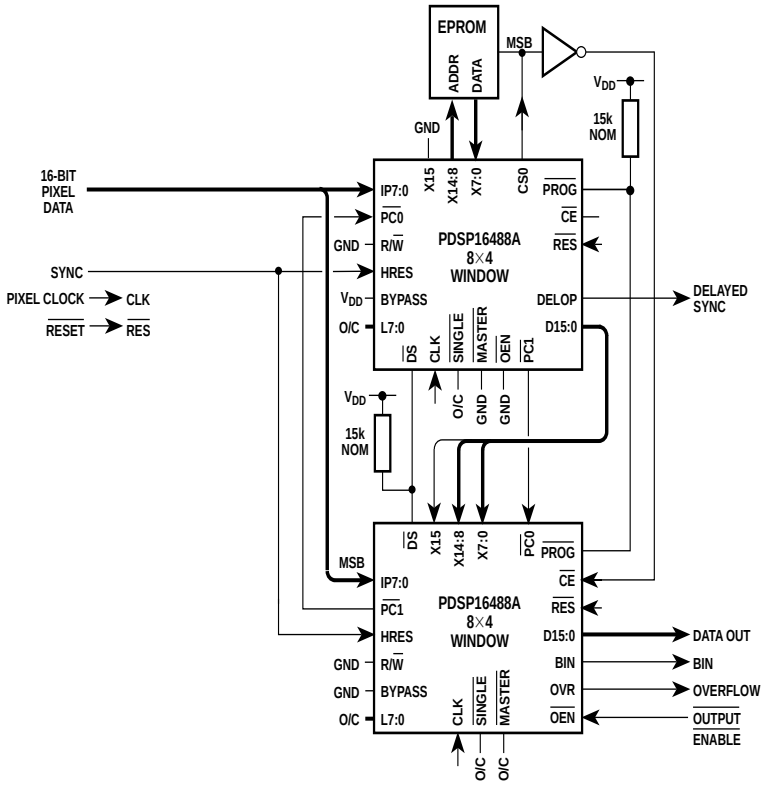


Non-interlaced

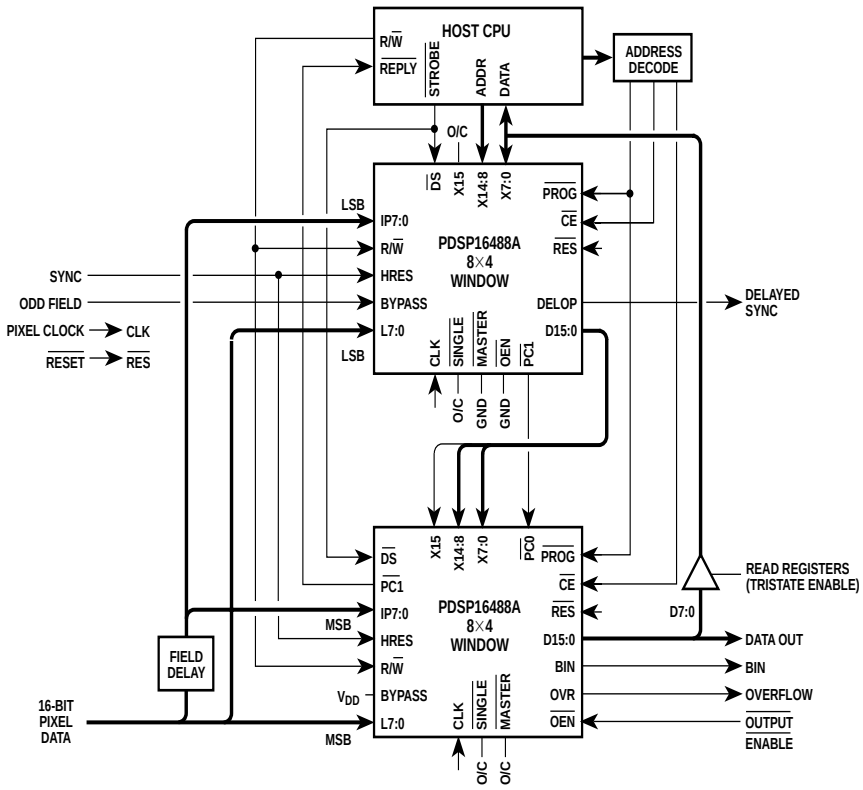


Interlaced

Fig. 14 8-bit dual device systems



Non-interlaced



Interlaced

Fig. 15 Dual device 16-bit systems.

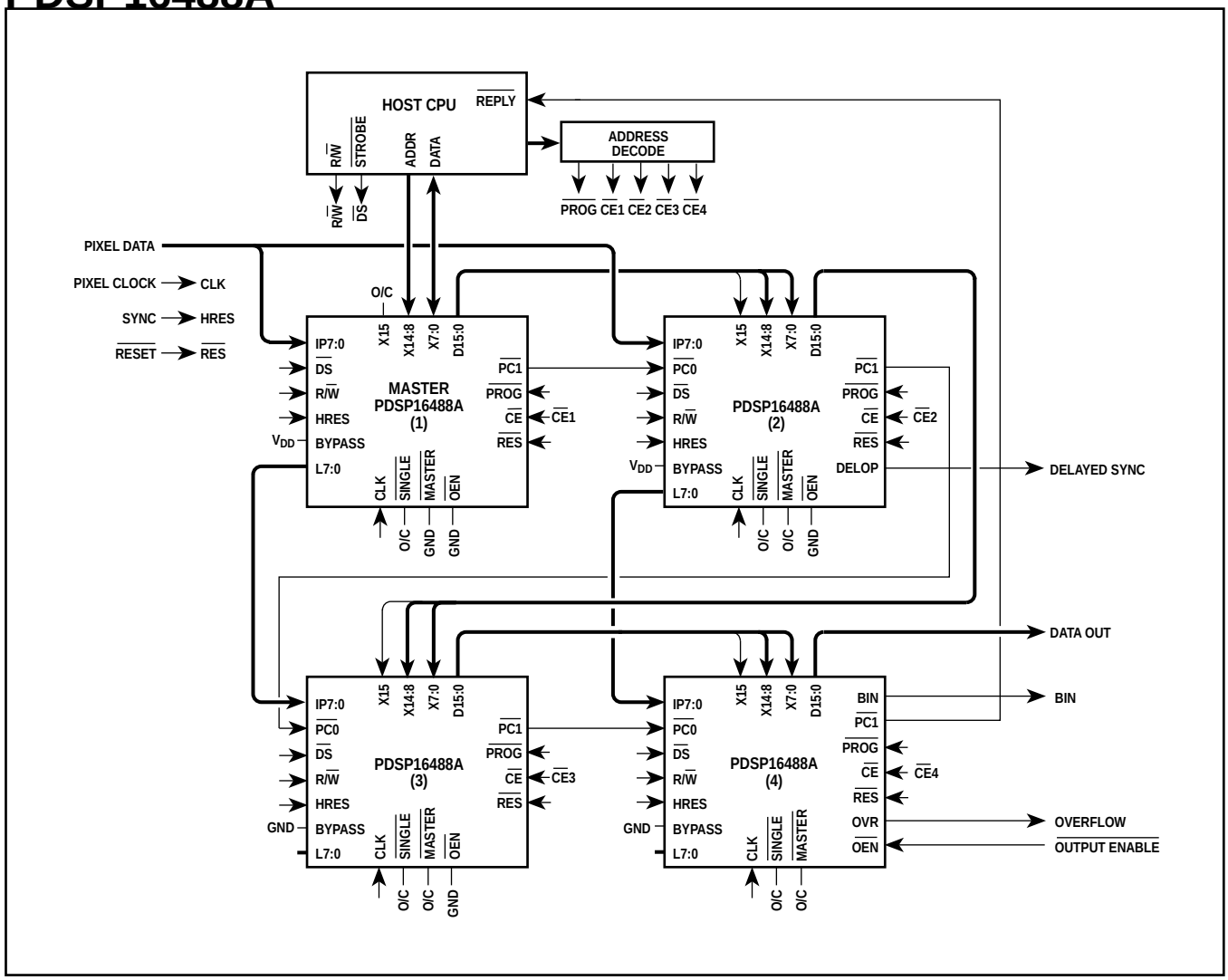


Fig. 16 Four device non-interlaced system.

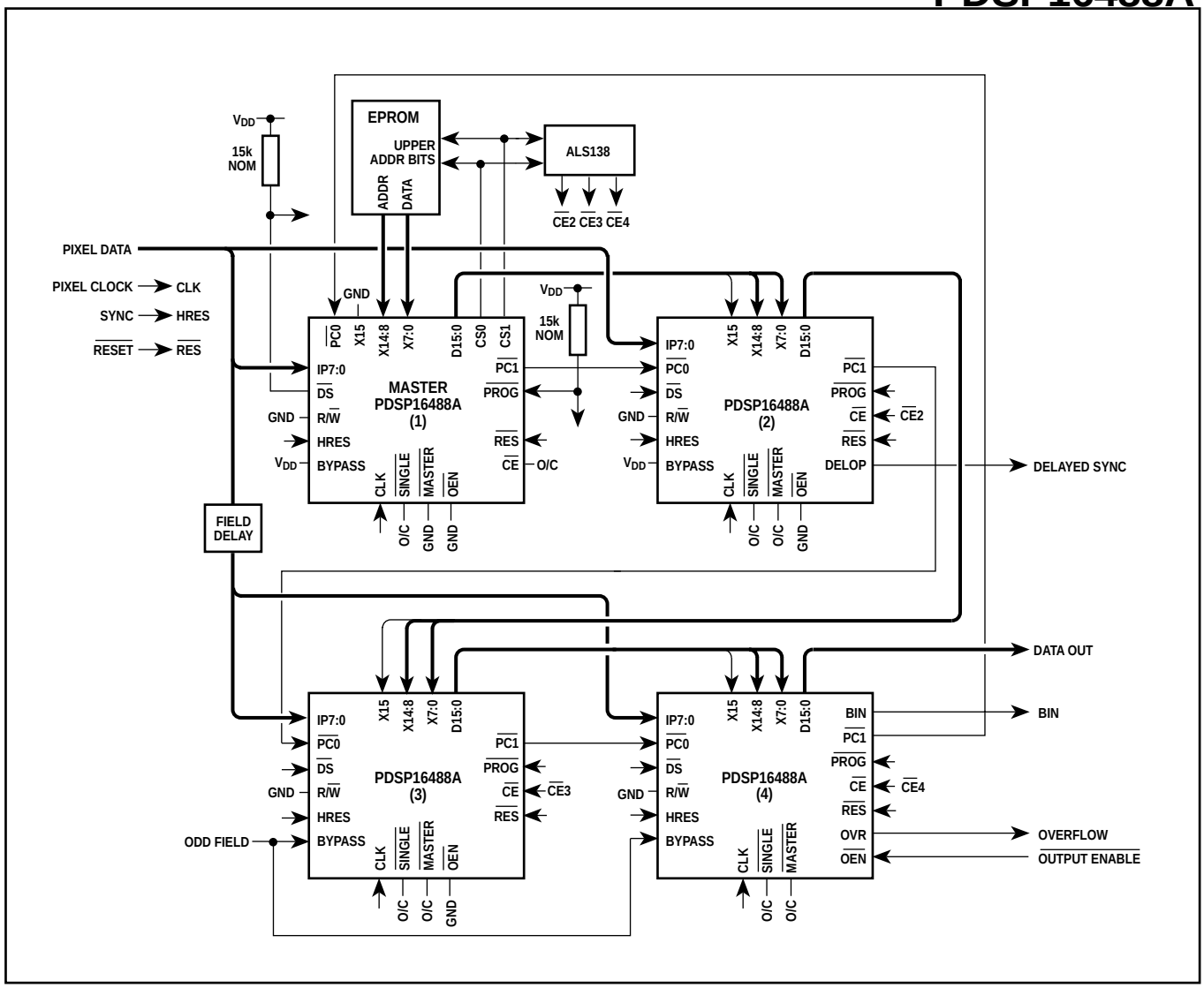


Fig. 17 Four device interlaced system.

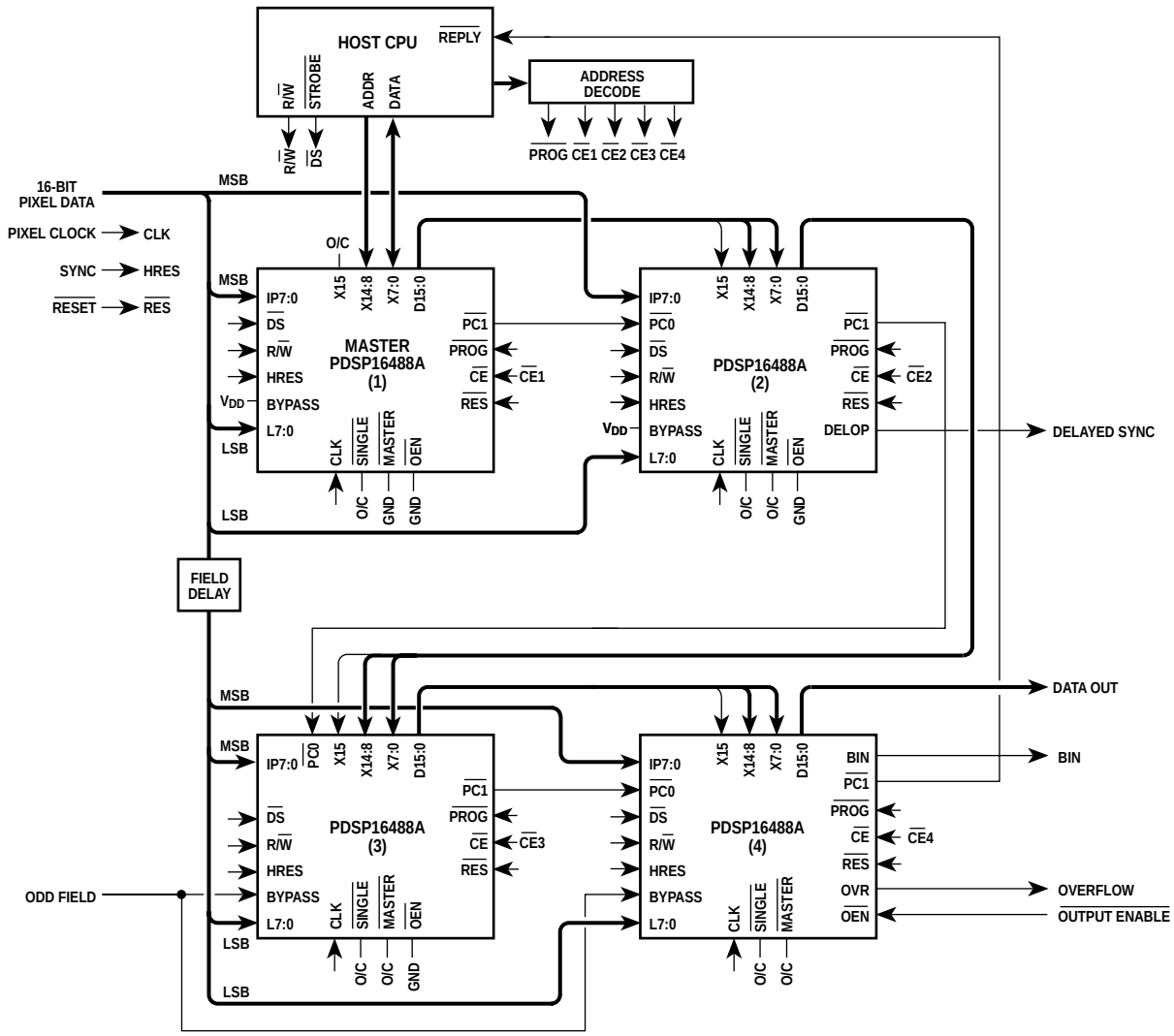


Fig. 18 Four device system with 16-bit pixels

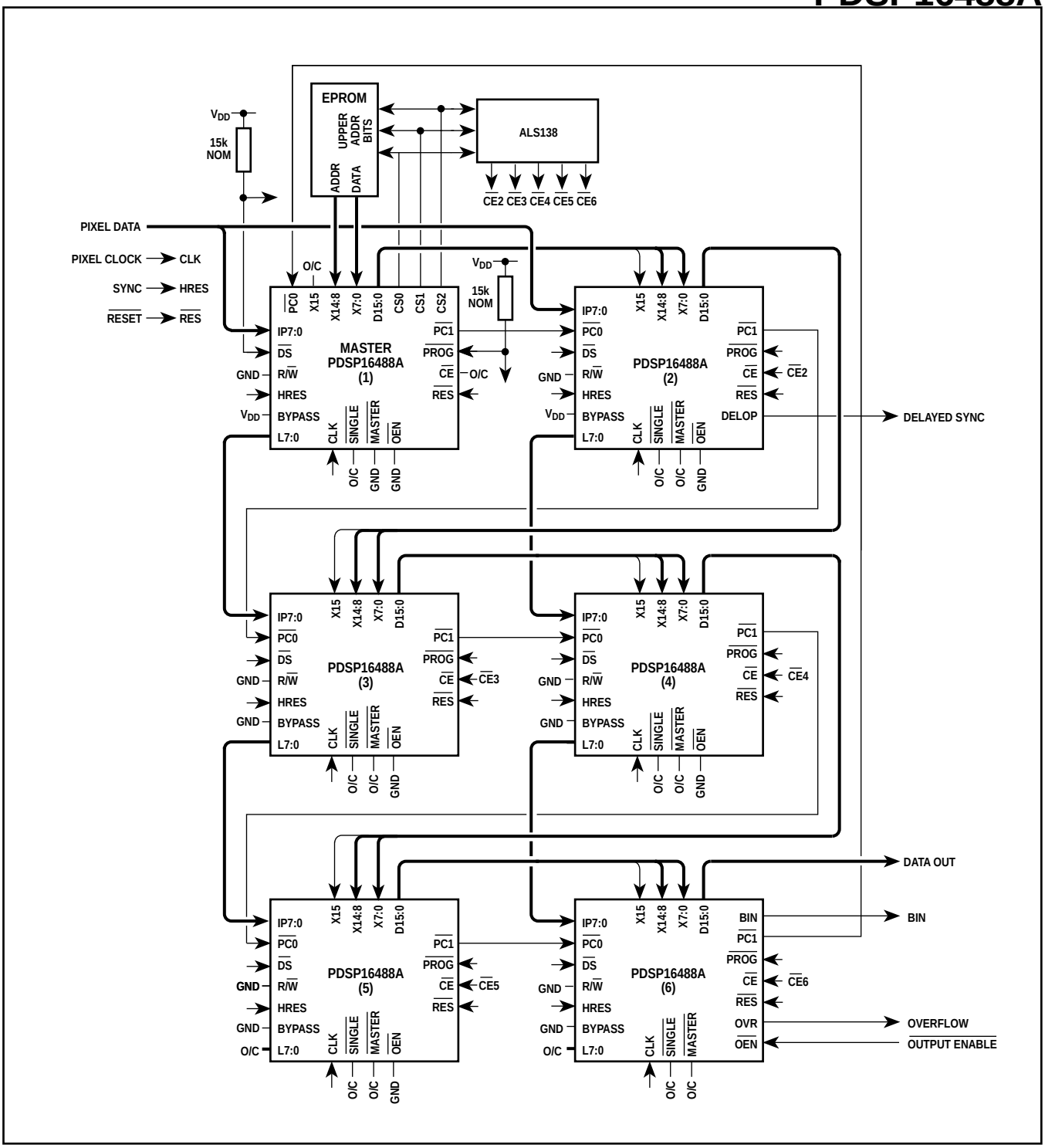


Fig. 19 Six device non-interlaced system.

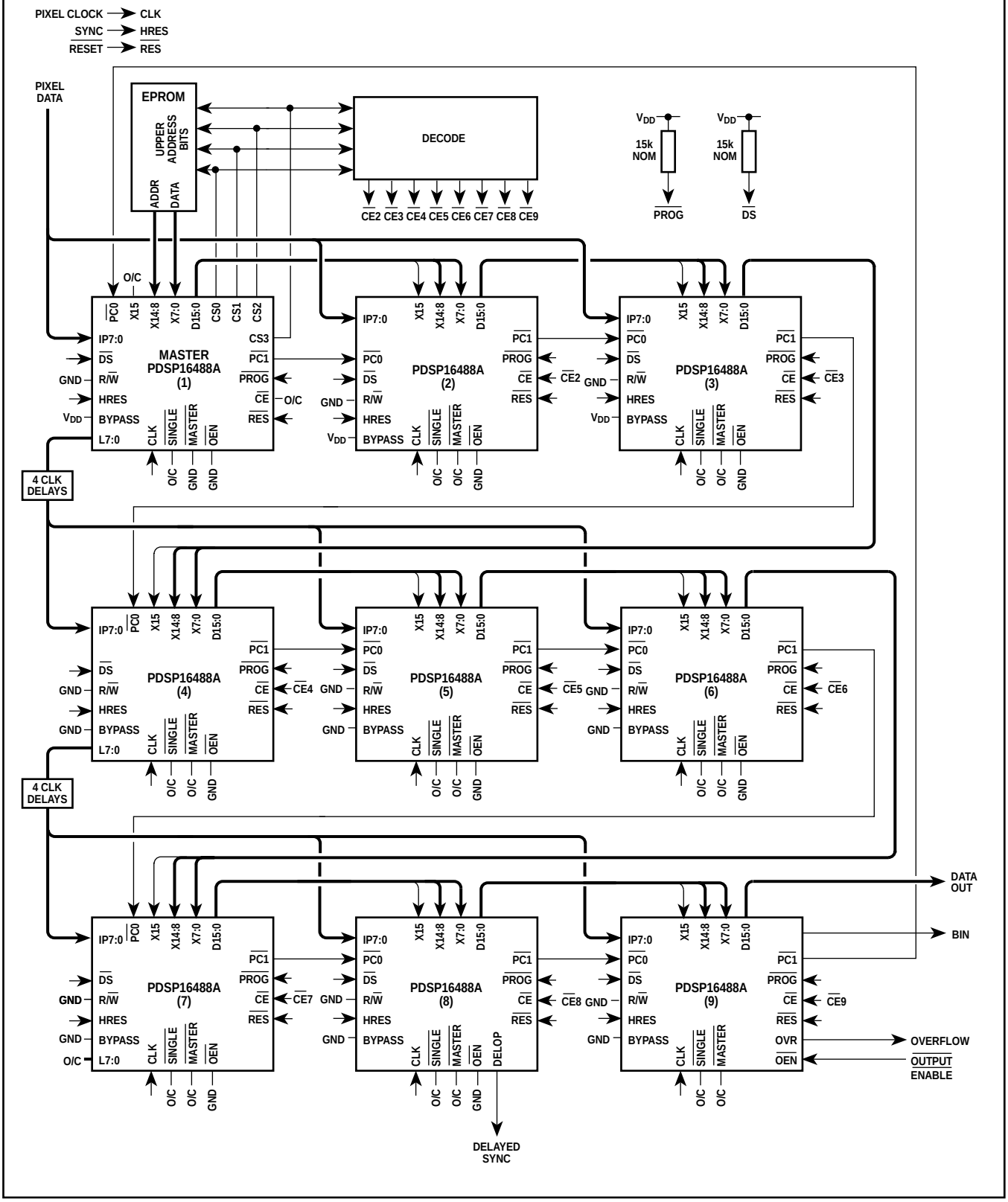


Fig. 20 Nine device non-interlaced system

BOND PAD No.	PIN REF.
1	A1
2	B1
3	C2
4	C1
5	D2
6	D1
7	E2
8	E1
9	F2
10	G2
11	G1
12	H2
13	J1
14	J2
15	K1
16	K2
17	L1

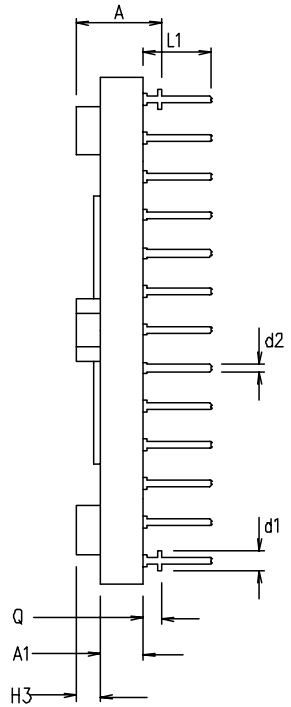
BOND PAD No.	PIN REF.
18	L2
19	M1
20	N1
21	N2
22	M3
23	N3
24	M4
25	N4
26	M5
27	N5
28	M6
29	M7
30	N7
31	M8
32	N9
33	M9
34	N10

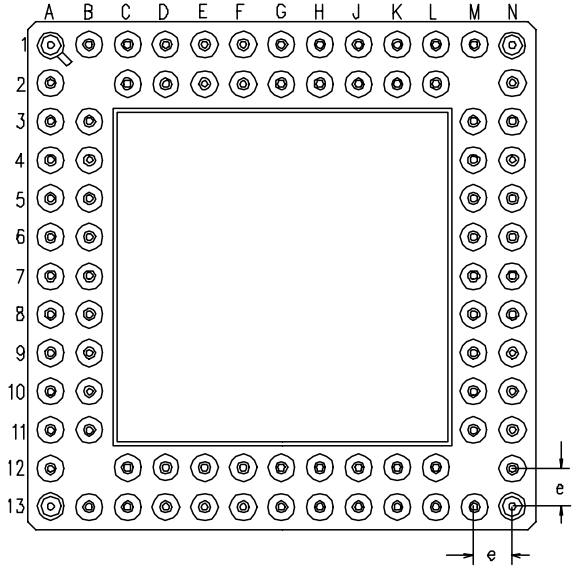
BOND PAD No.	PIN REF.
35	M10
36	N11
37	M11
38	N12
39	N13
40	M13
41	L12
42	L13
43	K12
44	K13
45	J12
46	J13
47	H12
48	G12
49	G13
50	F12
51	E13

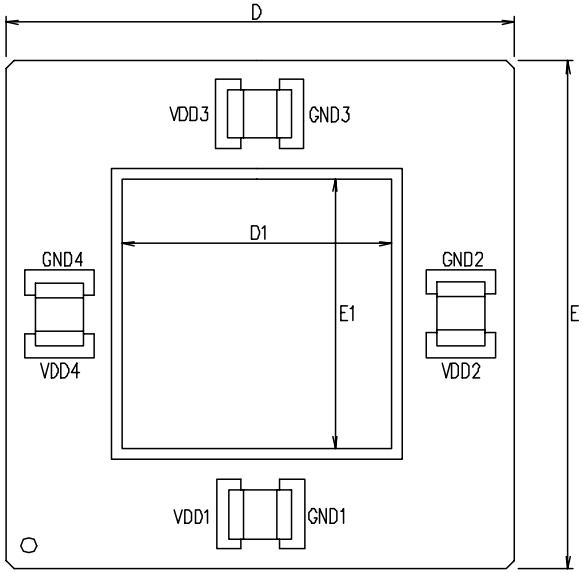
BOND PAD No.	PIN REF.
52	E12
53	D13
54	D12
55	C13
56	C12
57	B13
58	A13
59	A12
60	B11
61	A11
62	B10
63	A10
64	B9
65	A9
66	B8
67	B7
68	A7

BOND PAD No.	PIN REF.
69	B6
70	A5
71	B5
72	A4
73	B4
74	A3
75	B3
76	A2
GND1	H1
GND2	N8
GND3	H13
GND4	A8
VDD1	F1
VDD2	N6
VDD3	F13
VDD4	A6

S/R	NC
D/A	NC
H/S	NC







NOTES: –

1 H/S PLANE IS BELOW CAPACITOR HEIGHT

2 INDEX MARK INDICATES A1 REF CORNER & CAN BE ANY SHAPE

3 PLATING BARS CAN APPEAR IN VARIOUS POSITIONS & & SHOULD NOT BE USED FOR ORIENTATION PURPOSES

Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A			6.15				0.242
A1	2.52		3.08		0.099		0.121
Q	1.07		1.48		0.042		0.058
H3			1.60				0.063
D	33.23		33.84		1.308		1.332
D1	17.65		17.91		0.695		0.705
E	33.23		33.84		1.308		1.332
E1	17.65		17.91		0.695		0.705
e	2.54 REF				0.100 REF		
d1	1.14		1.40		0.045		0.055
d2	0.41		0.51		0.016		0.020
L1	4.27		4.88		0.168		0.192
	Pin features						
N	84						
NOTE	SQUARE						

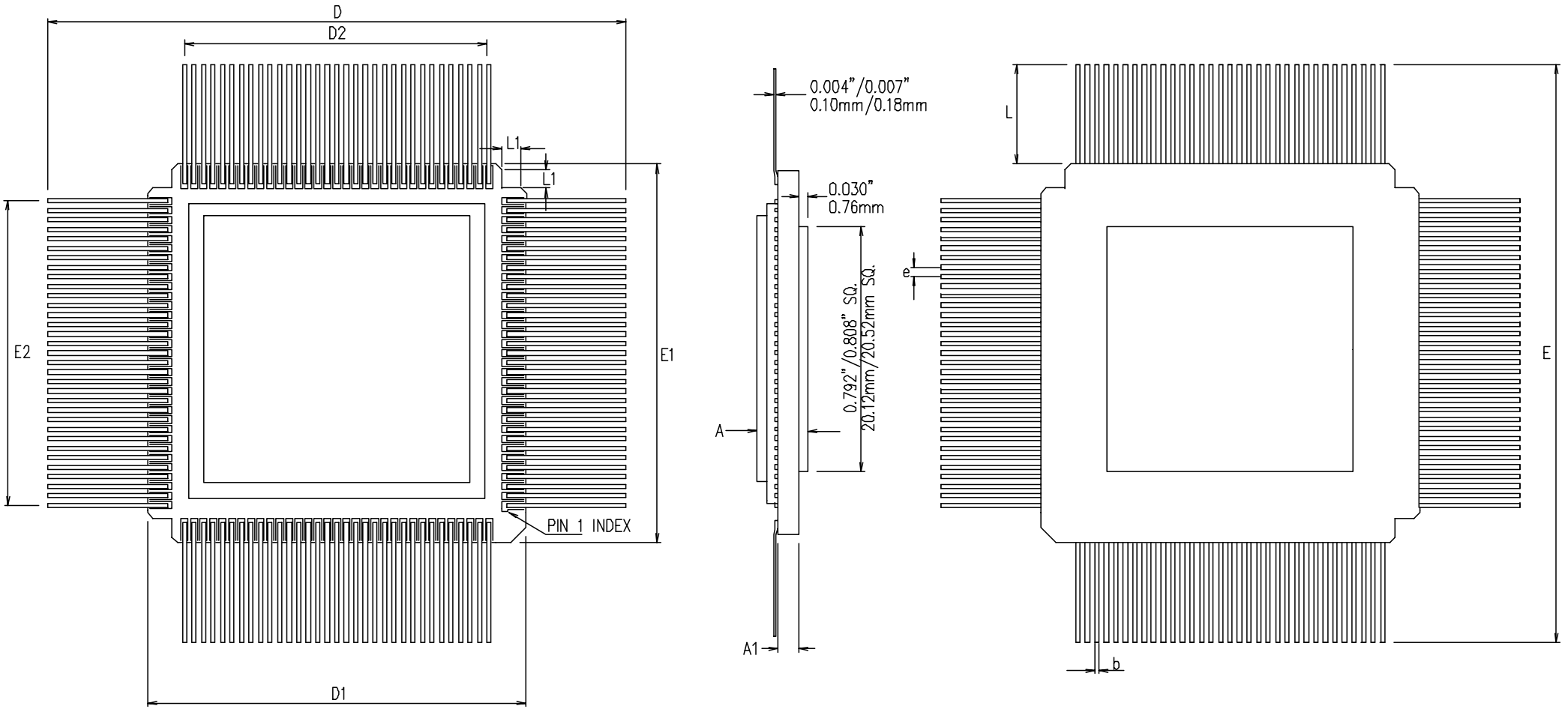
This drawing supersedes 418/ED/39506/102 issue 2 (Swindon)

ISSUE	1					
ACN	202177					
DATE	10.MAR.97					
APPD.						

ORIGINATING SITE: SWINDON

Title: Outline Drawing for 84 PGA (Power) (AC)

Drawing Number GPD00316



Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.92		3.33		0.115		0.131
A1	1.24		1.55		0.049		0.061
b	0.23		0.33		0.009		0.013
D	36.96		38.35		1.455		1.510
D1	24.00		24.38		0.945		0.960
D2		20.32				0.800	
E	36.96		38.35		1.455		1.510
E1	24.00		24.38		0.945		0.960
E2		20.32				0.800	
L	6.48		6.99		0.255		0.275
L1		1.27				0.050	
e	0.635 BSC				0.025 BSC		
	Pin features						
N	132						
N	33						
N	33						
NOTE	SQUARE						

NOTE:-

'A DIM' INCLUDES 0.018"/0.46mm (FOR LID (0.015"/0.38mm) + PREFORM (0.003"/0.08mm))

This drawing supersedes 418/ED/51407/001 issue 3 (Swindon)

							ORIGINATING SITE: SWINDON
ISSUE	1						Title: Outline Drawing for 132 LDCC Power (GC)
ACN	202184						
DATE	10.MAR.97						Drawing Number GPD00323
APPD.							

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