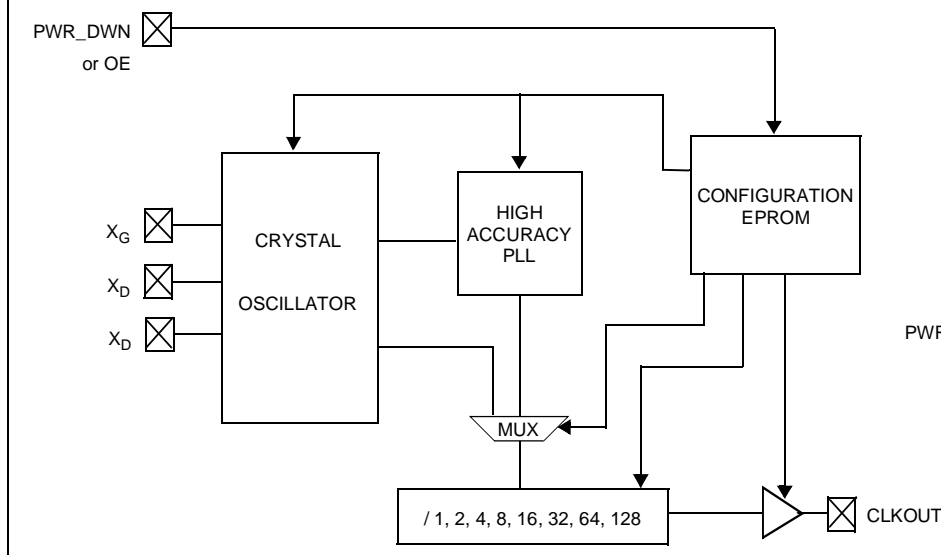




High Accuracy EPROM Programmable PLL Die for Crystal Oscillators

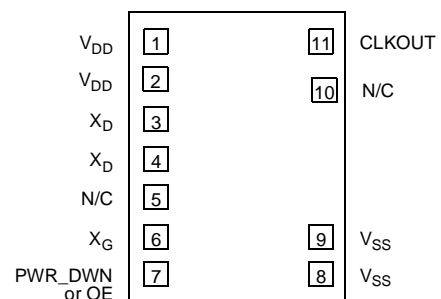
Features	Benefits
• EPROM-programmable die for in-package programming of crystal oscillators	Enables quick turnaround of custom oscillators Lowers inventory costs through stocking of blank parts
• High resolution PLL with 12 bit multiplier and 10 bit divider	Enables synthesis of highly accurate and stable output clock frequencies with zero or low PPM
• EPROM-programmable capacitor tuning array with Shadow register (Shadow register not enabled on CY2037-2)	Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal
• Twice programmable die	Enables reprogramming of programmed part, to correct errors, and control excess inventory
• Simple 4-wire programming interface	Enables programming of output frequency after packaging
• On-chip oscillator runs from 10–30 MHz crystal	Lowers cost of oscillator as PLL can be programmed to a high frequency using a low-frequency, low-cost crystal
• EPROM-selectable TTL or CMOS duty cycle levels	Duty cycle centered at 1.5V or $V_{DD}/2$ Provides flexibility to service most TTL or CMOS applications
• Operating frequency — 1–133 MHz at 5V — 1–100 MHz at 3.3V — 1–66.6 MHz at 2.7V	Services most PC, networking, and consumer applications
• Sixteen selectable post-divide options, using either PLL or reference oscillator output	Provides flexibility in output configurations and testing
• Programmable PWR_DWN or OE pin	Enables low-power operation or output enable function
• Programmable asynchronous or synchronous OE and PWR_DWN modes	Provides flexibility for system applications, through selectable instantaneous or synchronous change in outputs
• Low Jitter outputs typically — < ± 100 ps (pk-pk) at 5V and $f > 33$ MHz — < ± 125 ps (pk-pk) at 3.3V and $f > 33$ MHz	Suitable for most PC, consumer, and networking applications
• 3.3V or 5V operation	Lowers inventory cost as same die services both applications
• Small Die	Enables encapsulation in small-size, surface mount packages
• Controlled rise and fall times and output slew rate	Has lower EMI than oscillators

CY2037 Logic Block Diagram



Die Configuration

Top View



Functional Description

The CY2037 is an EPROM-programmable, high-accuracy, PLL-based die designed for the crystal oscillator market. The die attaches directly to a low-cost 10–30 MHz crystal and can be packaged into 4-pin through-hole or surface mount packages. The oscillator devices can be stocked as blank parts and custom frequencies programmed in-package at the last stage before shipping. This enables fast-turn manufacture of custom and standard crystal oscillators without the need for dedicated, expensive crystals.

The CY2037 contains an on-chip oscillator and a unique oscillator tuning circuit for fine-tuning of the output frequency. The crystal C_{load} can be selectively adjusted by programming a set of seven EPROM bits. This feature can be used to compensate for crystal variations or to obtain a more accurate synthesized frequency.

The CY2037 uses EPROM programming with a simple 2-wire, 4-pin interface that includes V_{SS} and V_{DD} . Clock outputs can be generated up to 133 MHz at 5V or up to 90 MHz at 3.3V. The entire configuration can be reprogrammed one time allowing programmed inventory to be altered or reused.

The CY2037 PLL die has been designed for very high resolution. It has a 12-bit feedback counter multiplier and a 10 bit reference counter divider. This enables the synthesis of highly accurate and stable output clock frequencies with zero or low PPM. The clock can be further modified by eight output divider options of 1, 2, 4, 8, 16, 32, 64 and 128. The divider input can be selected as either the PLL or crystal oscillator output providing a total of sixteen separate output options. For further flexibility, the output is selectable between TTL and CMOS duty cycle levels.

The CY2037 also contains flexible power management control. The part includes both PWR_DWN and OE features with integrated pull-up resistors. The PWR_DWN and OE modes have an additional setting to determine timing (asynchronous or synchronous) with respect to the output signal. When PWR_DWN or OE modes are enables, CLKOUT is pulled low by a weak pull down. The weak pull down is easily overdriven by another active CLKOUT for applications that require multiple CLKOUTs on a single signal path.

Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY2037 to have low jitter and accurate outputs making it suitable for most PC, networking and consumer applications

EPROM Configuration Block

The following table summarizes the features which are configurable by EPROM. Please refer to the “CY2037 Programming Specification” for further details. The specification can be obtained from your local Cypress representative.

EPROM Adjustable Features
Feedback counter value (P)
Reference counter value (Q)
Output divider selection
Oscillator Tuning (load capacitance values)
Duty cycle levels (TTL or CMOS)
Power management mode (OE or PWR_DWN)
Power management timing (synchronous or asynchronous)

PLL Output Frequency

The CY2037 contains a high resolution PLL with 12 bit multiplier and 10 bit divider. The output frequency of the PLL is determined by the following formula:

$$F_{PLL} = \frac{2 \cdot (P + 5)}{(Q + 2)} \cdot F_{REF}$$

where P is the feedback counter value and Q is the reference counter value. P and Q are EPROM programmable values.

Power Management Features

The CY2037 contains EPROM programmable PWR_DWN and OE functions. If Powerdown is selected, all active circuitry on the chip is shut down when the control pin goes LOW. The oscillator and PLL circuits must re-lock when the part leaves Powerdown Mode. If Output Enable mode is selected, the output is three-stated and weakly pulled low when the Control pin goes low. In this mode the oscillator and PLL circuits continue to operate, allowing a rapid return to normal operation when the Control input is deasserted.

In addition, the PWR_DWN and OE modes can be programmed to occur synchronously or asynchronously with respect to the output signal. When the asynchronous setting is used, the powerdown or output three-state occurs immediately (allowing for logic delays) irrespective of position in the clock cycle. However, when the synchronous setting is used, the part waits for a falling edge at the output before powerdown or output enable is initiated, thus preventing output glitches.

Crystal Oscillator Tuning Circuit

The CY2037 contains a unique tuning circuit to fine-tune the output frequency of the device. The tuning circuit consists of an array of eleven load capacitors on both sides of the oscillator drive inverter. The capacitor load values are EPROM programmable and can be increased in small increments. As the capacitor load is increased the circuit is fine-tuned to a lower frequency. The capacitor load values vary from 0.17 pF to 8 pF for a 100:1 total control ratio. The tuning increments are shown in the table on page 4.

Difference Between CY2037WAF and CY2307WAF-2

The CY2037WAF contains a shadow register in addition to the EPROM register. The shadow register is an exact copy of the EPROM register and is the default register when the Valid bit is not set. It is useful when the prototype or production envi-

ronment calls for measuring and adjusting the CLKOUT frequency numerous times. Multiple adjustments can be performed with the shadow register. Once the desired frequency is achieved the EPROM register is permanently programmed.

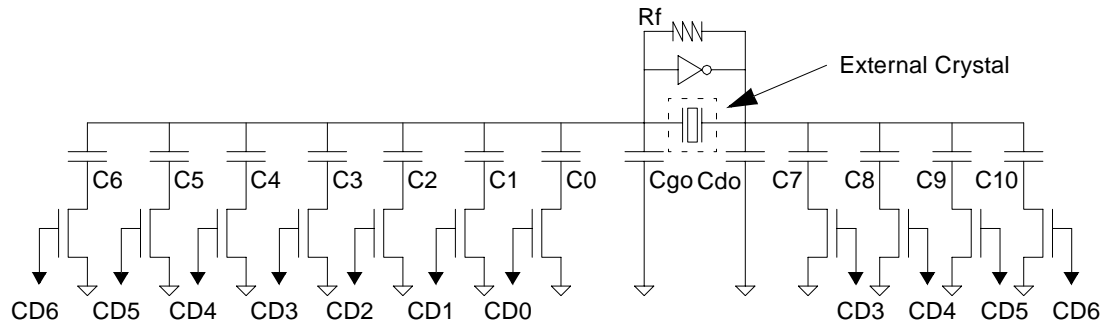
Some production flows do not require the use of the shadow register. If this is the case, then the CY2037WAF-2 is the device of choice. The CY2037WAF-2 has a disabled shadow register.

Die Pad Summary

Name	Die Pad	Description
V _{DD}	1,2	Voltage supply.
V _{SS}	8,9	Ground.
X _D	3,4	Crystal connection, drain pad. Bond to crystal drain.
X _G	6	Crystal connection, gate pad. Bond to crystal gate.
PWR_DWN / OE	7	EPROM programmable power down or output enable pad. Serves as V _{PP} in programming mode.
CLKOUT	11	Clock output. Also serves as three-state input during programming.
N/C	5,10	No Connect.

Device Functionality: Output Frequencies

Symbol	Description	Condition	Min.	Max.	Unit
Fo	Output frequency	V _{DD} = 4.5–5.5V	1	133	MHz
		V _{DD} = 3.0–3.6V	1	100	MHz
		V _{DD} = 2.7–3.6V	1	66.6	MHz

Crystal Oscillator Tuning Circuit


CD = EPROM BIT
 T = TRANSISTOR
 C = LOAD CAPACITOR

Symbol	Description	Min	Typ	Max	Unit
R_f	Feedback resistor, $V_{DD} = 4.5-5.5V$ Feedback resistor, $V_{DD} = 3.0-3.6V$	0.5 1.0	2 4	3.5 9.0	$M\Omega$ $M\Omega$
	Capacitors have $\pm 20\%$ Tolerance				
C_g	Gate capacitor		13		pF
C_d	Drain Capacitor		9		pF
C_0	Series Cap		0.27		pF
C_1	Series Cap		0.52		pF
C_2	Series Cap		1.00		pF
C_3	Series Cap		0.7		pF
C_4	Series Cap		1.4		pF
C_5	Series Cap		2.6		pF
C_6	Series Cap		5.0		pF
C_6	Series Cap		0.45		pF
C_8	Series Cap		0.85		pF
C_9	Series Cap		1.7		pF
C_{10}	Series Cap		3.3		pF

Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage -0.5 to +7.0V
 Input Voltage -0.5V to $V_{DD}+0.5V$

Storage Temperature (Non-Condensing) ... -55°C to +150°C
 Junction Temperature -40°C to +100°C
 Static Discharge Voltage >2000V
 (per MIL-STD-883, Method 3015)

Operating Conditions

Parameter	Description	Min.	Max.	Unit
AV_{DD}, V_{DD}	Analog and Digital Supply Voltage	2.7	5.5	V
T_{AJ} [1]	Operating Temperature, Junction	-40	+100	°C
C_{TTL}	Max. Capacitive Load on outputs for TTL levels $V_{DD} = 4.5-5.5V$, Output frequency = 1-40 MHz $V_{DD} = 4.5-5.5V$, Output frequency = 40-133 MHz		50 25	pF pF
C_{CMOS}	Max. Capacitive Load on outputs for CMOS levels $V_{DD} = 4.5-5.5V$, Output frequency = 1-66.6 MHz $V_{DD} = 4.5-5.5V$, Output frequency = 66.6-133 MHz $V_{DD} = 3.0-3.6V$, Output frequency = 1-40 MHz $V_{DD} = 3.0-3.6V$, Output frequency = 40-100 MHz $V_{DD} = 2.7-3.6V$, Output frequency = 1-40 MHz		50 25 30 15 15	pF pF pF pF pF
X_{REF}	Reference Frequency, input crystal	10	30	MHz

Electrical Characteristics Over the Operating Range (Part was characterized in a 20 pin SOIC package with external crystal, Electrical Characteristics may change with other package types)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level Input Voltage	$V_{DD} = 4.5-5.5V$ $V_{DD} = 3.0-3.6V$ $V_{DD} = 2.7-3.6V$			0.8 0.2 V_{DD} 0.2 V_{DD}	V V V
V_{IH}	High-level Input Voltage	$V_{DD} = 4.5-5.5V$ $V_{DD} = 3.0-3.6V$ $V_{DD} = 2.7-3.6V$	2.0 0.7 V_{DD} 0.7 V_{DD}			V V V
V_{OL}	Low-level Output Voltage	$V_{DD} = 4.5-5.5V, I_{OL} = 16\text{ mA}$ $V_{DD} = 3.0-3.6V, I_{OL} = 8\text{ mA}$ $V_{DD} = 2.7-3.6V, I_{OL} = 8\text{ mA}$			0.4 0.4 0.4	V V V
V_{OHCMOS}	High-level Output Voltage, CMOS levels	$V_{DD} = 4.5-5.5V, I_{OH} = -16\text{ mA}$ $V_{DD} = 3.0-3.6V, I_{OH} = -8\text{ mA}$ $V_{DD} = 2.7-3.6V, I_{OH} = -8\text{ mA}$	$V_{DD}-0.4$ $V_{DD}-0.4$ $V_{DD}-0.4$			V V V
V_{OHTTL}	High-level Output Voltage, TTL levels	$V_{DD} = 4.5-5.5V, I_{OH} = -16\text{ mA}$	2.4			V
I_{IL}	Input Low Current	$V_{IN} = 0V$			10	μA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$			5	μA
I_{DD}	Power Supply Current, Unloaded	$V_{DD} = 4.5-5.5V$, Output frequency $\leq 133\text{ MHz}$ $V_{DD} = 2.7-3.6V$, Output frequency $\leq 100\text{ MHz}$			45 25	mA mA
I_{DDS}	Stand-by current	$V_{DD} = 2.7-3.6V$		10	50	μA
R_{UP}	Input Pull-Up Resistor	$V_{DD} = 4.5-5.5V, V_{IN} = 0V$ $V_{DD} = 4.5-5.5V, V_{IN} = 0.7V_{DD}$	1.1 50	3.0 100	8.0 200	M Ω k Ω
I_{OE_CLKOUT}	CLKOUT Pull-Down Current	$V_{DD}=5.0$		20		μA

Note:

1. This product is sold in die form so operating conditions are specified for the die, or junction temperature.

Output Clock Switching Characteristics Over the Operating Range

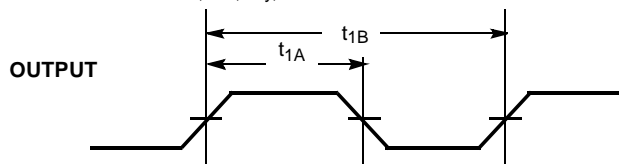
Symbol	Description	Test Conditions	Min	Typ	Max	Unit
t _{1w}	Output Duty Cycle at 1.4V, V _{DD} = 4.5–5.5V t _{1w} = t _{1A} ÷ t _{1B}	1–50 MHz, C _L ≤ 50 pF	45		55	%
		50–66 MHz, C _L ≤ 15 pF	45		55	%
		66–125 MHz, C _L ≤ 25 pF	40		60	%
		125–133 MHz, C _L ≤ 15 pF	40		60	%
t _{1x}	Output Duty Cycle at V _{DD} /2, V _{DD} = 4.5–5.5V t _{1x} = t _{1A} ÷ t _{1B}	1–66.6 MHz, C _L ≤ 25 pF	45		55	%
		66.6–125 MHz, C _L ≤ 25 pF	40		60	%
		125–133 MHz, C _L ≤ 15 pF	40		60	%
t _{1y}	Output Duty Cycle at V _{DD} /2, V _{DD} = 3.0–3.6V t _{1y} = t _{1A} ÷ t _{1B}	1–40 MHz, C _L ≤ 30 pF	45		55	%
		40–100 MHz, C _L ≤ 15 pF	40		60	%
t _{1z}	Output Duty Cycle at V _{DD} /2, V _{DD} = 2.7–3.6V t _{1z} = t _{1A} ÷ t _{1B}	1–40 MHz, C _L ≤ 15 pF	40		60	%
		40–66.6 MHz, C _L ≤ 15 pF	40		60	%
t ₂	Output Clock Rise Time	Between 0.8 –2.0V, V _{DD} = 4.5V–5.5V, C _L = 50 pF			1.8	ns
		Between 0.8 –2.0V, V _{DD} = 4.5V–5.5V, C _L = 25 pF			1.2	ns
		Between 0.8 –2.0V, V _{DD} = 4.5V–5.5V, C _L = 15 pF			0.9	ns
		Between 0.2V _{DD} – 0.8V _{DD} , V _{DD} = 4.5V–5.5V, C _L = 50 pF			3.4	ns
		Between 0.2V _{DD} – 0.8V _{DD} , V _{DD} = 3.0V–3.6V, C _L = 30 pF			4.0	ns
		Between 0.2V _{DD} – 0.8V _{DD} , V _{DD} = 3.0V–3.6V, C _L = 15 pF			2.4	ns
		Between 0.2V _{DD} – 0.8V _{DD} , V _{DD} = 2.7V–3.6V, C _L = 15 pF			4.0	ns
t ₃	Output Clock Fall Time	Between 0.8V–2.0V, V _{DD} = 4.5V–5.5V, C _L = 50 pF			1.8	ns
		Between 0.8 –2.0V, V _{DD} = 4.5V–5.5V, C _L = 25 pF			1.2	ns
		Between 0.8 –2.0V, V _{DD} = 4.5V–5.5V, C _L = 15 pF			0.9	ns
		Between 0.2V _{DD} – 0.8V _{DD} , V _{DD} = 4.5V–5.5V, C _L = 50 pF			3.4	ns
		Between 0.2V _{DD} – 0.8V _{DD} , V _{DD} = 3.0V–3.6V, C _L = 30 pF			4.0	ns
		Between 0.2V _{DD} – 0.8V _{DD} , V _{DD} = 3.0V–3.6V, C _L = 15 pF			2.4	ns
		Between 0.2V _{DD} – 0.8V _{DD} , V _{DD} = 2.7V–3.6V, C _L = 15 pF			4.0	ns
t ₄	Start-Up Time Out of Power-Down	PWR_DWN or OE pin LOW to HIGH ^[2]		1	2	ms
t _{5a}	Power Down Delay Time (synchronous setting)	PWR_DWN pin HIGH to output LOW (T=frequency oscillator period)		T/2	T+10	ns
t _{5b}	Power Down Delay Time (asynchronous setting)	PWR_DWN pin HIGH to output LOW		10	15	ns
t ₆	Power Up Time	From power on ^[2]		1	2	ms
t _{7a}	Output Disable Time (synchronous setting)	OE pin HIGH to output Hi-Z (T=frequency oscillator period)		T/2	T+10	ns
t _{7b}	Output Disable Time (asynchronous setting)	OE pin HIGH to output Hi-Z		10	15	ns
t ₈	Output Enable Time	PWR_DWN or OE pin LOW to HIGH			100	ns
t ₉	Peak-to-Peak Period Jitter	V _{DD} = 4.5V–5.5V, F _o > 33 MHz, VCO > 100 MHz		±100	±125	ps
		V _{DD} = 3.0V–3.6V, F _o > 33 MHz, VCO > 100 MHz		±125	±200	ps
		V _{DD} = 3.0V–5.5V, F _o < 33 MHz		±250	1% of F _O	ps

Note:

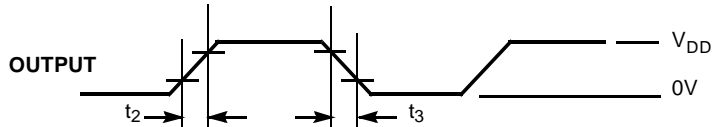
- Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70 ohms.

Switching Waveforms

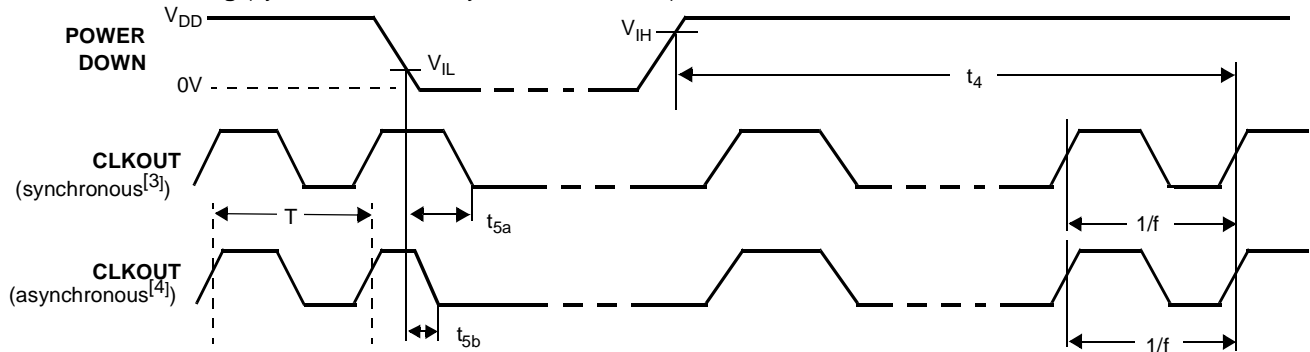
Duty Cycle Timing (t_{1w} , t_{1x} , t_{1y} , t_{1z})



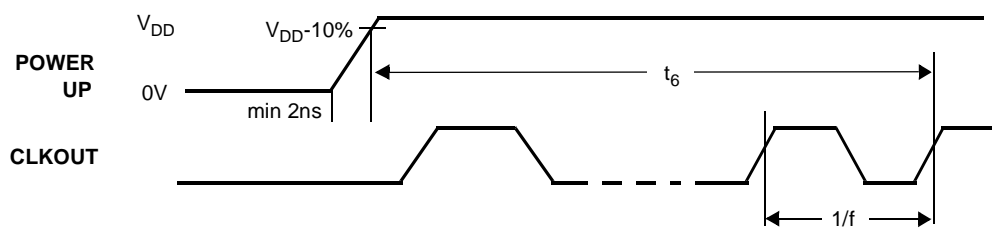
Output Rise/Fall Time



Power Down Timing (synchronous and asynchronous modes)



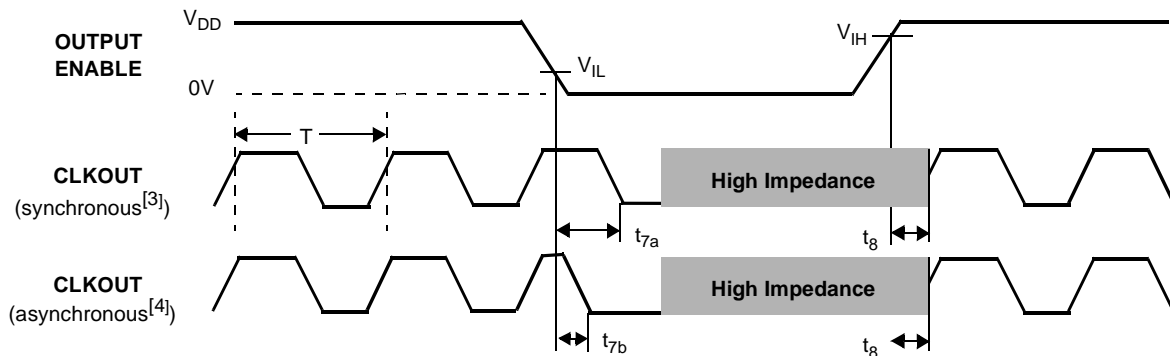
Power Up Timing



Notes:

3. In synchronous mode the powerdown or output three-state is not initiated until the next falling edge of the output clock.
4. In asynchronous mode the powerdown or output three-state occurs within 25 ns irrespective of position in the output clock cycle.

Switching Waveforms (continued)

Output Enable Timing (synchronous and asynchronous modes)

Ordering Information

Ordering Code	Type	Operating Range
CY2037AWAF	Wafer	Industrial
CY2037-2WAF	Wafer	Industrial

*NOTE: The only difference between the CY2037AWAF and the CY2037-2WAF is: The CY2037-2WAF has the shadow register disabled.

Die Size Dimensions

x by y	1497x1105 microns
Wafer Thickness	14 ±0.5 mils

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