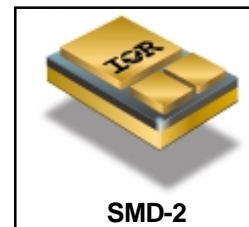


**RADIATION HARDENED  
 POWER MOSFET  
 SURFACE MOUNT (SMD-2)**

**IRHNA57160  
 100V, N-CHANNEL  
 R5 TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	RDS(on)	ID
IRHNA57160	100K Rads (Si)	0.012Ω	75*A
IRHNA53160	300K Rads (Si)	0.012Ω	75*A
IRHNA54160	600K Rads (Si)	0.012Ω	75*A
IRHNA58160	1000K Rads (Si)	0.013Ω	75*A



International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm<sup>2</sup>)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

**Features:**

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight

**Absolute Maximum Ratings**

**Pre-Irradiation**

	Parameter		Units
ID @ VGS = 12V, TC = 25°C	Continuous Drain Current	75*	A
ID @ VGS = 12V, TC = 100°C	Continuous Drain Current	69	
IDM	Pulsed Drain Current ①	300	
PD @ TC = 25°C	Max. Power Dissipation	300	W
	Linear Derating Factor	2.4	W/°C
VGS	Gate-to-Source Voltage	±20	V
EAS	Single Pulse Avalanche Energy ②	363	mJ
IAR	Avalanche Current ①	75	A
EAR	Repetitive Avalanche Energy ①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.0	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	3.3 (Typical)	g

\* Current is limited by internal wire diameter  
 For footnotes refer to the last page

**Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	0.115	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.013	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> = 75A ④
		—	—	0.012		V <sub>GS</sub> = 12V, I <sub>D</sub> = 69A
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
g <sub>fs</sub>	Forward Transconductance	42	—	—	S (r <sub>l</sub> )	V <sub>DS</sub> > 15V, I <sub>DS</sub> = 69A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	10	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
		—	—	25		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	—	160	nC	V <sub>GS</sub> = 12V, I <sub>D</sub> = 75A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	55		V <sub>DS</sub> = 50V
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	65		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	35	ns	V <sub>DD</sub> = 50V, I <sub>D</sub> = 75A, V <sub>GS</sub> = 12V, R <sub>G</sub> = 2.35Ω
t <sub>r</sub>	Rise Time	—	—	125		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	75		
t <sub>f</sub>	Fall Time	—	—	50		
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C <sub>iss</sub>	Input Capacitance	—	6440	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1660	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	60	—		

**Source-Drain Diode Ratings and Characteristics**

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	75*	A	
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	300		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>j</sub> = 25°C, I <sub>S</sub> = 75A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	300	nS	T <sub>j</sub> = 25°C, I <sub>F</sub> = 35A, di/dt ≤ 100A/μs
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	2.2	μC	V <sub>DD</sub> ≤ 25V ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

\* Current is limited by internal wire diameter

**Thermal Resistance**

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJC</sub>	Junction-to-Case	—	—	0.42	°C/W	soldered to a 2" square copper-clad board
R <sub>thJ-PCB</sub>	Junction-to-PC board	—	1.6	—		

**Note:** Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

## Radiation Characteristics

IRHNA57160

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

	Parameter	Up to 600K Rads(Si) <sup>1</sup>		1000K Rads (Si) <sup>2</sup>		Units	Test Conditions
		Min	Max	Min	Max		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	4.0	1.5	4.0		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1.0mA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100	—	-100		V <sub>GS</sub> = -20V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	10	—	10	μA	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.013	—	0.014	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> =45A
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (SMD-2)	—	0.012	—	0.013	Ω	V <sub>GS</sub> = 12V, I <sub>D</sub> =45A
V <sub>SD</sub>	Diode Forward Voltage ④	—	1.2	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 45A

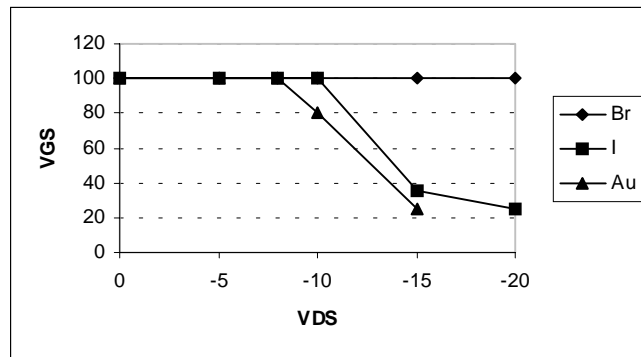
1. Part numbers IRHNA57160, IRHNA53160 and IRHNA54160

2. Part number IRHNA58160

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Single Event Effect Safe Operating Area**

Ion	LET MeV/(mg/cm <sup>2</sup> )	Energy (MeV)	Range (μm)	V <sub>DS</sub> (V)				
				@ V <sub>GS</sub> = 0V	@ V <sub>GS</sub> = -5V	@ V <sub>GS</sub> = -10V	@ V <sub>GS</sub> = -15V	@ V <sub>GS</sub> = -20V
Br	36.7	309	39.5	100	100	100	100	100
I	59.8	341	32.5	100	100	100	35	25
Au	82.3	350	28.4	100	100	80	25	—



**Fig a. Single Event Effect, Safe Operating Area**

For footnotes refer to the last page

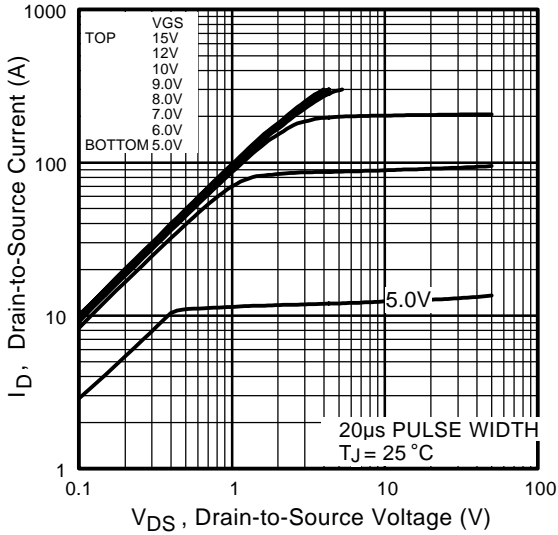


Fig 1. Typical Output Characteristics

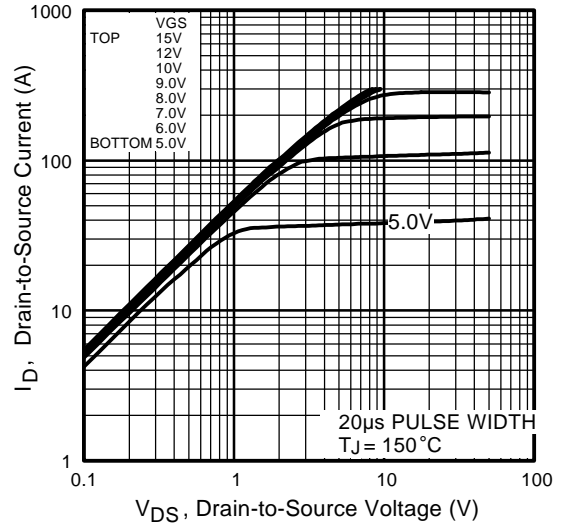


Fig 2. Typical Output Characteristics

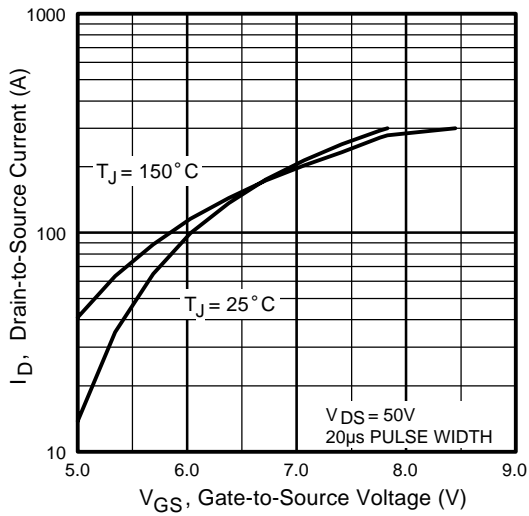


Fig 3. Typical Transfer Characteristics

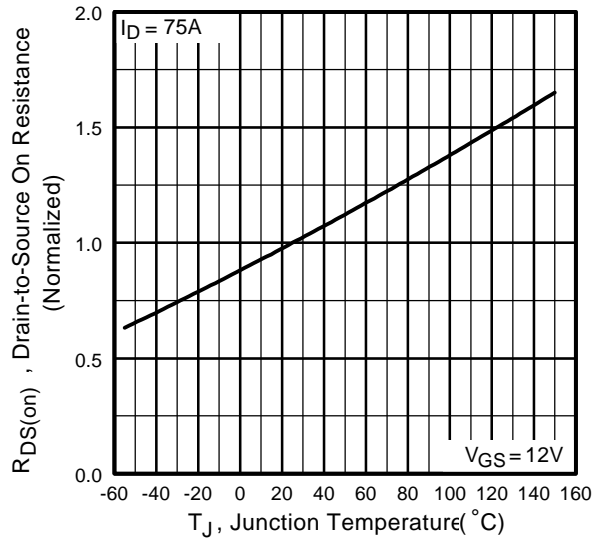
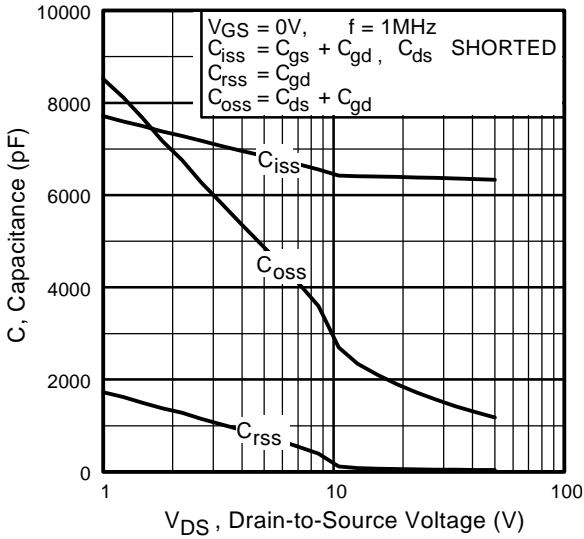
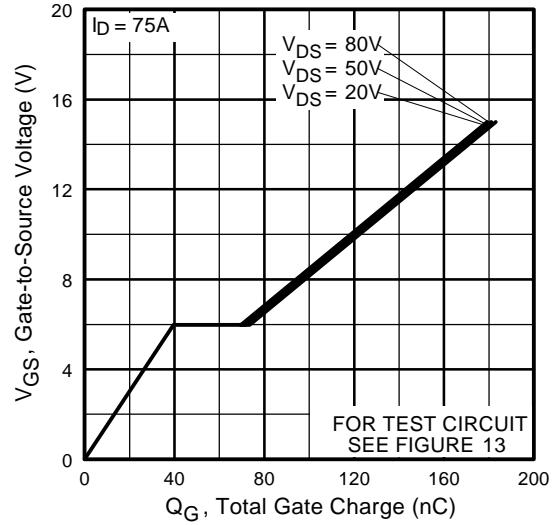


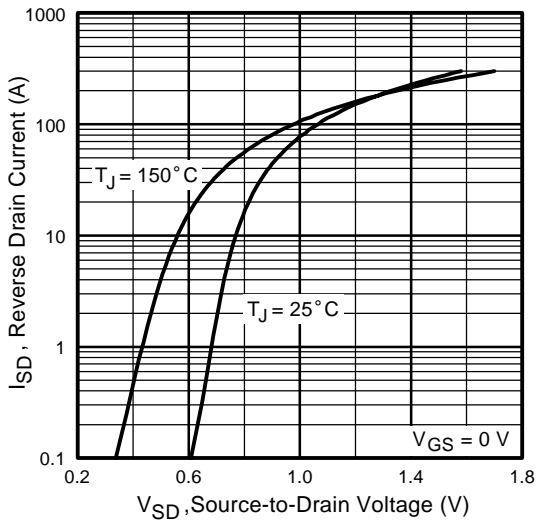
Fig 4. Normalized On-Resistance Vs. Temperature



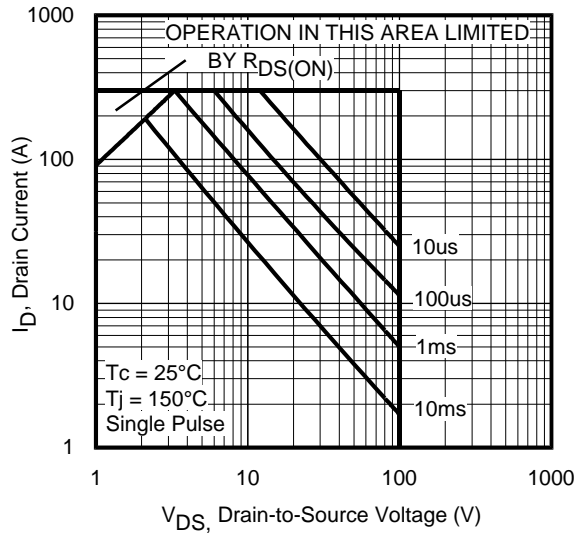
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



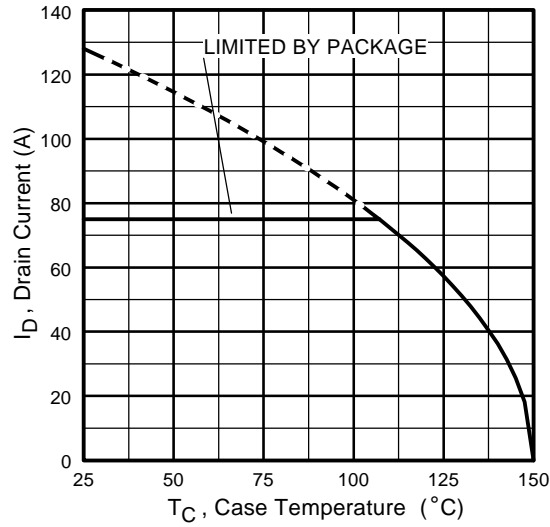
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



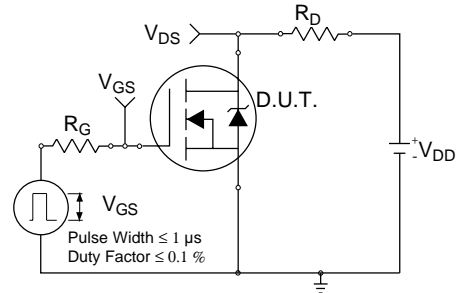
**Fig 7.** Typical Source-Drain Diode Forward Voltage



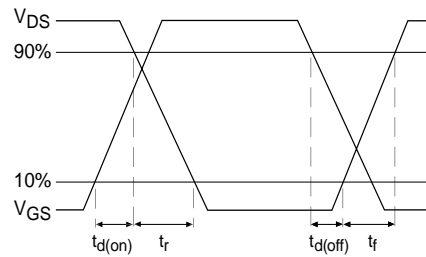
**Fig 8.** Maximum Safe Operating Area



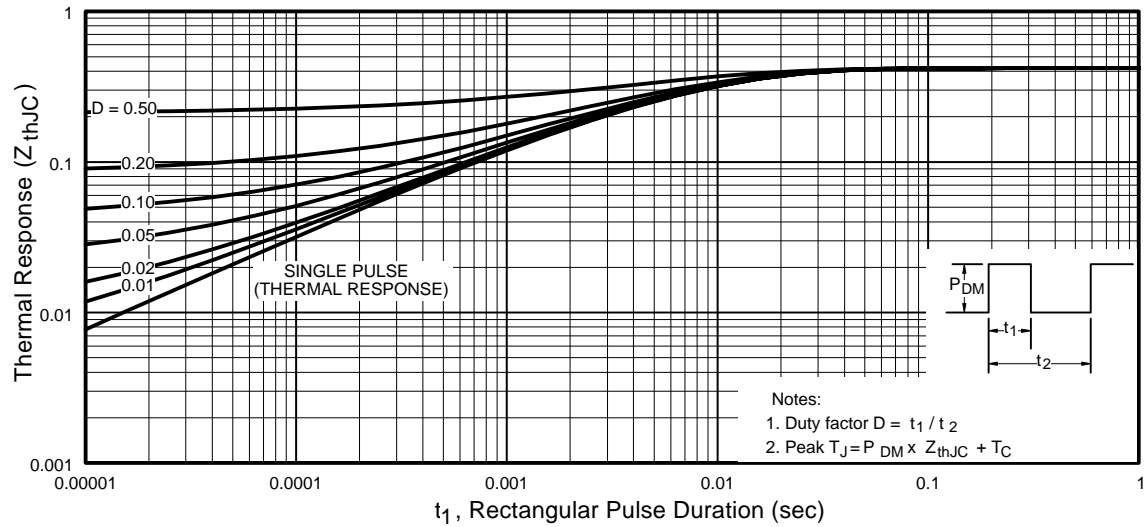
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

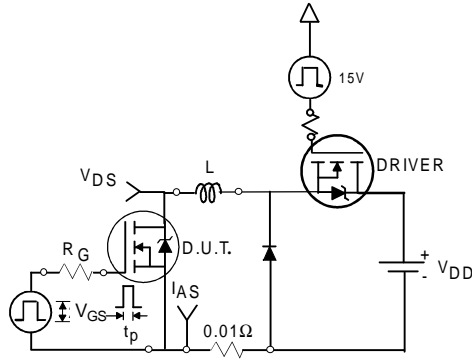


Fig 12a. Unclamped Inductive Test Circuit

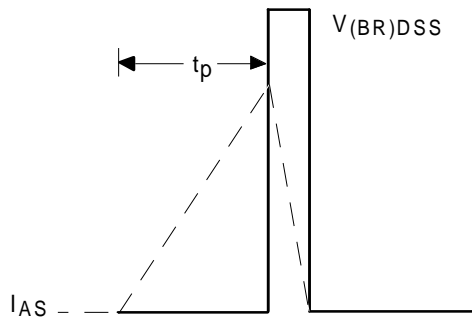


Fig 12b. Unclamped Inductive Waveforms

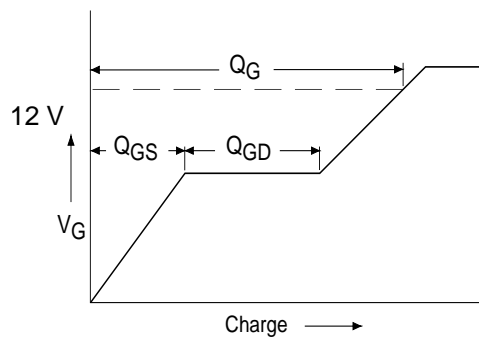


Fig 13a. Basic Gate Charge Waveform

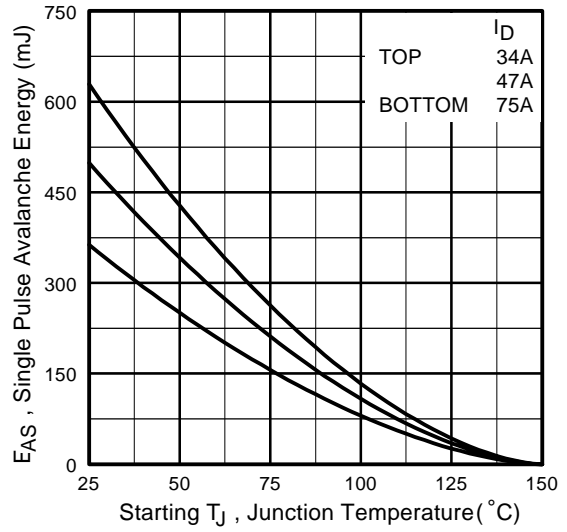


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

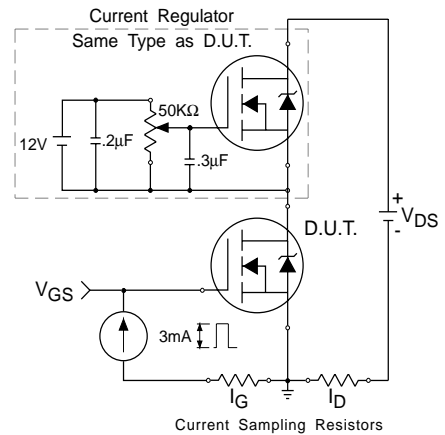
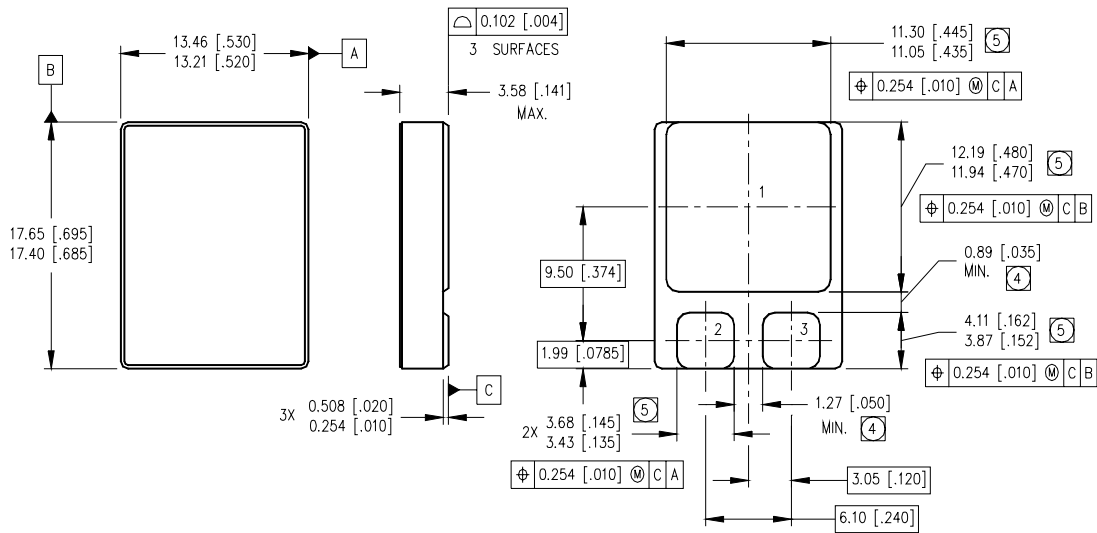


Fig 13b. Gate Charge Test Circuit

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = 50V$ , starting  $T_J = 25^\circ C$ ,  $L = 0.13\text{ mH}$   
Peak  $I_L = 75A$ ,  $V_{GS} = 12V$
- ③  $ISD \leq 75A$ ,  $di/dt \leq 340A/\mu s$ ,  
 $V_{DD} \leq 100V$ ,  $T_J \leq 150^\circ C$
- ④ Pulse width  $\leq 300\ \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤ **Total Dose Irradiation with VGS Bias.**  
12 volt  $V_{GS}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with VDS Bias.**  
80 volt  $V_{DS}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A.

**Case Outline and Dimensions — SMD-2**



**NOTES:**

- 1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
- 2. CONTROLLING DIMENSION: INCH.
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- ④ DIMENSION INCLUDES METALLIZATION FLASH.
- ⑤ DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

**PAD ASSIGNMENTS**

- 1 = DRAIN
- 2 = GATE
- 3 = SOURCE



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TAC Fax: (310) 252-7903

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