



LB1896

3-phase Brushless Motor Driver for CD-ROM Spindle Drive Use

Overview

The LB1896 is a 3-phase brushless motor driver IC that is ideal for driving CD-ROM spindle motors.

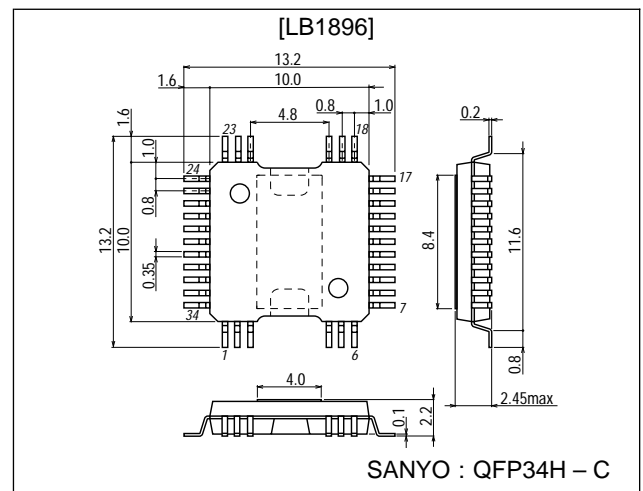
Functions and Features

- 120° voltage linear technique
- V-type control voltage
- Switchable control gain
- Control, noncontrol, acceleration/deceleration mode select pins built in.
- Start/Stop pin built in, Hall bias built in.

Package Dimensions

unit : mm

3219-QFP34H-C



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|-----------------------|----------------|-------------|------|
| Maximum supply voltage | $V_{CC1 \text{ max}}$ | | 20 | V |
| | $V_{CC2 \text{ max}}$ | | 7.0 | V |
| Applied output voltage | $V_{OU, V, W}$ | | 20 | V |
| Output current | I_{OUT} | | 1.2 | A |
| Allowable power dissipation | $P_d \text{ max}$ | Independent IC | 0.77 | W |
| Operating temperature | T_{opr} | | -20 to +75 | °C |
| Storage temperature | T_{stg} | | -55 to +150 | °C |

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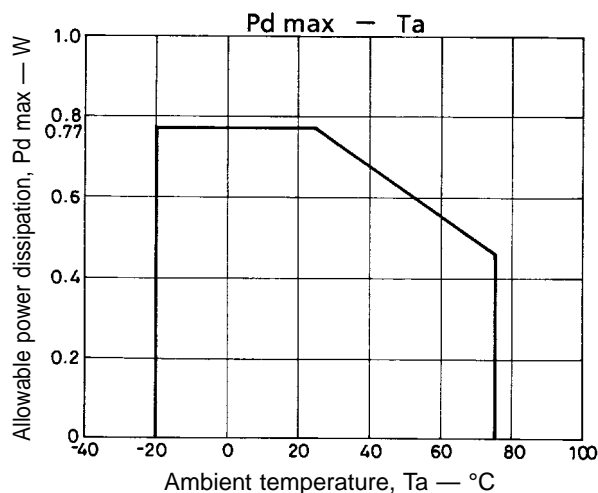
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13096HA(II) No.5225-1/8

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Operating Conditions at Ta = 25 °C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---------------------------------|-------------------|-------------------------------------|----------------------------|------|
| Supply voltage | V _{CC1} | | 5 to 18 | V |
| | V _{CC2} | V _{CC1} ≥ V _{CC2} | 4.3 to 6.5 | V |
| V _{Cref} input voltage | V _{Cref} | | V _{CC2} /2 ±1.0 | V |
| V _{NS} input voltage | V _{NS} | | 0 to V _{CC2} -1.0 | V |



Electrical Characteristics at Ta = 25 °C, V_{CC1} = 12 V, V_{CC2} = 5 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--|-------------------------|---|------|------|------|------|
| Supply current 1 | I _{CC1} | V _C = open, V _{Cref} = open, R _L = ∞, V _{S/S} = 5 V | | 17 | 30 | mA |
| Supply current 2 | I _{CC2} | V _C = open, V _{Cref} = open | | 7.5 | 10.5 | mA |
| Supply current 3 | I _{CC3} | V _C = open, V _{Cref} = open, R _L = ∞, V _{S/S} = 0 V, (I _{CC} of V _{CC1}) | | 0.9 | 3 | mA |
| [Drive block] | | | | | | |
| Output saturation voltage | V _{O(sat)1} | I _{OUT} = 0.4 A, sink + source | | 1.6 | 2.2 | V |
| | V _{O(sat)2} | I _{OUT} = 0.8 A, sink + source | | 2.0 | 3.0 | V |
| Output TRS sustaining voltage | V _{O(sus)} | I _{OUT} = 20 mA | 20 | | | V |
| Output static voltage | V _{OQ} | V _C = 2.5 V, V _{Cref} = 2.5 V | 5.7 | 6.0 | 6.3 | V |
| Hall amplifier input offset voltage | V _{H offset} | | -5 | | +5 | mV |
| Hall amplifier input bias current | I _{H bias} | | | 1 | 5 | μA |
| Hall amplifier common-mode input voltage range | V _{Hch} | | 1.3 | | 2.2 | V |
| Hall input/output voltage gain | G _{VHO} | | 40 | 43 | 46 | dB |
| Control/output drive gain 1 | G _{VCO1} | RZ1 = RZ2, GC1 = L, GC2 = L | 26 | 29 | | dB |
| Control/output channel difference 1 | ΔG _{VCO1} | RZ1 = RZ2, GC1 = L, GC2 = L | -1.5 | | +1.5 | dB |
| Control/output drive gain 2 | G _{VCO2} | RZ1 = RZ2, GC1 = L, GC2 = H | 32 | 35 | | dB |
| Control/output channel difference 2 | ΔG _{VCO2} | RZ1 = RZ2, GC1 = L, GC2 = H | -1.9 | | +1.9 | dB |
| Input dead zone voltage | V _{DZ} | RZ1 = RZ2, GC1 = L, GC2 = L V _O (voltage between out and out) = 0.1 V | ±13 | ±38 | ±55 | mV |
| Input bias current 1 | I _{B SERVO} | V _C = 1.0 V | | | 500 | nA |
| Input bias current 2 | I _{B n.s} | V _{NS} = 1.0 V | | | 500 | nA |
| S/S pin high voltage | V _{S/S H} | Input is CMOS level | 4 | | | V |
| S/S pin low voltage | V _{S/S L} | Note) S/S pin V _{th} = V _{CC2} /2 | | | 1 | V |
| Gain control 1 high voltage | V _{GC1 H} | Input is at CMOS level. | 4 | | | V |
| Gain control 1 low voltage | V _{GC1 L} | Note) GC1 pin V _{th} = 2.0 V | | | 1 | V |
| Gain control 2 high voltage | V _{GC2 H} | Input is at CMOS level. | 4 | | | V |
| Gain control 2 low voltage | V _{GC2 L} | Note) GC2 pin V _{th} = 2.0 V | | | 1 | V |
| S/S pin input current | I _{S/S} | Input voltage = 5 V | | 50 | 100 | μA |
| Gain control 1, 2 current | I _{GC} | Input voltage = 5 V | | 53 | 110 | μA |
| Rotation output saturation voltage | V _{(sat) H.FG} | I _O = -5 mA | | 0.24 | 0.5 | V |
| Rotation output saturation sustaining voltage | V _{(sus) H.FG} | | | | 7 | V |

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| Parameter | Symbol | Conditions | min | typ | max | Unit |
|-----------------------|--------------------|---|-----|------|-----|--------------------|
| Hall bias voltage | $V_{H\pm}$ | $I_O = 5 \text{ mA}$, $R_H = 200 \ \Omega$ | 0.7 | 0.97 | 1.2 | V |
| CTRL pin high voltage | $V_{CTRL\ H}$ | Common for CTRL1 and CTRL2 input CMOS level | 4 | | | V |
| CTRL pin low voltage | $V_{CTRL\ L}$ | Note) CTRL pin $V_{th} = 2.5 \text{ V}$ | | | 1.0 | V |
| CTRL input current | I_{CTRL} | Input voltage = 5 V | | 53 | 110 | μA |
| TSD operation voltage | TSD | Design target | 150 | 180 | 210 | $^{\circ}\text{C}$ |
| TSD hysteresis | ΔTSD | Design target | | 15 | | $^{\circ}\text{C}$ |

Note) V_{th} is a design target and not measured.

Mode Switching Truth Table

| CTRL0 | CTRL1 | Mode |
|-------|-------|--------------|
| L | L | Control |
| L | H | Noncontrol |
| H | L | Acceleration |
| H | H | Deceleration |

L = 0 to 1.0 V

H = 4.0 V or more

Hall Logic Truth Table

| | Source → Sink | Hall input | | | F/R Control |
|---|---------------|------------|----------|----------|-------------|
| | | U_{IN} | V_{IN} | W_{IN} | |
| 1 | W → V | H | H | L | Forward |
| | V → W | | | | Reverse |
| 2 | W → U | H | L | L | Forward |
| | U → W | | | | Reverse |
| 3 | V → W | L | L | H | Forward |
| | W → V | | | | Reverse |
| 4 | U → V | L | H | L | Forward |
| | V → U | | | | Reverse |
| 5 | V → U | H | L | H | Forward |
| | U → V | | | | Reverse |
| 6 | U → W | L | H | H | Forward |
| | W → U | | | | Reverse |

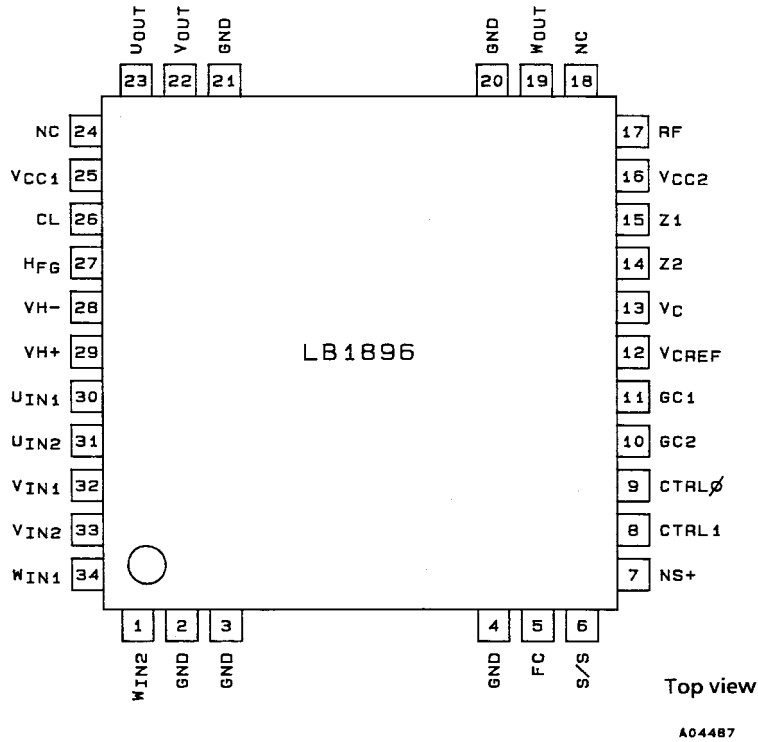
An input is considered to be HIGH when $U_{IN1} > U_{IN2}$, $V_{IN1} > V_{IN2}$, and $W_{IN1} > W_{IN2}$ by 0.2 V or more.

Forward when $V_C > V_{Cref}$

Reverse when $V_C < V_{Cref}$

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Pin Assignment



Pin Functions

| Pin No. | Pin Name | Pin Voltage | Equivalent Circuit Diagram | Pin Function |
|----------------|-------------------------|--------------|--|---|
| 3, 4 20, 21 | Frame GND | | | Frame GND. GND must be shared. |
| 2 | GND | | | GND |
| 23 22 19 | U OUT V OUT W OUT | | <p style="text-align: right;">A04490</p> | Output pins. Motor connection |
| 17 | Rf | | <p style="text-align: right;">A04491</p> | Output Tr GND. A resistor can be connected between this pin and GND to sense the output current as a voltage drop to provide for overcurrent protection. |
| 18, 24 | NC | | | Idle pins. |
| 16 | V CC2 | 4.3 to 6.5 V | | <ul style="list-style-type: none"> Power supply for blocks other than the output block. This supply should be kept stable to prevent ripple and noise from entering this pin. |
| 15 14 | Z1 Z2 | | <p style="text-align: right;">A04492</p> | <ul style="list-style-type: none"> First-stage amplifier gain setting resistors. Z1 and Z2 normally range from several tens of kΩ to several hundreds of kΩ. The gain is about 6 dB. |

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| Pin No. | Pin Name | Pin Voltage | Equivalent Circuit Diagram | Pin Function |
|----------|----------------------|--------------------------|--|--|
| 13 12 | V_C V_{Cref} | $V_{CC2}/2$ ± 1.0 | <p style="text-align: right;">A04493</p> | <ul style="list-style-type: none"> V_C is the speed control pin. Forward when $V_C > V_{Cref}$. Reverse when $V_C < V_{Cref}$. V_C is used to control the output voltage. V_{Cref} determines the motor control stop voltage. $V_{CC2}/2$ in normal use. |
| 11 10 | GC1 GC2 | 0 to V_{CC2} | <p style="text-align: right;">A04494</p> | <ul style="list-style-type: none"> Input/output gain switching pins. GC1 is for first-stage amplifier Z1/Z2 switching. When GC1 is LOW, Z1 is selected; when HIGH, Z2 is selected. GC2 is for next-stage amplifier switching. |
| 9 8 | CTRL ϕ CTRL1 | 0 to V_{CC2} | <p style="text-align: right;">A04495</p> | <ul style="list-style-type: none"> Operation mode switching pins. Refer to the Mode Switching Truth Table for selection of control, acceleration, or deceleration. |
| 7 | NS+ | 0 to $V_{CC2} - 1 V$ | <p style="text-align: right;">A04496</p> | <ul style="list-style-type: none"> Input pin at noncontrol mode. The input-output gain is 14 dB. (GC2: LOW) Motor stops when $V_{NS} = 0 V$. |
| 6 | S/S | 0 to V_{CC2} | <p style="text-align: right;">A04497</p> | <ul style="list-style-type: none"> When the S/S pin is HIGH, START; when LOW, STOP. The threshold is $V_{CC2}/2$. |

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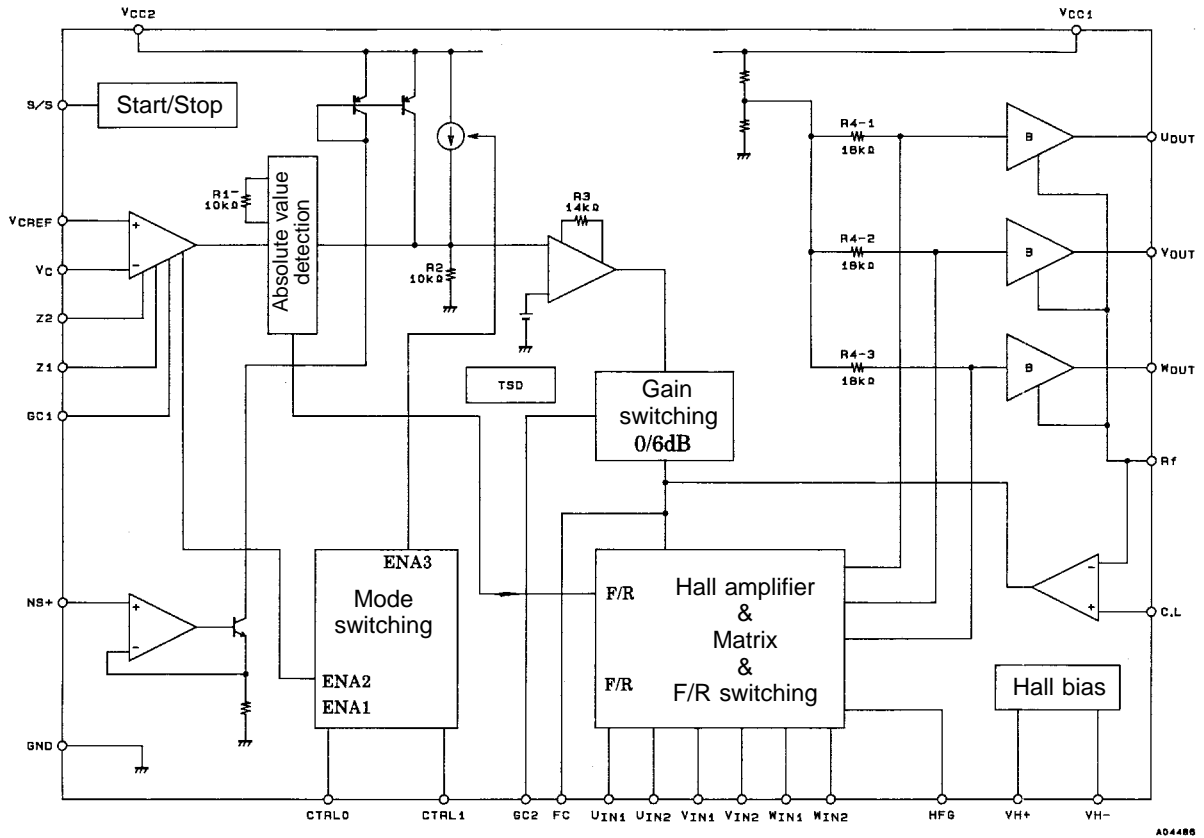
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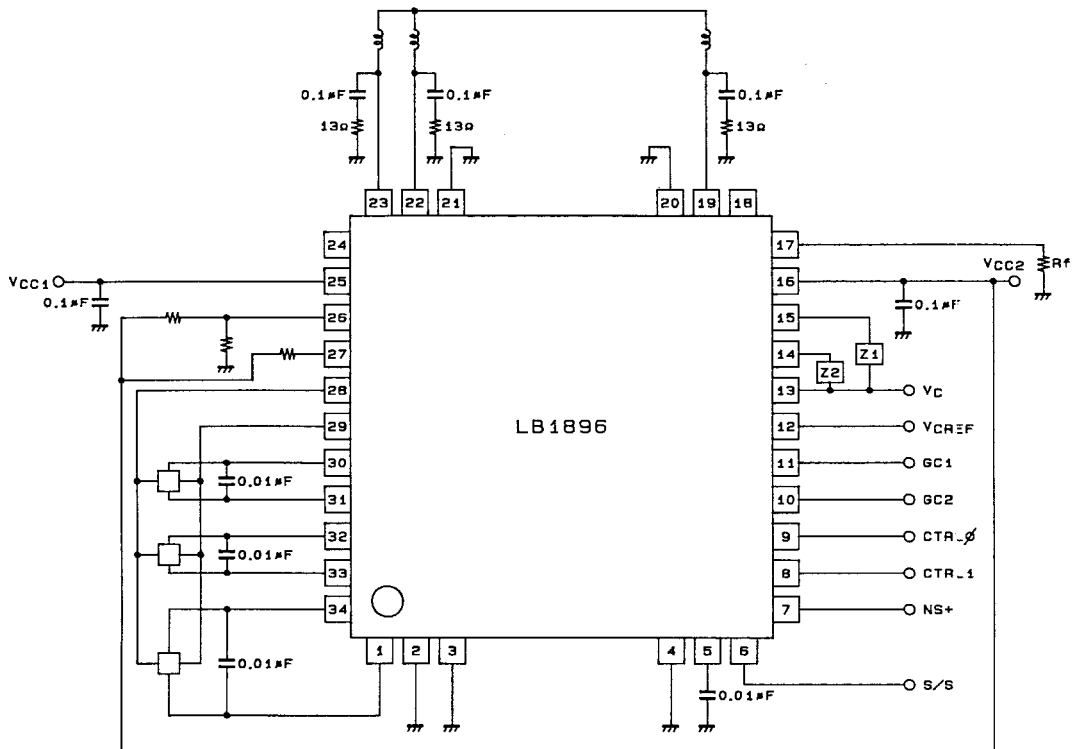
| Pin No. | Pin Name | Pin Voltage | Equivalent Circuit Diagram | Pin Function |
|---------------------------------|--|----------------|--|---|
| 5 | FC | | <p style="text-align: right;">A04498</p> | <ul style="list-style-type: none"> Connect a capacitor between this pin and GND to reduce the input/output gain frequency response and to stop the oscillator. |
| 1 34 33 32 31 30 | W_{IN2} W_{IN1} V_{IN2} V_{IN1} U_{IN2} U_{IN1} | 1.3 to 2.2 V | <p style="text-align: right;">A04489</p> | <p>W-phase Hall device input pins. Logic "H" represent $W_{IN1} > W_{IN2}$</p> <p>V-phase Hall device input pins. Logic "H" represent $V_{IN1} > V_{IN2}$</p> <p>U-phase Hall device input pins. Logic "H" represent $U_{IN1} > U_{IN2}$</p> |
| 29 28 | $VH+$ $VH-$ | 2.4 V 1.4 V | <p style="text-align: right;">A04500</p> | <ul style="list-style-type: none"> Hall device power supply pins. A voltage difference of 1.0 V is developed between $VH+$ and $VH-$. |
| 27 | H.FG | 0 to V_{CC2} | <p style="text-align: right;">A04501</p> | <ul style="list-style-type: none"> Hall FG pin. The Hall waveform is converted into a pulse signal and then used as the FG pulse signal. |
| 26 | CL | 0 to V_{CC2} | <p style="text-align: right;">A04502</p> | <ul style="list-style-type: none"> When the R_f pin voltage becomes equal to the C_L pin voltage, the current limiter operate. The C_L voltage is determined externally. |
| 25 | V_{CC1} | 5 to 18 V | | <ul style="list-style-type: none"> Power supply for output block. This supply should be kept stable to prevent ripple and noise from entering this pin. |

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Block Diagram



Sample Application Circuit



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