FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11145-1E

MEMORY

Un-buffered

4 M × 72 BIT SYNCHRONOUS DYNAMIC RAM SO-DIMM

MB8504S072CE-100/-100L

144-pin, 2 Clock, 1-bank, based on 4 M × 16 Bit SDRAMs with SPD

■ DESCRIPTION

The Fujitsu MB8504S072CE is a fully decoded, CMOS Synchronous Dynamic Random Access Memory (SDRAM) Module consisting of five MB81F641642C devices which organized as two banks of 4 M × 16 bits and a 2K-bit serial EEPROM on a 144-pin glass-epoxy substrate.

The MB8504S072CE features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence.

The MB8504S072CE is optimized for those applications requiring high speed, high performance and large memory storage, and high density memory organizations.
This module is ideally suited for workstations, PCs, laser printers, and other applications where a simple interface is needed.

■ PRODUCT LINE & FEATURES

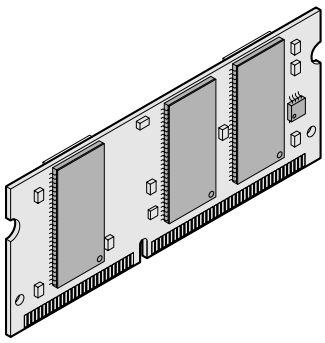
Parameter	MB8504S072CE	
	-100	-100L
Clock Frequency	100 MHz max.	
Burst Mode Cycle Time	10 ns min.	
Access Time from Clock	8.5 ns max. (CL = 3)	
Operating Current	450 mA max.	
Power Down Mode Current (I_{CC2P})	10 mA max.	5 mA max.
Self Refresh Current (I_{CC6})	5 mA max.	2.5 mA max.

- Unbuffered 144-pin SO-DIMM Socket Type
  (Lead pitch: 0.8 mm)
- Conformed to JEDEC Standard (2 CLK)
- Organization: 4,194,304 words × 72 bits
- Memory: MB81F641642C (4 M × 16, 4-bank) × 5 pcs.
- 3.3 V ±0.3 V Supply Voltage
- All input/output LVTTL compatible
- 4096 Refresh Cycle every 65.6 ms
- Auto and Self Refresh
- CKE Power Down Mode
- DQM Byte Masking (Read/Write)
- Serial Presence Detect (SPD) with Serial EEPROM:
  JEDEC Standard SPD Format
- Module size:
  1.1” (height) × 2.66” (length) × 0.15” (thickness)
- CL-t_{RCD}-t_{RP}: 3-3-3 clk min. @100 MHz,
  2-2-2 clk min. @66 MHz

MB8504S072CE-100/-100L

■ PACKAGE

144-pin plastic DIMM (socket type)



(MDS-144P-P10)

Package and Ordering Information

– 144-pin SO-DIMM, order as MB8504S072CE-100DG (DG = Std. power ver., Gold Pad)
-100LDG(LDG = Std. power ver., Gold Pad))

MB8504S072CE-100/-100L

■ PIN ASSIGNMENTS

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V_{SS}	49	DQ_{13}	97	DQ_{22}	2	V_{SS}	50	DQ_{45}	98	DQ_{54}
3	DQ_0	51	DQ_{14}	99	DQ_{23}	4	DQ_{32}	52	DQ_{46}	100	DQ_{55}
5	DQ_1	53	DQ_{15}	101	V_{CC}	6	DQ_{33}	54	DQ_{47}	102	V_{CC}
7	DQ_2	55	V_{SS}	103	A_6	8	DQ_{34}	56	V_{SS}	104	A_7
9	DQ_3	57	CB_0	105	A_8	10	DQ_{35}	58	CB_4	106	BA_0
11	V_{CC}	59	CB_1	107	V_{SS}	12	V_{CC}	60	CB_5	108	V_{SS}
13	DQ_4	61	CLK_0	109	A_9	14	DQ_{36}	62	CKE_0	110	BA_1
15	DQ_5	63	V_{CC}	111	A_{10}	16	DQ_{37}	64	V_{CC}	112	A_{11}
17	DQ_6	65	$\overline{RAS}$	113	V_{CC}	18	DQ_{38}	66	$\overline{CAS}$	114	V_{CC}
19	DQ_7	67	$\overline{WE}$	115	$DQMB_2$	20	DQ_{39}	68	N.C.	116	$DQMB_6$
21	V_{SS}	69	$\overline{CS_0}$	117	$DQMB_3$	22	V_{SS}	70	N.C.	118	$DQMB_7$
23	$DQMB_0$	71	N.C.	119	V_{SS}	24	$DQMB_4$	72	N.C.	120	V_{SS}
25	$DQMB_1$	73	N.C.	121	DQ_{24}	26	$DQMB_5$	74	CLK_1	122	DQ_{56}
27	V_{CC}	75	V_{SS}	123	DQ_{25}	28	V_{CC}	76	V_{SS}	124	DQ_{57}
29	A_0	77	CB_2	125	DQ_{26}	30	A_3	78	CB_6	126	DQ_{58}
31	A_1	79	CB_3	127	DQ_{27}	32	A_4	80	CB_7	128	DQ_{59}
33	A_2	81	V_{CC}	129	V_{CC}	34	A_5	82	V_{CC}	130	V_{CC}
35	V_{SS}	83	DQ_{16}	131	DQ_{28}	36	V_{SS}	84	DQ_{48}	132	DQ_{60}
37	DQ_8	85	DQ_{17}	133	DQ_{29}	38	DQ_{40}	86	DQ_{49}	134	DQ_{61}
39	DQ_9	87	DQ_{18}	135	DQ_{30}	40	DQ_{41}	88	DQ_{50}	136	DQ_{62}
41	DQ_{10}	89	DQ_{19}	137	DQ_{31}	42	DQ_{42}	90	DQ_{51}	138	DQ_{63}
43	DQ_{11}	91	V_{SS}	139	V_{SS}	44	DQ_{43}	92	V_{SS}	140	V_{SS}
45	V_{CC}	93	DQ_{20}	141	SDA	46	V_{CC}	94	DQ_{52}	142	SCL
47	DQ_{12}	95	DQ_{21}	143	V_{CC}	48	DQ_{44}	96	DQ_{53}	144	V_{CC}

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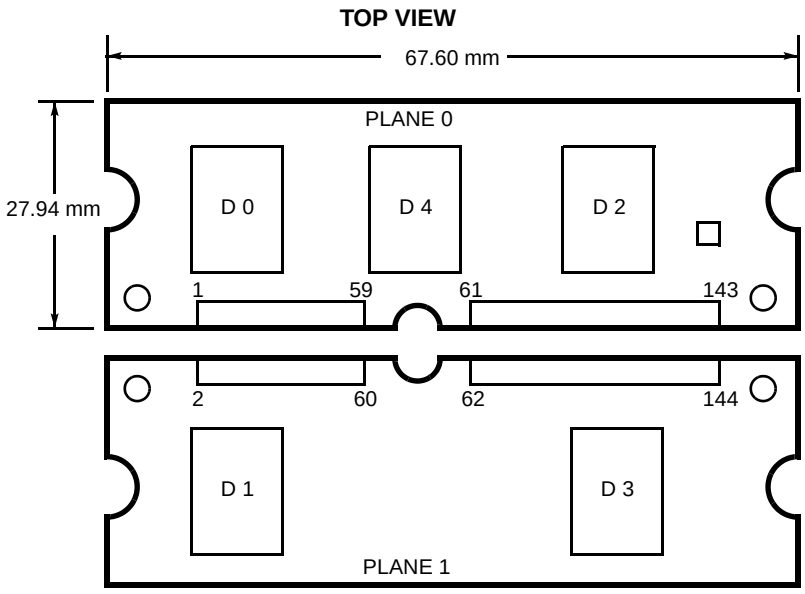

(MDS-144P-P10)

■ PIN DESCRIPTIONS

Symbol	I/O	Function	Symbol	I/O	Function
A_0 to A_{11}	I	Address Input	$\overline{CS}_0$	I	Chip Select
BA_0, BA_1	I	Bank Address	DQ_0 to DQ_{63}	I/O	Data Input/Data Output
$\overline{RAS}$	I	Row Address Strobe	CB_0 to CB_7	I/O	Data I/O for ECC
$\overline{CAS}$	I	Column Address Strobe	V_{CC}	—	Power Supply (+3.3 V)
$\overline{WE}$	I	Write Enable	V_{SS}	—	Ground (0 V)
$DQMB_0$ to $DQMB_7$	I	Data (DQ) Mask	N.C.	—	No Connection
CLK_0, CLK_1	I	Clock Input	SCL	I	Serial PD Clock
CKE_0	I	Clock Enable	SDA	I/O	Serial PD Address/Data I/O

■ SERIAL-PD INFORMATION

Byte	Function Described		Hex Value
			-100/100L
0	Defines Number of Bytes Written into Serial Memory at Module Manufacture	128 Byte	80h
1	Total Number of Bytes of SPD Memory Device	256 Byte	08h
2	Fundamental Memory Type	SDRAM	04h
3	Number of Row Addresses	12	0Ch
4	Number of Column Addresses	8	08h
5	Number of Module Banks	1 bank	01h
6	Data Width	72 bit	48h
7	Data Width (Continuation)	+0	00h
8	Interface Type	LVTTL	01h
9	SDRAM Cycle Time (Highest CAS Latency)	10 ns	A0h
10	SDRAM Access from Clock (Highest CAS Latency)	8.5 ns	85h
11	DIMM Configuration Type	ECC	02h
12	Refresh Rate/Type	Self, Normal	80h
13	Primary SDRAM Width	×16	10h
14	Error Checking SDRAM Width	×16	10h
15	Minimum Clock Delay for Back to Back Random Column Addresses	1 Cycle	01h
16	Burst Lengths Supported	1, 2, 4, 8, Page	8Fh
17	Number of Banks on Each SDRAM Device	4 bank	04h
18	CAS Latency	2, 3	06h
19	CS Latency	0	01h
20	Write Latency	0	01h
21	SDRAM Module Attributes	UN-buffer	00h
22	SDRAM Device Attributes	*1	0Eh
23	SDRAM Cycle Time (2nd. Highest CAS Latency)	15 ns	F0h
24	SDRAM Access from Clock (2nd. Highest CAS Latency)	9 ns	90h
25	SDRAM Cycle Time (3rd. Highest CAS Latency)	No Support	00h
26	SDRAM Access from Clock (3rd. Highest CAS Latency)	No Support	00h
27	Precharge to Activate Min. (t_{RP})	30 ns	1Eh
28	$\overline{\text{Row}}$ Activate to Row Activate Min. (t_{RRD})	20 ns	14h
29	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Min. (t_{RCD})	30 ns	1Eh
30	Activate to Precharge Minimum Time (t_{RAS})	60 ns	3Ch
31	Module Bank Density	32 MByte	08h
32 to 61	Unused Storage Locations	—	00h
62	SPD Data Revision Code	1	01h
63	Checksum for Byte 0 to 62	*2	70h
64 to 98	Manufacturer's Information: Unused Storage	—	00h
99 to 125	Vendor Specific Data: Unused Storage	—	00h
126	Intel Specification Frequency	66 MHz	66h
127	Intel Specification Details for 66 MHz Support	CL=2, 3	CFh
128+	Unused Storage Locations	—	—

Note: Any write operation must NOT be executed into the addresses of Byte 0 to Byte 127. Some or all data stored into Byte 0 to Byte 127 may be broken.

*1. SDRAM Device Attributes

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TBD	TBD	Upper V_{CC} tolerance 0 = 10%	Lower V_{CC} tolerance 0 = 10%	Supports Write 1/ Read Burst	Supports Precharge All	Supports Auto-Precharge	Supports Early $\overline{\text{RAS}}$ Precharge
0	0	0	0	1	1	1	0

*2. Checksum for Bytes 0 to 62

This byte is the checksum for bytes 0 through 62. This byte contains the value of the low 8-bits of the arithmetic sum of bytes 0 through 62.

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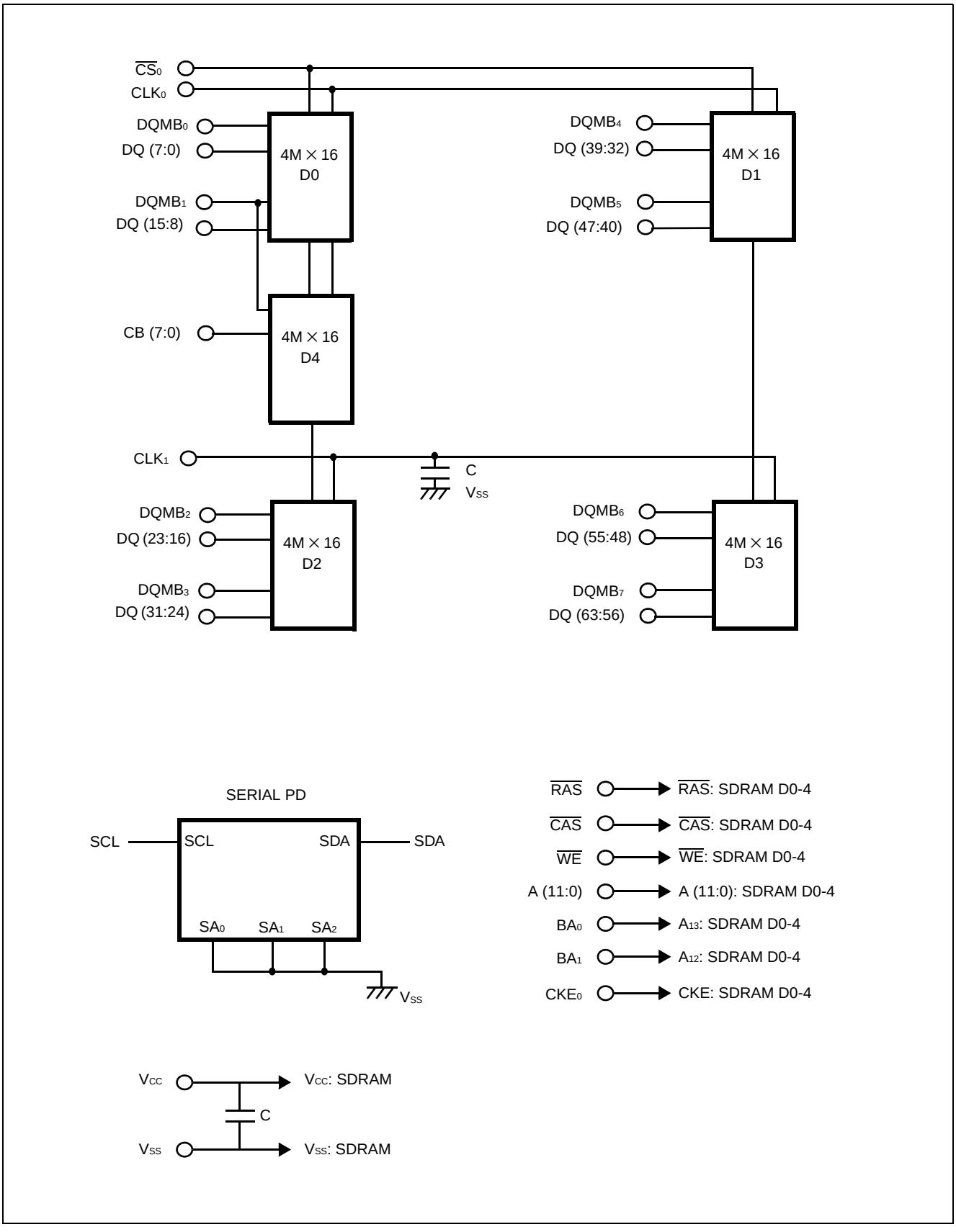
■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Supply Voltage*	V_{CC}	–0.5	+4.6	V
Input Voltage*	V_{IN}	–0.5	+4.6	V
Output Voltage*	V_{OUT}	–0.5	+4.6	V
Storage Temperature	T_{STG}	–55	+125	°C
Power Dissipation	P_D	—	5.0	W
Output Current (D.C.)	I_{OUT}	–50	+50	mA

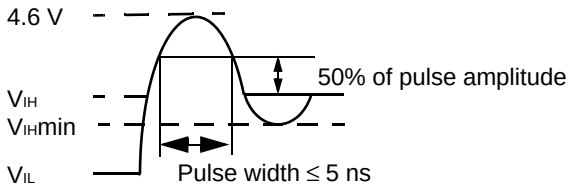
* : Voltages referenced to V_{SS} (= 0 V)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

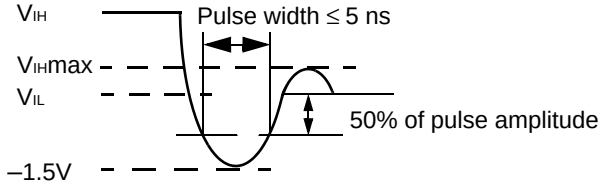
■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	*1	V_{CC}	3.0	3.3	3.6	V
		V_{SS}	0	0	0	V
Input High Voltage, All Inputs	*1, 2	V_{IH}	2.0	—	V_{CC} +0.5	V
Input Low Voltage, All Inputs	*1, 3	V_{IL}	–0.5	—	0.8	V
Ambient Temperature		T_A	0	—	+70	°C

*1. Voltages referenced to V_{SS} (= 0 V)



*2. Overshoot limit: V_{IH} (max)
= 4.6 V for pulse width <= 5 ns acceptable,
pulse width measured at 50% of pulse amplitude.



*3. Undershoot limit: V_{IL} (min)
= V_{SS} –1.5 V for pulse width <= 5 ns acceptable,
pulse width measured at 50% of pulse amplitude.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating conditionranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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■ CAPACITANCE

(V_{CC} = +3.3 V, f = 1 MHz, T_A = +25°C)

Parameter		Symbol	Value		Unit
			Min.	Max.	
Input Capacitance	A_0 to A_{11}, BA_0, BA_1	C_{IN1}	—	45	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	38	pF
	$\overline{CS}_0$	C_{IN3}	—	35	pF
	CKE_0	C_{IN4}	—	37	pF
	CLK_0, CLK_1	C_{IN5}	—	38	pF
	$DQMB_0$ to $DQMB_7$	C_{IN6}	—	16	pF
	SCL	C_{SCL}	—	7	pF
Input/Output Capacitance	SDA	C_{SDA}	—	7	pF
	DQ_0 to DQ_{63}	C_{DQ}	—	12	pF
	CB_0 to CB_7	C_{CB}	—	12	pF

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2

Parameter	Notes	Symbol	Condition	Value			Unit
				Min.	Max.		
					Std. ver.	Low ver.	
Operating Current (Average Power Supply Current)	*3	I_{CC1S}	Burst: Length = 1 t_{RC} = min for BL = 1 t_{CK} = min One Bank Active, Outputs Open Addresses changed up to 1-time during t_{CK} (min.) 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	450		mA
Precharge Standby Current (Power Supply Current)	*3	I_{CC2P}	CKE = V_{IL}, All Banks Idle t_{CK} = min, Power Down Mode 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	10	5	mA
		I_{CC2PS}	CKE = V_{IL}, All Banks Idle CLK = H or L, Power Down Mode 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	5	2.5	mA
		I_{CC2N}	CKE = V_{IH}, All Banks Idle, t_{CK} = min NOP commands only, Input signals (except to CMD) are changed 1-time during 3 clock cycles. 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	50		mA
		I_{CC2NS}	CKE = V_{IH}, All Banks Idle CLK = H or L, Input signal are stable. 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	10		mA
Active Standby Current (Power Supply Current)	*3	I_{CC3P}	CKE = V_{IL}, Any Bank Active t_{CK} = min. 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	10	5	mA
		I_{CC3PS}	CKE = V_{IL}, Any Bank Active CLK = H or L 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	5	2.5	mA
		I_{CC3N}	CKE = V_{IH}, Any Bank Active t_{CK} = min., NOP commands only, Input signals (except to CMD) are changed 1-time during 3 clock cycles. 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	75		mA
		I_{CC3NS}	CKE = V_{IH}, Any Bank Active CLK = H or L 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	10		mA

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(Continued)

Parameter	Notes	Symbol	Condition	Value			Unit
				Min.	Max.		
					Std. ver.	Low ver.	
Burst Mode Current (Average Power Supply Current)	*3	I_{CC4}	t_{CK} = min, Burst Length = 4 Outputs Open, All Banks Active Gapless Data 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	425		mA
Auto-refresh Current (Average Power Supply Current)	*3	I_{CC5}	Auto Refresh t_{CK} = min t_{RC} = min 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	850		mA
Self-refresh Current (Average Power Supply Current)	*3	I_{CC6}	Self-Refresh t_{CK} = min. CKE ≤ 0.2 V 0 V ≤ V_{IN} ≤ V_{IL} (max.) V_{IH} (min.) ≤ V_{IN} ≤ V_{CC}	—	5	2.5	mA
Input Leakage Current (All Inputs)		$I_{I(L)}$	0 V ≤ V_{IN} ≤ V_{CC} All other pins not under test = 0 V	–20	20		µA
Output Leakage Current		$I_{O(L)}$	0 V ≤ V_{IN} ≤ V_{CC} Output is disabled (Hi-Z)	–5	5		µA
LVTTL Output High Voltage	*4	V_{OH}	I_{OH} = –2.0 mA	2.4	—		V
LVTTL Output Low Voltage	*4	V_{OL}	I_{OL} = +2.0 mA	—	0.4		V

Notes: *1. An initial pause (DESL on NOP) of 200 µs is required after power-on followed by a minimum of eight Auto-refresh cycles.

*2. DC characteristics is the Serial PD standby state (V_{IN} = V_{SS} or V_{CC}).

*3. I_{CC} depends on the output termination, load conditions, clock cycle rate and signal clock rate. The specified values are obtained with the output open and no termination resistor.

*4. Voltages referenced to V_{SS} = V_{SSQ} (= 0 V)

■ AC CHARACTERISTICS

(1) BASE CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes		Symbol	MB8504S072CE -100/100L		Unit
					Min.	Max.	
1	Clock Period		CL = 3	t_{CK3}	10	—	ns
			CL = 2	t_{CK2}	15	—	ns
2	Clock High Time			t_{CH}	3.5	—	ns
3	Clock Low Time			t_{CL}	3.5	—	ns
4	Input Setup Time			t_{SI}	3	—	ns
5	Input Hold Time			t_{HI}	1	—	ns
6	Output Valid from Clock (t_{CLK} = min)	*4, *5	CL = 3	t_{AC3}	—	8.5	ns
			CL = 2	t_{AC2}	—	9	
7	Output in Low-Z	*6		t_{LZ}	0	—	ns
8	Output in High-Z	*6	CL = 3	t_{HZ3}	3	8.5	ns
			CL = 2	t_{HZ2}	3	9	ns
9	Output Hold Time	*6		t_{OH}	3	—	ns
10	Time between Refresh			t_{REF}	—	65.6	ms
11	Transition Time			t_T	0.5	2	ns
12	CKE Setup Time for Power Down Exit Time			t_{CKSP}	3	—	ns

(2) BASE VALUES FOR CLOCK COUNT/LATENCY

No.	Parameter	Notes		Symbol	MB8504S072CE -100/100L		Unit
					Min.	Max.	
1	$\overline{RAS}$ Cycle Time	*7		t_{RC}	90	—	ns
2	$\overline{RAS}$ Precharge Time			t_{RP}	30	—	ns
3	$\overline{RAS}$ Active Time			t_{RAS}	60	110000	ns
4	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*8		t_{RCD}	30	—	ns
5	Write Recovery Time			t_{WR}	10	—	ns
6	$\overline{RAS}$ to $\overline{CAS}$ Bank Active Delay Time			t_{RRD}	20	—	ns
7	Data-in to Precharge Lead Time			t_{DPL}	10	—	ns
8	Data-in to Active/Refresh Command Period		CL = 3	t_{DAL3}	2 cyc + t_{RP}	—	ns
			CL = 2	t_{DAL2}	1 cyc + t_{RP}	—	ns
9	Mode Register Set Cycle Time			t_{RSC}	20	—	ns

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(3) CLOCK COUNT FORMULA (*9)

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \text{ (Round off a whole number)}$$

(4) LATENCY (The latency values on these parameters are fixed regardless of clock period.)

No.	Parameter		Symbol	MB8504S072CE -100/100L	Unit
1	CKE to Clock Disable		I_{CKE}	1	Cycle
2	DQM to Output in High-Z		I_{DQZ}	2	Cycle
3	DQM to Input Data Delay		I_{DQD}	0	Cycle
4	Last Output to Write Command Delay		I_{OWD}	2	Cycle
5	Write Command to Input Data Delay		I_{DWD}	0	Cycle
6	Precharge to Output in High-Z Delay	CL = 3	I_{ROH3}	3	Cycle
		CL = 2	I_{ROH2}	2	Cycle
7	Burst Stop Command to Output in High-Z Delay	CL = 3	I_{BSH3}	3	Cycle
		CL = 2	I_{BSH2}	2	Cycle
8	$\overline{CAS}$ to $\overline{CAS}$ Delay (min)		I_{CCD}	1	Cycle
9	$\overline{CAS}$ Bank Delay (min)		I_{CBD}	1	Cycle

Notes: *1. An initial pause (DESL on NOP) of 200 µs is required after power-up followed by a minimum of eight Auto-refresh cycles.

*2. 1.4 V or V_{REF} is the reference level for measuring timing of signals.
Transition times are measured between V_{IH} (min) and V_{IL} (max).

*3. AC characteristics assume t_T = 1 ns and 50 pF of capacitive load.

*4. Maximum value of CL = 2 depends on t_{CK}.

*5. t_{AC} also specifies the access time at burst mode except for first access.

*6. Specified where output buffer is no longer driven. t_{OH}, t_{LZ}, and t_{HZ} define the times at which the output level achieves ±200 mV.

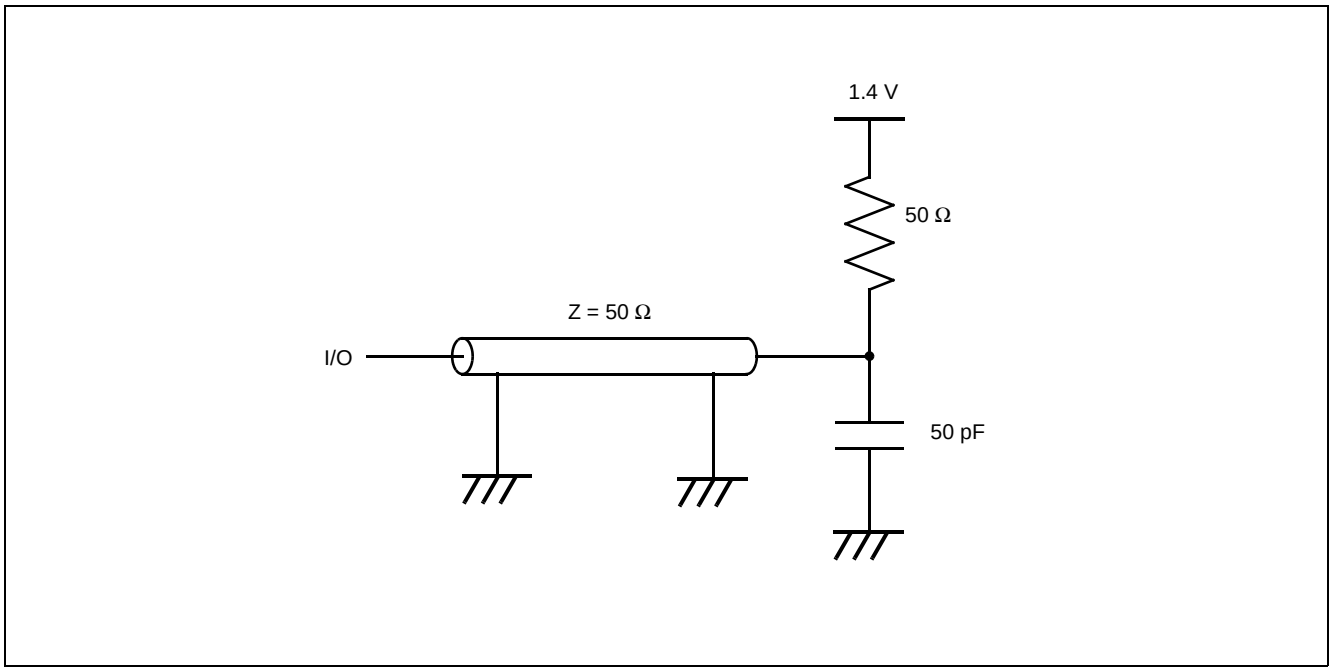
*7. Actual clock count of t_{RC} (I_{RC}) will be sum of clock count of t_{RAS} (I_{RAS}) and t_{RP} (I_{RP}).

*8. Operation within the t_{RCD} (min) ensures that access time is determined by t_{RCD} (min) + t_{AC} (max); if t_{RCD} is greater than the specified t_{RCD} (min), access time is determined by t_{CAC} and t_{AC}.

*9. All base values are measured from the clock edge at the command input to the clock edge for the next command input.
All clock counts are calculated by a simple formula:
clock count equals base value divided by clock period (round off to a whole number).

*Source: See MB81F641642C Data Sheet for details on the electrical.

■ AC OPERATING TEST CONDITION (Example of AC Test Load Circuit)



MB8504S072CE-100/-100L

■ SERIAL PRESENCE DETECT(SPD) FUNCTION

1. PIN DESCRIPTIONS

SCL (Serial Clock)

SCL input is used to clock all data input/output of SPD

SDA (Serial Data)

SDA is a common pin used for all data input/output of SPD. The SDA pull-up resistor is required due to the open-drain output.

SA_0, SA_1, SA_2 (Address)

Address inputs are used to set the least significant three bits of the eight bits slave address. The address inputs must be fixed to select a particular module and the fixed address of each module must be different each other. For this module, any address inputs are not required because all addresses (SA_0, SA_1, SA_2) are driven to V_{SS} on the module.

2. SPD OPERATIONS

CLOCK and DATA CONVENTION

Data states on the SDA can change only during SCL = Low. SDA state changes during SCL = High are indicated start and stop conditions. Refer to Fig. 1 below.

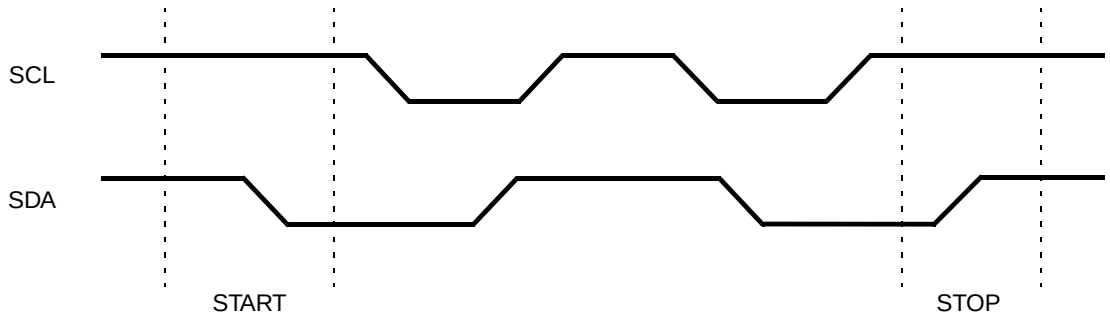
START CONDITION

All commands are preceded by a start condition, which is a transition of SDA state from High to Low when SCL = High. SPD will not respond to any command until this condition has been met.

STOP CONDITION

All read or write operation must be terminated by a stop condition, which is a transition of SDA state from Low to High when SCL = High. The stop condition is also used to make the SPD into the state of standby power mode after a read sequence.

Fig. 1 – START AND STOP CONDITIONS



START = High to Low transition of SDA state when SCL is High
STOP = Low to High transition of SDA state when SCL is High

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will put the SDA line to Low in order to acknowledge that it received the eight bits of data.

The SPD will respond with an acknowledge when it received the start condition followed by slave address issued by master.

In the read operation, the SPD will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is issued by master, the SPD will continue to transmit data. If an acknowledge is not detected, the SPD will terminated further data transmissions. The master must then issue a stop condition to return the SPD to the standby power mode.

In the write operation, upon receipt of eight bits of data the SPD will respond with an acknowledge, and await the next eight bits of data, again responding with an acknowledge until the stop condition is issued by master.

SLAVE ADDRESS ADDRESSING

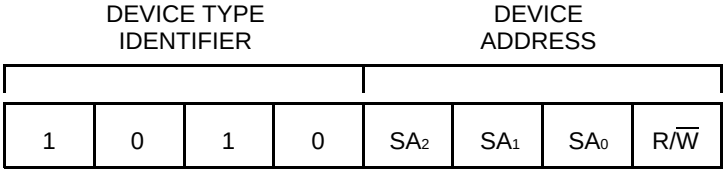
Following a start condition, the master must output the eight bits slave address. The most significant four bits of the slave address are device type identifier. For the SPD this is fixed as 1010[B]. Refer to the Fig. 2 below.

The next three significant bits are used to select a particular device. A system could have up to eight SPD devices —namely up to eight modules— on the bus. The eight addresses for eight SPD devices are defined by the state of the SA_0, SA_1 and SA_2 inputs. For this module, the three bits are fixed as 000[B] because all addresses are driven to V_{SS} on the module. Therefore, no address inputs are required.

The last bit of the slave address defines the operation to be performed. When R/$\overline{W}$ bit is “1”, a read operation is selected, when R/$\overline{W}$ bit is “0”, a write operation is selected.

Following the start condition, the SPD monitors the SDA line comparing the slave address being transmitted with its slave address (device type and state of SA_0, SA_1, and SA_2 inputs). Upon a correct compare the SPD outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the SPD will execute a read or write operation.

Fig. 2 – SLAVE ADDRESS

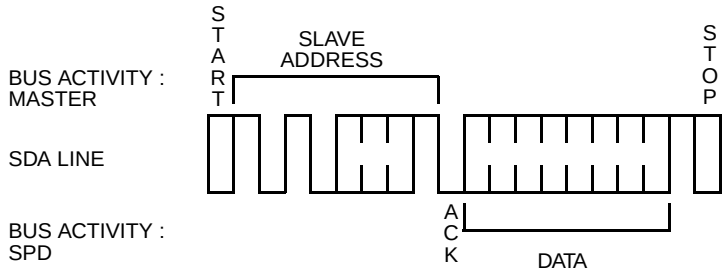


3. READ OPERATIONS

CURRENT ADDRESS READ

Internally the SPD contains an address counter that maintains the address of the last data accessed, incremented by one. Therefore, if the last access (either a read or write operation) was to address(n), the next read operation would access data from address(n+1). Upon receipt of the slave address with the R/$\overline{W}$ bit = "1", the SPD issues an acknowledge and transmits the eight bits of data during the next eight clock cycles. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig. 3 for the sequence of address, acknowledge and data transfer.

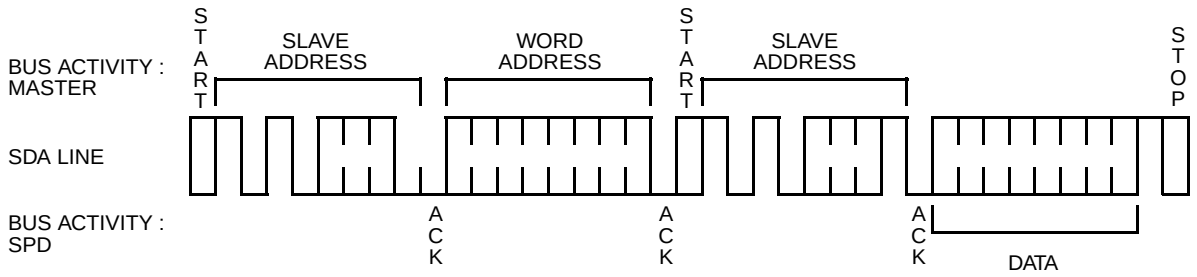
Fig. 3 – CURRENT ADDRESS READ



RANDOM READ

Random Read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit = "1", the master must first perform a "dummy" write operation on the SPD. The master issues the start condition, and the slave address followed by the word address. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit = "1". This will be followed by an acknowledge from the SPD and then by the eight bits of data. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig. 4 for the sequence of address, acknowledge and data transfer.

Fig. 4 – RANDOM READ

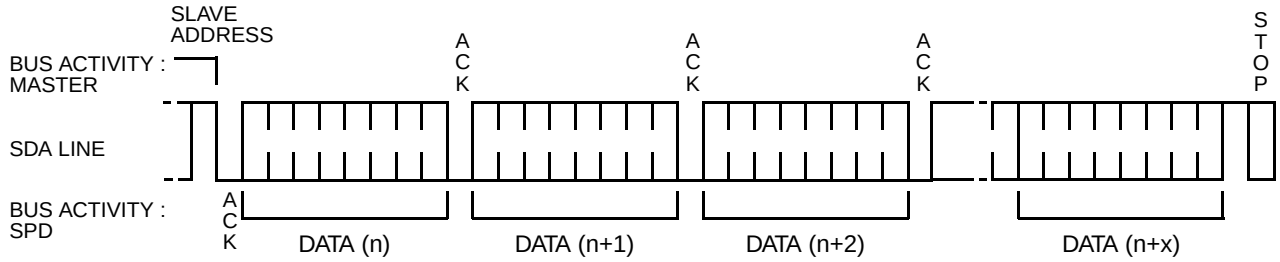


SEQUENTIAL READ

Sequential Read can be initiated as either a current address read or random read. The first data are transmitted as with the other read mode, however, the master now responds with an acknowledge, indicating it requires additional data. The SPD continues to output data for each acknowledge received. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig. 5 for the sequence of address, acknowledge and data transfer.

The data output is sequential, with the data from address(n) followed by the data from address(n+1). The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter “rolls over” to address0 and the SPD continues to output data for each acknowledge received.

Fig. 5 – SEQUENTIAL READ



4. DC CHARACTERISTICS

Parameter	Note	Symbol	Condition	Value		Unit
				Min.	Max.	
Input Leakage Current		S_{ILI}	$0\ V \le V_{IN} \le V_{CC}$	–10	10	µA
Output Leakage Current		S_{ILO}	$0\ V \le V_{OUT} \le V_{CC}$	–10	10	µA
Output Low Voltage	*1	S_{VOL}	I_{OL} = 3.0 mA	—	0.4	V

Note: *1. Referenced to V_{SS}.

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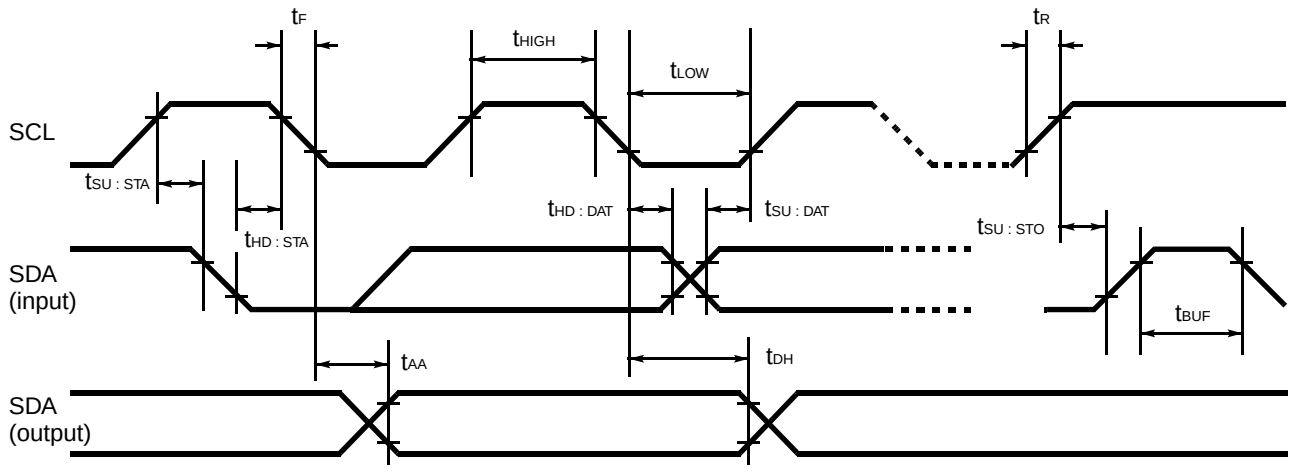
5. AC CHARACTERISTICS

No.	Parameter	Symbol	Value		Unit
			Min.	Max.	
1	SCL Clock Frequency	f_{SCL}	—	100	KHz
2	Noise Suppression Time Constant at SCL, SDA Inputs	T_I	—	100	ns
3	SCL Low to SDA Data Out Valid	t_{AA}	—	3.5	µs
4	Time the Bus Must Be Free Before a New Transmission Can Start	t_{BUF}	4.7	—	µs
5	Start Condition Hold Time	$t_{HD:STA}$	4.0	—	µs
6	Clock Low Period	t_{LOW}	4.7	—	µs
7	Clock High Period	t_{HIGH}	4.0	—	µs
8	Start Condition Setup Time	$t_{SU:STA}$	4.7	—	µs
9	Data in Hold Time	$t_{HD:DAT}$	0	—	µs
10	Data in Setup Time	$t_{SU:DAT}$	250	—	ns
11	SDA and SCL Rise Time	t_R	—	1	µs
12	SDA and SCL Fall Time	t_F	—	300	ns
13	Stop Condition Setup Time	$t_{SU:STO}$	4.7	—	µs
14	Data Out Hold Time	t_{DH}	100	—	ns
15	Write Cycle Time	t_{WR}	—	15	ms

Fig. 6 – TIMING WAVEFORM



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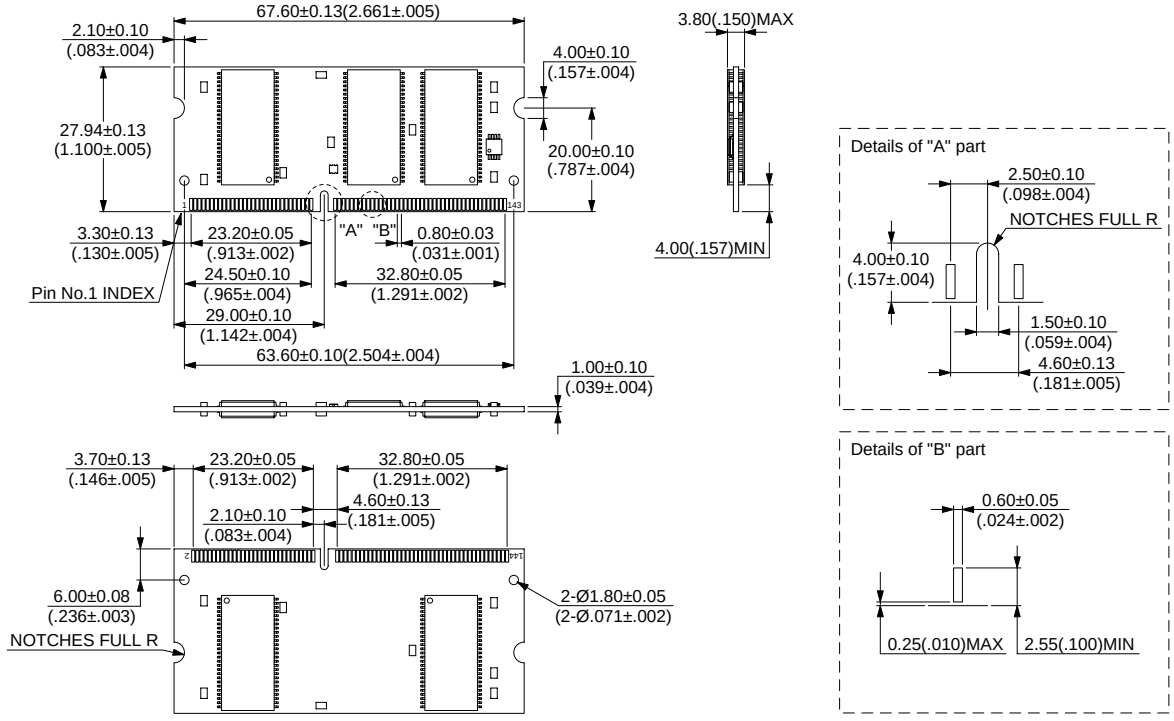
■ PACKAGE DIMENSION

144-pin plastic DIMM
(MDS-144P-P10)



Dimension in mm (inches).

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