

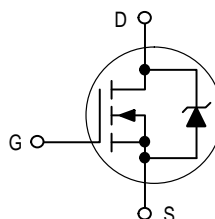
*Advance Information*

**TMOS E-FET™**

**Power Field Effect Transistors  
D2PAK for Surface Mount  
Logic Level TMOS (L<sup>2</sup>TMOS™)  
N-Channel Enhancement-Mode Silicon Gate**

These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers. This Logic Level Series part is specified to operate with level logic gate-to-source voltage of 5 volt and 4 volt.

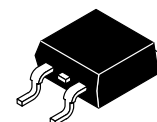
- Silicon Gate for Fast Switching Speeds
- Low  $R_{DS(on)}$  — 0.028  $\Omega$  max
- Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13-inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number



**MTB50N06EL**

Motorola Preferred Device

TMOS POWER FET  
LOGIC LEVEL  
50 AMPERES  
60 VOLTS  
 $R_{DS(on)} = 0.028 \text{ OHM}$



CASE 418B-02, Style 2  
D<sup>2</sup>PAK

**MAXIMUM RATINGS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	60	Vdc
Drain-Gate Voltage ( $R_{GS} = 1.0 \text{ M}\Omega$ )	$V_{DGR}$	60	Vdc
Gate-Source Voltage — Continuous	$V_{GS}$	$\pm 15$	Vdc
Drain Current — Continuous	$I_D$	50	Adc
— Continuous @ $100^\circ\text{C}$	$I_D$	28	
— Single Pulse ( $t_p \leq 10 \mu\text{s}$ )	$I_{DM}$	142	Apk
Total Power Dissipation	$P_D$	125	Watts
Derate above $25^\circ\text{C}$		1.0	W/ $^\circ\text{C}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ , when mounted with the minimum recommended pad size		2.5	Watts
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 25 \text{ Vdc}$ , $V_{GS} = 5.0 \text{ Vpk}$ , $I_L = 50 \text{ Apk}$ , $L = 0.32 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	400	mJ
Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.0	$^\circ\text{C/W}$
— Junction to Ambient	$R_{\theta JA}$	62.5	
— Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JA}$	50	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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**Preferred** devices are Motorola recommended choices for future use and best overall value.

# MTB50N06EL

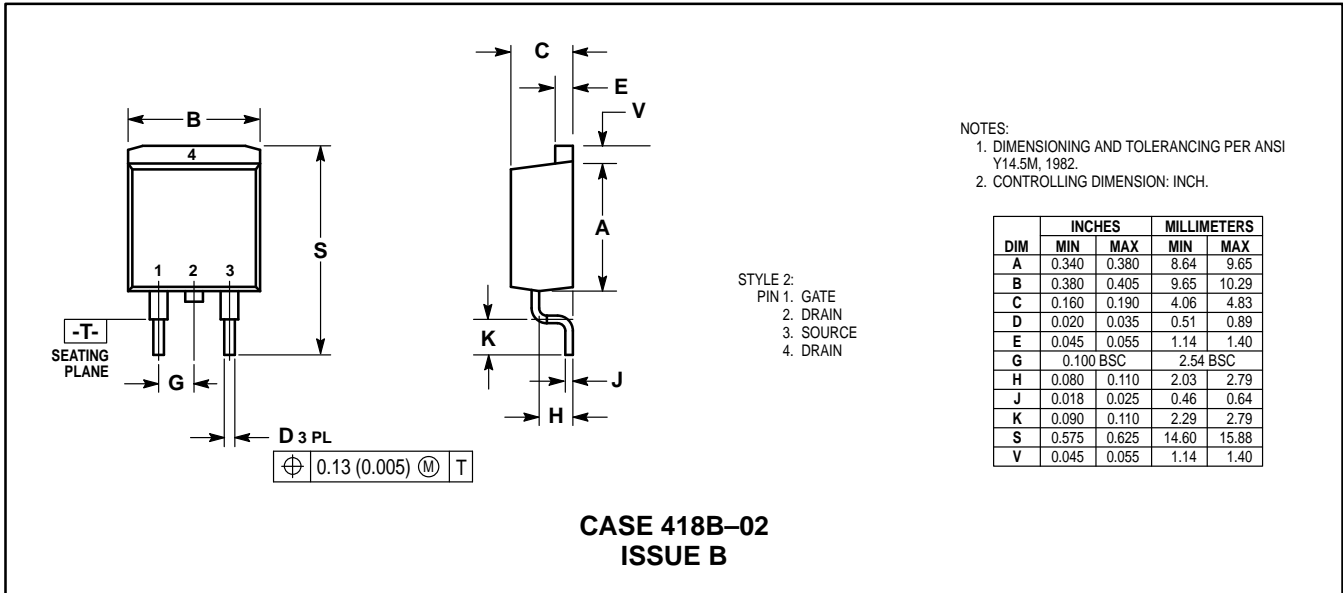
## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)


Characteristic	Symbol	Min	Typ	Max	Unit	
<b>OFF CHARACTERISTICS</b>						
Drain–Source Breakdown Voltage (V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 —	— 64	— —	Vdc mV/°C	
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	— —	— —	10 100	μAdc	
Gate–Body Leakage Current (V <sub>GS</sub> = ±15 Vdc, V <sub>DS</sub> = 0)	I <sub>GSS</sub>	—	—	100	nAdc	
<b>ON CHARACTERISTICS (1)</b>						
Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 —	— 4.78	2.0 —	Vdc mV/°C	
Static Drain–Source On–Resistance (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 25 Adc) (V <sub>GS</sub> = 4.0 Vdc, I <sub>D</sub> = 25 Adc)	R <sub>DS(on)</sub>	— —	— —	0.028 0.039	Ohm	
Drain–Source On–Voltage (V <sub>GS</sub> = 5.0 Vdc) (I <sub>D</sub> = 50 Adc) (I <sub>D</sub> = 25 Adc, T <sub>J</sub> = 125°C)	V <sub>DS(on)</sub>	— —	— —	1.68 1.40	Vdc	
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 25 Adc)	g <sub>FS</sub>	17	—	—	mhos	
<b>DYNAMIC CHARACTERISTICS</b>						
Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0, f = 1.0 MHz)	C <sub>iss</sub>	—	3100	pF	
Output Capacitance		C <sub>oss</sub>	—	1065		
Reverse Transfer Capacitance		C <sub>rss</sub>	—	260		
<b>SWITCHING CHARACTERISTICS (2)</b>						
Turn–On Delay Time	(V <sub>DD</sub> = 25 Vdc, I <sub>D</sub> = 50 Adc, V <sub>GS</sub> = 5.0 Vdc, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	—	21	ns	
Rise Time		t <sub>r</sub>	—	365		
Turn–Off Delay Time		t <sub>d(off)</sub>	—	55		
Fall Time		t <sub>f</sub>	—	150		
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 50 Adc, V <sub>GS</sub> = 5.0 Vdc)	Q <sub>T</sub>	—	52	nC	
		Q <sub>1</sub>	—	13		
		Q <sub>2</sub>	—	34		
		Q <sub>3</sub>	—	27		
<b>SOURCE–DRAIN DIODE CHARACTERISTICS</b>						
Forward On–Voltage	(I <sub>S</sub> = 50 Adc, V <sub>GS</sub> = 0) (I <sub>S</sub> = 50 Adc, V <sub>GS</sub> = 0, T <sub>J</sub> = °C)	V <sub>SD</sub>	— —	1.52 1.1	2.5 —	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 50 Adc, V <sub>GS</sub> = 0, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	—	200	—	ns
<b>INTERNAL PACKAGE INDUCTANCE</b>						
Internal Drain Inductance (Measured from the tab to center of die)	L <sub>d</sub>	—	3.5	—	nH	
Internal Source Inductance (Measured from the source lead 0.1" from package to source bond pad)	L <sub>s</sub>	—	7.5	—	nH	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS



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