

Matched N-Channel JFET Pairs

Product Summary

Part Number	V _{GS(off)} (V)	V _{(BR)GSS} Min (V)	g _{fs} Min (mS)	I _G Typ (pA)	V _{GS1} - V _{GS2} Max (mV)
2N5564	-0.5 to -3	-40	7.5	-3	5
2N5565	-0.5 to -3	-40	7.5	-3	10
2N5566	-0.5 to -3	-40	7.5	-3	20

Features

- Two-Chip Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 3 pA
- Low Noise: 12 nV/√Hz @ 10 Hz
- Good CMRR: 76 dB
- Minimum Parasitics

Benefits

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signals
- Maximum High Frequency Performance

Applications

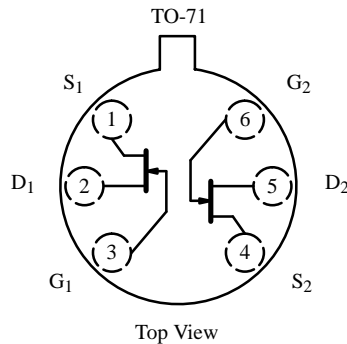
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters
- Matched Switches

Description

The 2N5564/5565/5566 are matched pairs of JFETs mounted in a TO-71 package. This two-chip design reduces parasitics for good performance at high frequency while ensuring extremely tight matching. This series features high breakdown voltage (V_{(BR)DSS} typically > 55 V), high gain (typically > 9 mS), and <5-mV offset between the two die.

The hermetically-sealed TO-71 package is available with full military processing (see Military Information).

For similar products see the low-noise U/SST401 series, and the low-leakage 2N5196/5197/5198/5199 data sheets.



Absolute Maximum Ratings

Gate-Drain, Gate-Source Voltage	-40 V	Operating Junction Temperature	-55 to 150°C
Gate-Gate Voltage	± 80 V	Power Dissipation : Per Side ^a	325 mW
Gate Current	50 mA	Total ^b	650 mW
Lead Temperature (1/16" from case for 10 sec.)	300 °C	Notes	
Storage Temperature	-65 to 200°C	a. Derate 2.6 mW/°C above 25°C	
		b. Derate 5.2 mW/°C above 25°C	

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70254.

2N5564/5565/5566

Specifications^a

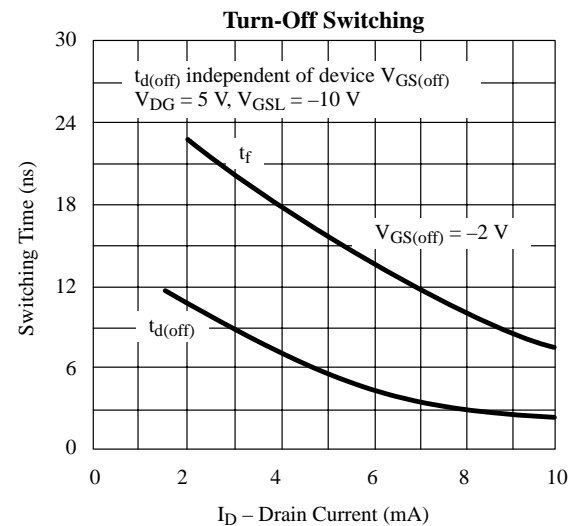
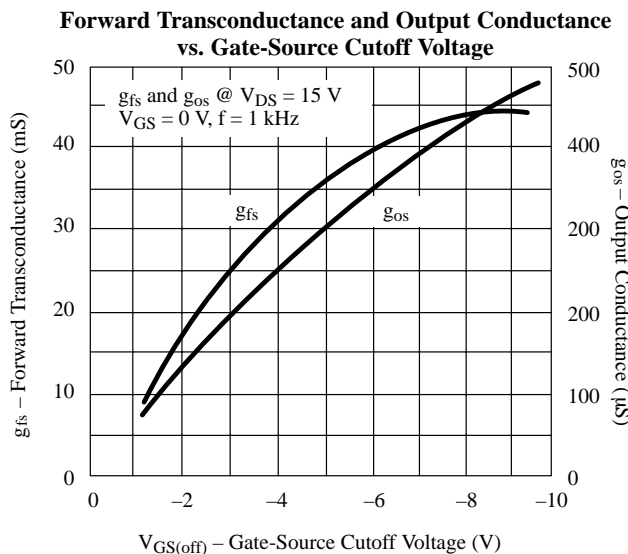
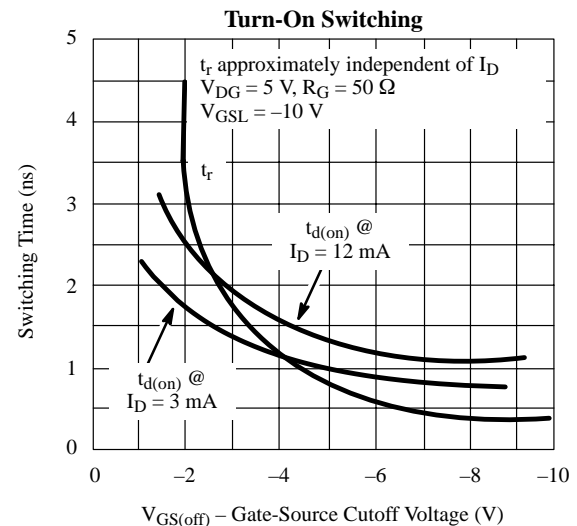
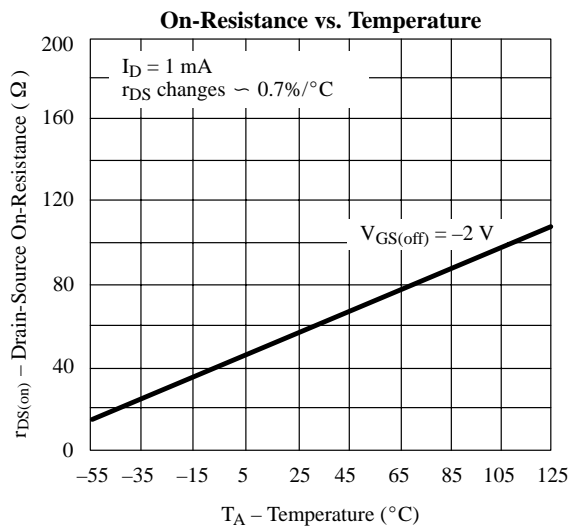
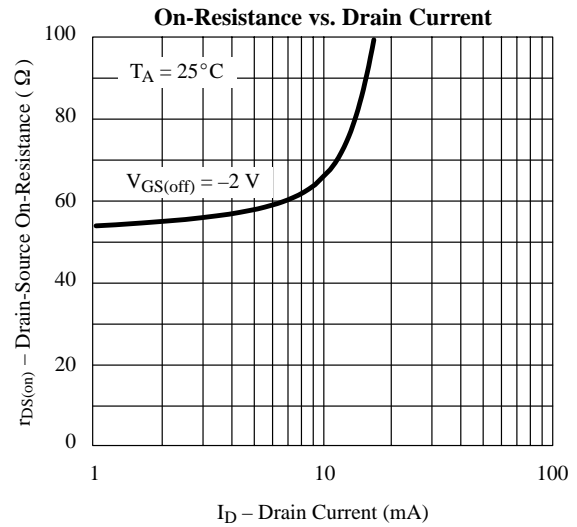
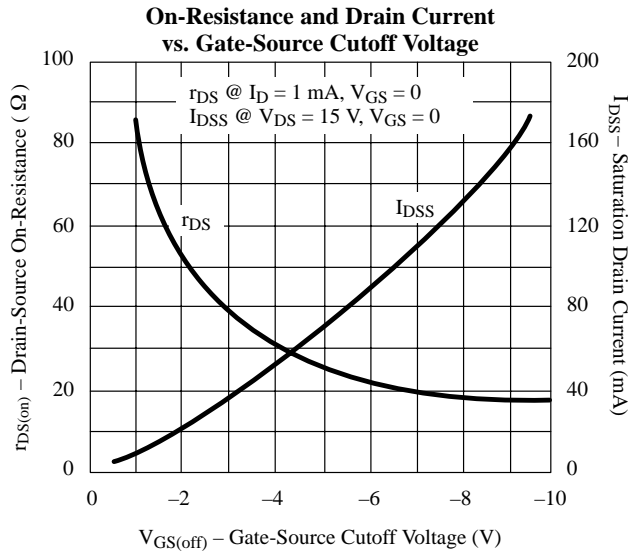
Parameter	Symbol	Test Conditions	Typ ^b	Limits						Unit
				2N5564		2N5565		2N5566		
				Min	Max	Min	Max	Min	Max	
Static										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-55	-40		-40		-40		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 15 V, I_D = 1 nA$	-2	-0.5	-3	-0.5	-3	-0.5	-3	
Saturation Drain Current ^c	I_{DSS}	$V_{DS} = 15 V, V_{GS} = 0 V$	20	5	30	5	30	5	30	mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -20 V, V_{DS} = 0 V$	-5		-100		-100		-100	pA
		$T_A = 150^\circ C$	-10		-200		-200		-200	nA
Gate Operating Current ^d	I_G	$V_{DG} = 15 V, I_D = 2 mA$	-3							pA
		$T_A = 125^\circ C$	-1							nA
Drain-Source On-Resistance	$r_{DS(on)}$	$V_{GS} = 0 V, I_D = 1 mA$	50		100		100		100	Ω
Gate-Source Voltage ^d	V_{GS}	$V_{DG} = 15 V, I_D = 2 mA$	-1.2							V
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 2 mA, V_{DS} = 0 V$	0.7		1		1		1	V
Dynamic										
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 15 V, I_D = 2 mA$ $f = 1 kHz$	9	7.5	12.5	7.5	12.5	7.5	12.5	mS
Common-Source Output Conductance	g_{os}		35		45		45		45	μS
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 15 V, I_D = 2 mA$ $f = 100 MHz$	8.5	7		7		7		mS
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 15 V, I_D = 2 mA$ $f = 1 MHz$	10		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		2.5		3		3		3	
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DS} = 15 V, I_D = 2 mA$ $f = 10 Hz$	12		50		50		50	nV/\sqrt{Hz}
Noise Figure	NF	$R_G = 10 M\Omega$			1		1		1	dB
Matching										
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 15 V, I_D = 2 mA$			5		10		20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 15 V, I_D = 2 mA$ $T_A = -55 \text{ to } 125^\circ C$			10		25		50	$\mu V/^\circ C$
Saturation Drain Current Ratio ^d	$\frac{I_{DSS1}}{I_{DSS2}}$	$V_{DS} = 15 V, V_{GS} = 0 V$	0.98	0.95	1	0.95	1	0.95	1	
Transconductance Ratio	$\frac{g_{fs1}}{g_{fs2}}$	$V_{DS} = 15 V, I_D = 2 mA$ $f = 1 kHz$	0.98	0.95	1	0.90	1	0.90	1	
Common Mode Rejection Ratio ^d	CMRR	$V_{DG} = 10 \text{ to } 20 V$ $I_D = 2 mA$	76							dB

Notes

- $T_A = 25^\circ C$ unless otherwise noted.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Pulse test: $PW \leq 300 \mu s$ duty cycle $\leq 3\%$.
- This parameter not registered with JEDEC.

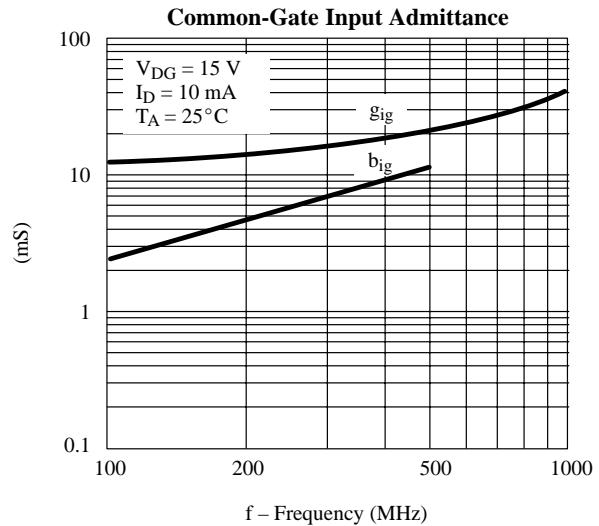
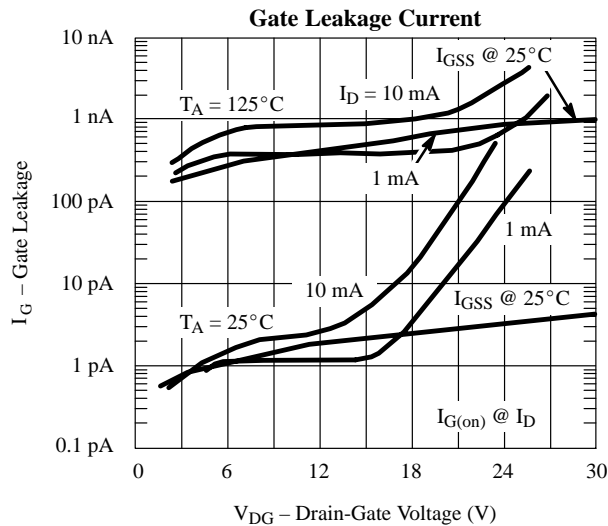
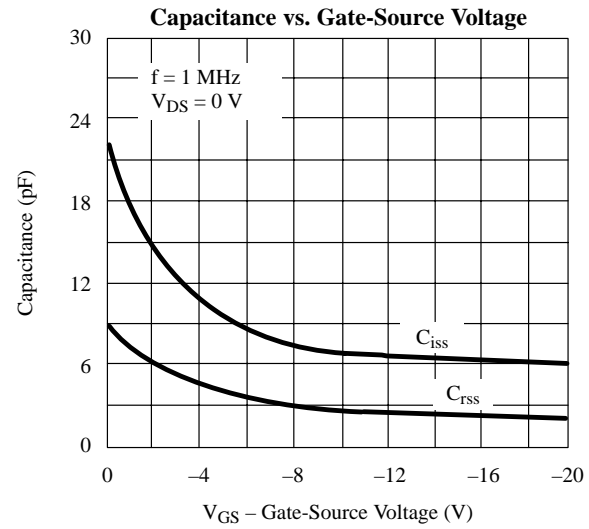
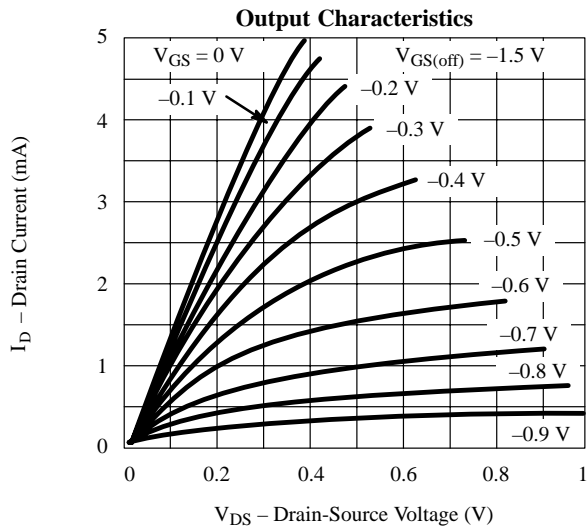
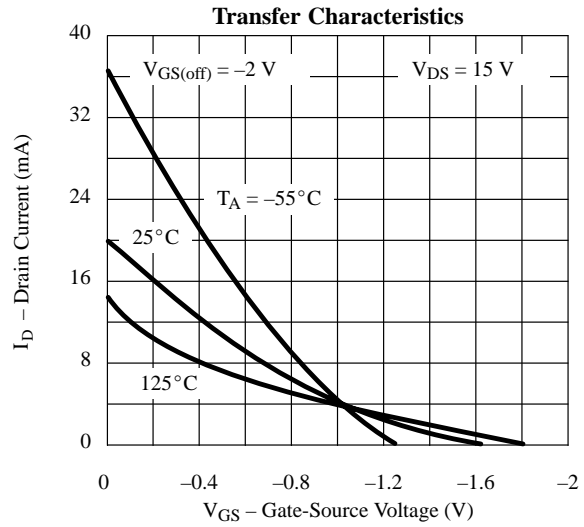
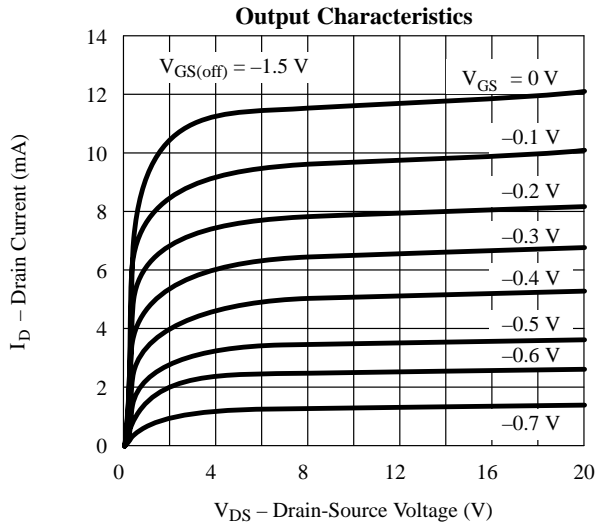
NCBD

Typical Characteristics



2N5564/5565/5566

Typical Characteristics (Cont'd)



Typical Characteristics (Cont'd)

