Micropower 1.2V/150mA CMOS LDO Regulator with Power Good

Features

- 1-5ms Power Good (PG) control signal
- Regulated 1.2V output
- 150mA output current
- Low quiescent operating current (90μA typical)
- "Zero" disable mode current
- Foldback current limiting protection
- Thermal shutdown protection
- Stable with low-ESR capacitors
- SOT23-5 package
- "MIC5258" pinout

Applications

- Pentium® 4 Motherboards
- Processor Power-up Sequencing
- Desktop, Notebook and Palmtop Computers
- PC Cards
- Peripheral Adapter Cards

Product Description

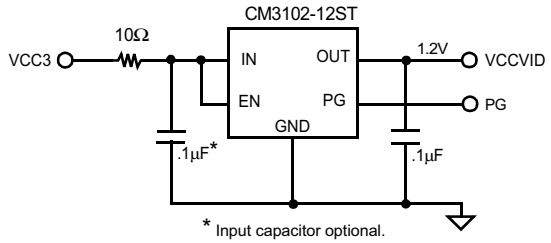
The CM3102 is a low quiescent current (90uA) regulator that delivers up to 150mA of load current at a fixed 1.2V output. In addition, the CM3102 features a Power Good output signal (PG) that goes open drain 1 to 5 ms after the output voltage has exceeded typically 93% of its nominal level.

A dedicated control input (EN, Active High) has been included for power-up sequencing flexibility. When this input is taken low, the regulator is disabled. In this state, the supply current will drop to near zero. An internal discharge MOSFET resistance (500Ω) will force the output to ground whenever the device has been shutdown.

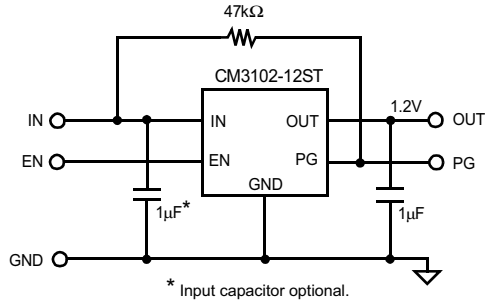
The CM3102 is fully protected, offering both overload current limiting and high temperature thermal shutdown.

Available in a tiny SOT23 package, the device is ideal for space critical applications.

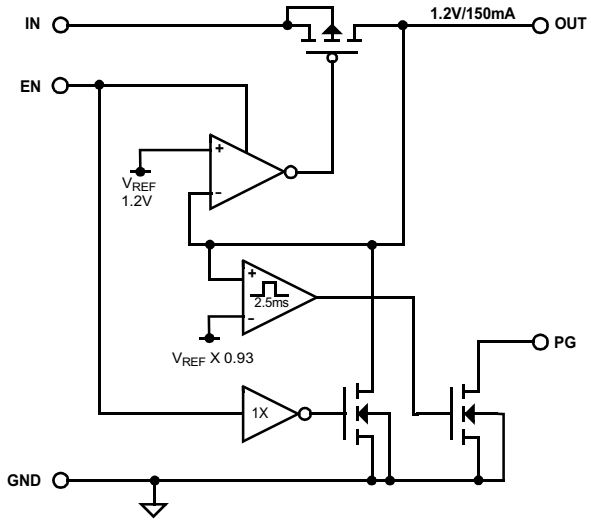
Pentium® 4 Motherboard Application Circuit



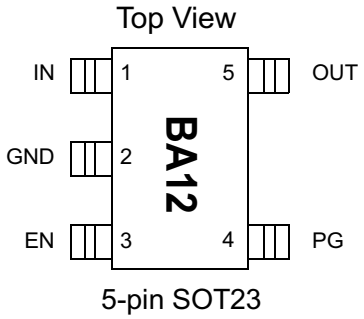
Typical Application Circuit



Simplified Electrical Schematic



PACKAGE / PINOUT DIAGRAM



5-pin SOT23

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	IN	Positive input voltage for the regulator. The internal loading on this input is typically 300µA whenever the regulator is enabled, and less than 1µA when the regulator is disabled. Although an input filter capacitor is not required, it is recommended that a 1µF ceramic capacitor be used for additional filtering and stability if this pin is greater than 2 inches from the main input filter.
2	GND	The negative reference for all voltages.
3	EN	Enable/shutdown input. When EN is asserted high ($V_{EN} \geq 1.6V$), the regulator is enabled. When EN is asserted low ($V_{EN} \leq 0.4V$), the regulator's series pass transistor is forced into a high impedance mode and an internal discharge resistance (500Ω) is applied to the output to quickly reduce the output voltage to 0 volts.
4	PG	Power Good output. This is an open drain output and functions as a supply voltage supervisor for the output voltage. It is asserted low when the output falls below 89% of its nominal value. This output becomes inactive when V_{OUT} remains above 97% of its nominal value for 1 to 5ms.
5	OUT	The regulated voltage output. An output capacitor of 1µF is recommended to minimize any transient load disturbances under normal operating conditions. Additional output capacitance can be used to further improve transient load response.

Ordering Information

PART NUMBERING INFORMATION

Regulator	Pins	Package	Ordering Part Number[1]	Part Marking
CM3102-12ST	5	SOT23-5	CM3102-12ST	BA12

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
ESD Protection (HBM)	±2000	V
Pin Voltages V_{IN} V_{OUT} V_{EN}	 [GND - 0.6] to +6.0 [GND - 0.6] to [V_{IN}+0.6] [GND - 0.6] to [V_{IN}+0.6]	 V V V
Storage Temperature Range	-40 to +150	°C
Operating Temperature Range Ambient Junction	 0 to +70 0 to +150	 °C °C
Power Dissipation (See note 1)	Internally Limited	W

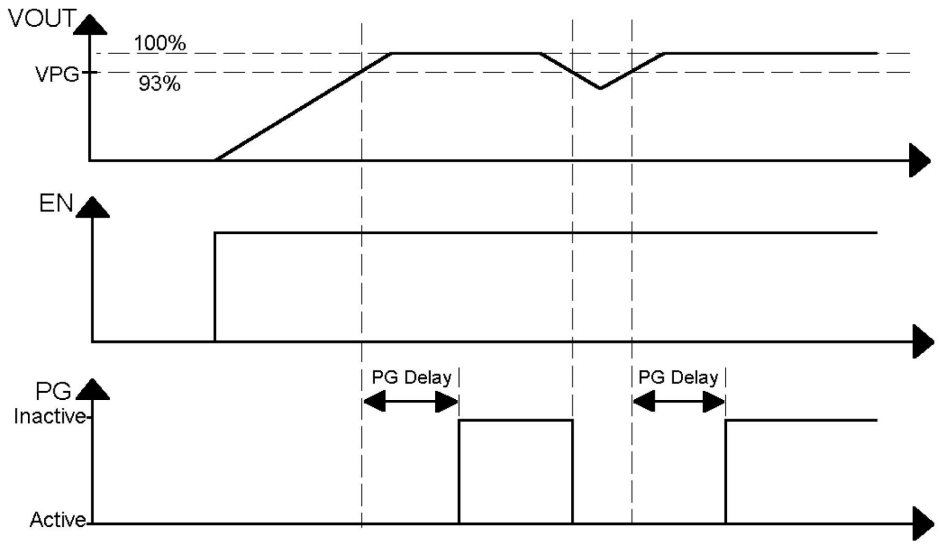
Note 1: The power rating is based on a printed circuit board heat spreading capability equivalent to 2 square inches of copper connected to the GND pins. Typical multi-layer boards using power plane construction will provide this heat spreading ability without the need for additional dedicated copper area. Please consult with factory for thermal evaluation assistance.

STANDARD OPERATING CONDITIONS		
PARAMETER	**VALUE**	**UNITS**
V_{IN}	2.7 to 5.5	V
Ambient Operating Temperature Range	0 to +70	°C
Load Current	0 to 150	mA
C_{OUT}	1 ±20%	µF

ELECTRICAL OPERATING CHARACTERISTICS[1]						
SYM-BOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OUT}	Regulator Output Voltage	0.1mA < I_{LOAD} < 150mA	1.1	1.2	1.3	V
$V_{R\ LOAD}$	Load Regulation	10mA ≤ I_{LOAD} ≤ 150mA		30		mV
$V_{R\ LINE}$	Line Regulation	I_{LOAD} = 5mA; 2.7V ≤ V_{IN} ≤ to 3.6V		20		mV
I_{LIM}	Overload Current Limit		160	350		mA
I_{SC}	Short Circuit Current Limit	V_{OUT} < 0.5V		140		mA
R_{DISCH}	Discharge Resistance	EN tied to GND		500		Ω
I_{GND}	Ground Current	Regulator Enabled (EN=V_{IN}); I_{LOAD}= 0mA Regulator Enabled (EN=V_{IN}); I_{LOAD}= 150mA Regulator Disabled (EN=GND); (Disable Mode)		90 100 0.01	200 250 10	µA µA µA
V_{EN}	EN Input Logic High Threshold	Regulator Enabled	1.6			V
V_{DIS}	EN Input Logic Low Threshold	Regulator Disabled			0.4	V
I_{EN}	Enable Input Current			0.01		µA
V_{PGL}	Power Good Low Threshold	% of V_{OUT} (PG ON)	89			%
V_{PGH}	Power Good High Threshold	% of V_{OUT} (PG OFF)			97	%
V_{OL}	Power Good Logic "0" Voltage	I_L=100µA; Fault Condition		0.02	0.1	V
I_{PG}	Power Good Leakage Current	Power Good Off; V_{PG}=5.5V		0.01		µA
PG_{DELAY}	Delay Time to Power Good		1		5	mS

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.

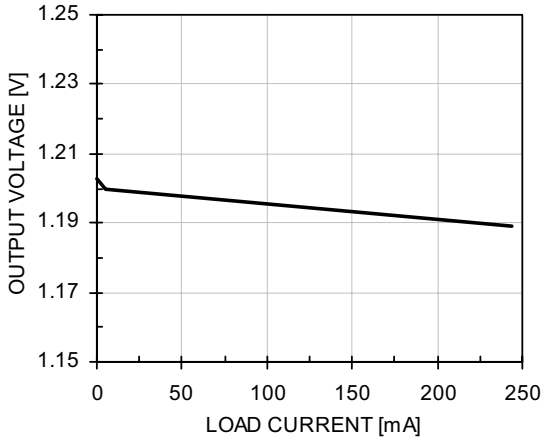
Timing Diagram



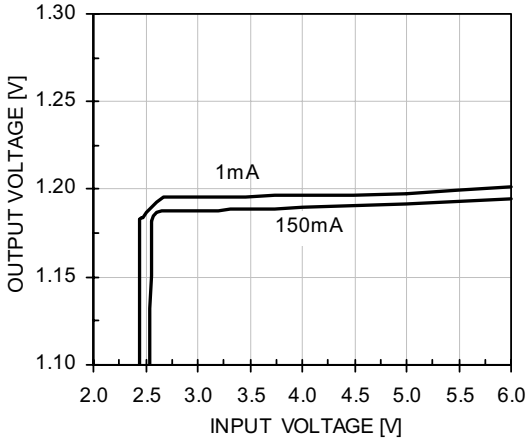
Performance Information

CM3102 Typical DC Characteristics (nominal conditions unless specified otherwise)

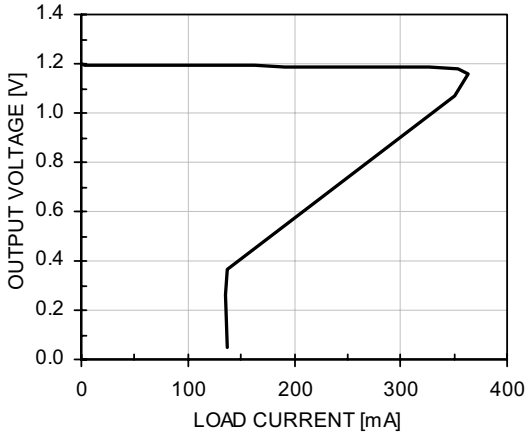
Load Regulation



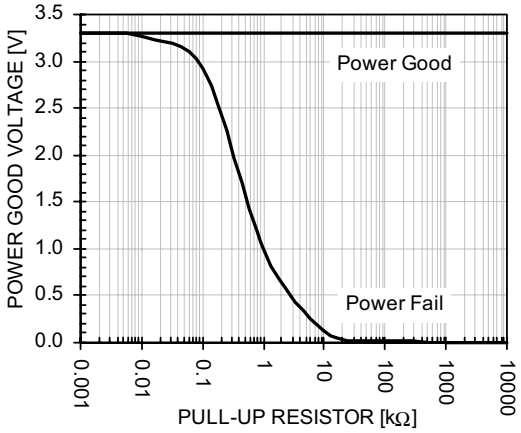
Line Regulation (1% and 100% rated load)



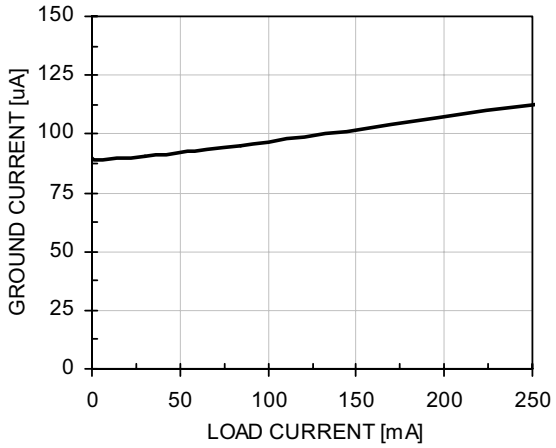
Foldback Current Protection



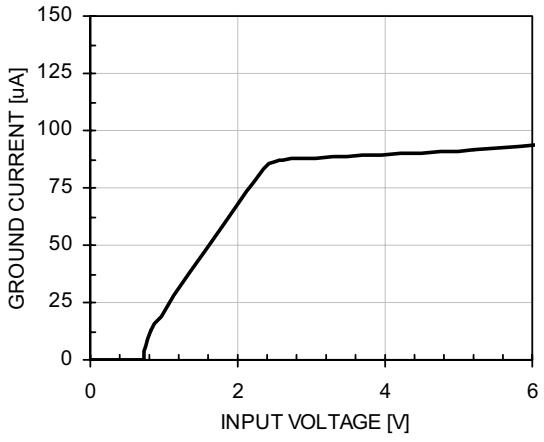
Power Good Pull-up Resistor vs. V_{PG}



Ground Current vs. Load Current (V_{IN}=3.3V)



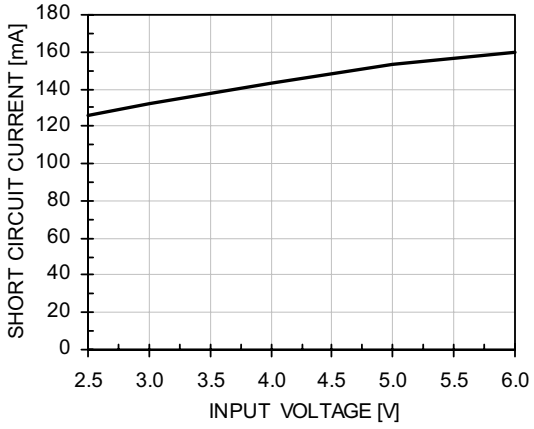
Ground Current vs. Input Voltage (1mA Load)



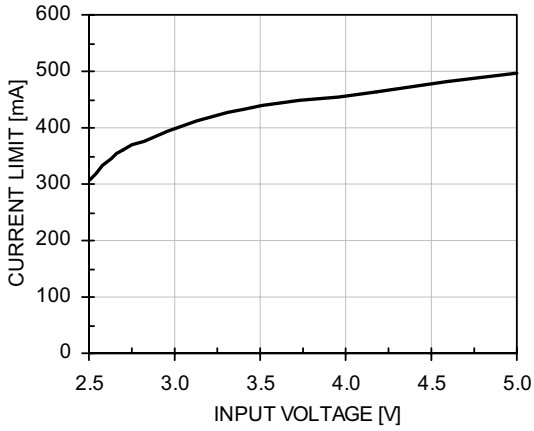
Performance Information (cont'd)

CM3102 Typical DC Characteristics (cont'd, nominal conditions unless specified otherwise)

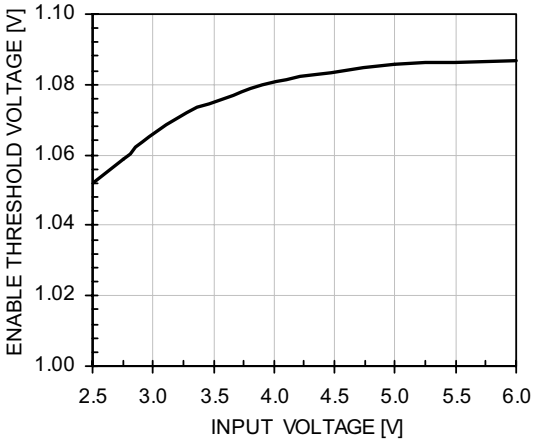
Short Circuit Current vs. Input Voltage



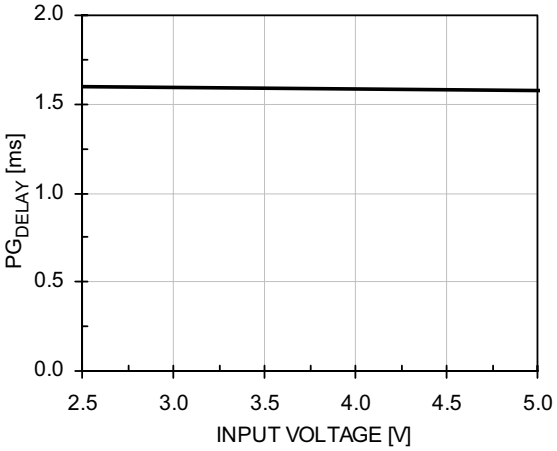
Current Limit vs. Input Voltage (V_{OUT}=1.15V)



Enable Voltage vs. Input Voltage



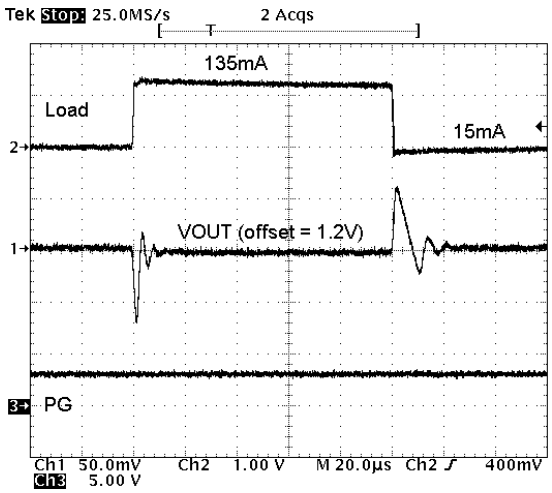
PG_{DELAY} vs. Input Voltage



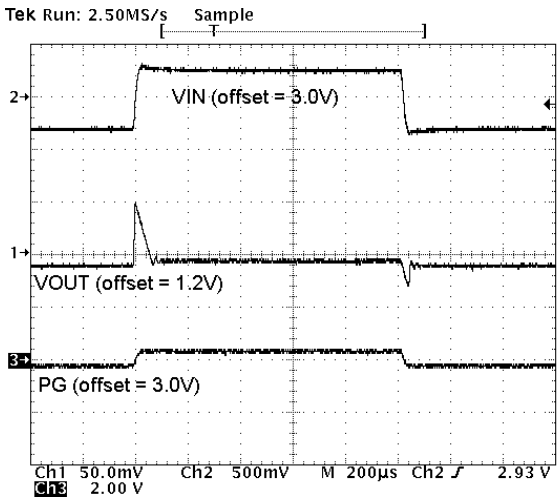
Performance Information (cont'd)

CM3102 Transient Characteristics (nominal conditions unless specified otherwise)
(PG connected to V_{IN} with a 47kΩ resistor)

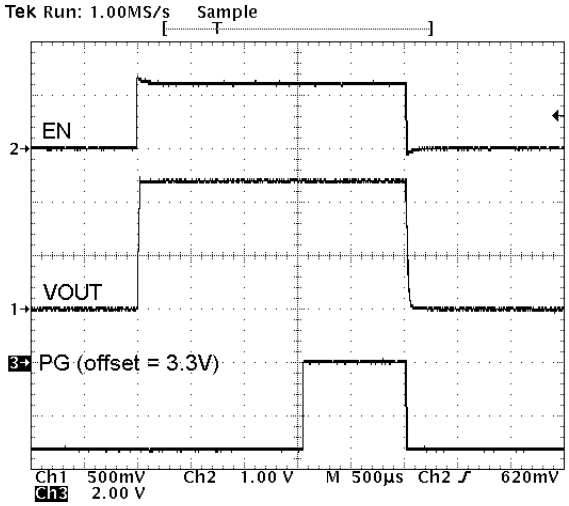
Load transient (10% to 90%) Step Response (V_{IN} = 3.3V, C_{IN} = C_{OUT} = 1uF Ceramic)



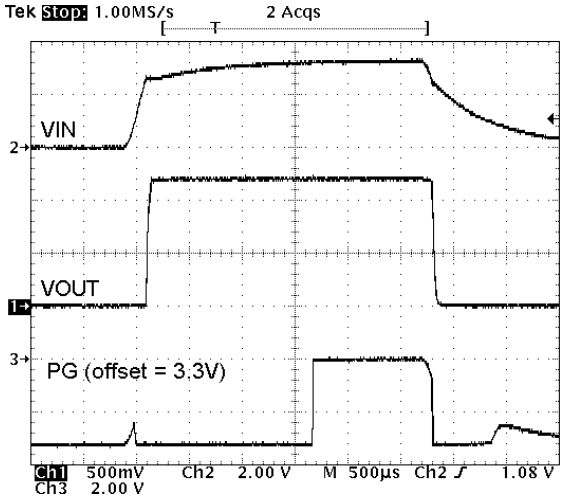
Line Transient (0.6Vpp) Step Response (1mA Load, C_{OUT} = 1uF Ceramic, no C_{IN})



Enable Response (150mA Load, C_{IN} = C_{OUT} = 1uF Ceramic)



Cold Start & Power Down (150mA Load, C_{IN} = C_{OUT} = 1uF Ceramic)



Performance Information (cont'd)

CM3102-12ST Typical Thermal Characteristics

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (PD) consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) which is defined by the package style, and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_D (\theta_{JC}) + P_D (\theta_{CA})$$
$$= T_{AMB} + P_D (\theta_{JA})$$

The CM3102-12ST uses a SOT23-5 package. When this package is mounted on a double sided printed circuit board with two square inches of copper allocated for "heat spreading", the resulting θ_{JA} is 175°C/W.

Based on a maximum power dissipation of 315mW (2.1Vx150mA), with an ambient of 70°C the resulting junction temperature will be:

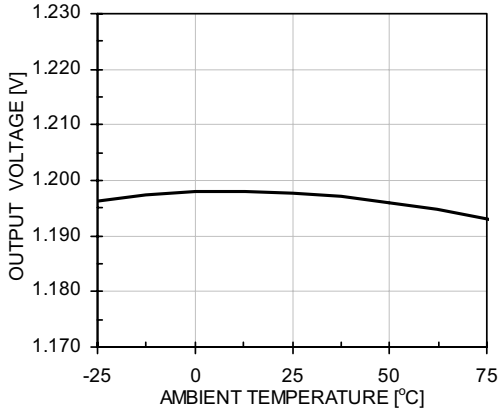
$$T_{JUNC} = T_{AMB} + P_D (\theta_{JA})$$
$$= 70°C + 315mW \text{ X } (175°C/W)$$
$$= 70°C + 55°C = 125°C$$

Thermal characteristics were measured using a double sided board with two square inches of copper area connected to the GND pin for "heat spreading".

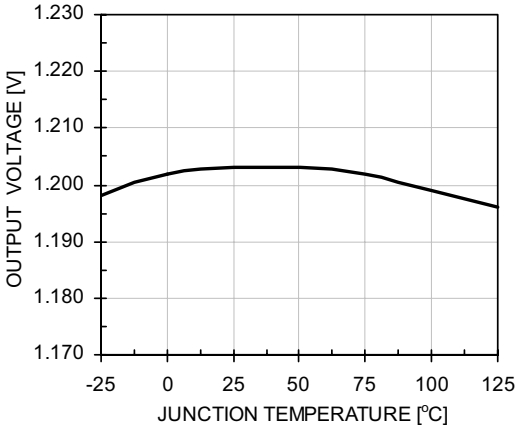
Measurements showing performance up to junction temperature of 125°C were performed under light load conditions (1mA). This allows the ambient temperature to be representative of the internal junction temperature.

Note: The use of multi-layer board construction with separate ground and power planes will further enhance the overall thermal performance. In the event of no copper area being dedicated for heat spreading, a multi-layer board construction, using only the minimum size pad layout, will provide the CM3102-12ST with an overall θ_{JA} of 175°C/W which allows up to 450mW to be safely dissipated for the maximum junction temperature.

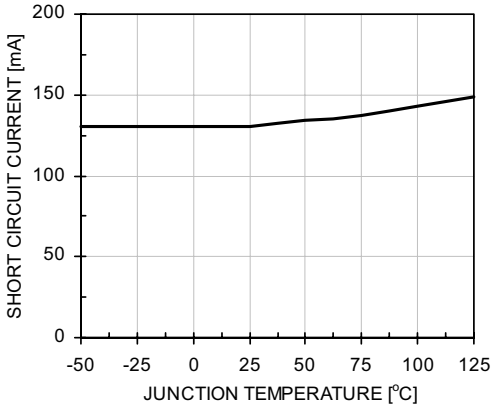
V_{OUT} Variation with T_{AMB} (150mA Load)



V_{OUT} Variation with T_{JUNCT} (1mA Load)



Short Circuit Current vs. T_{JUNCT}



Mechanical Details

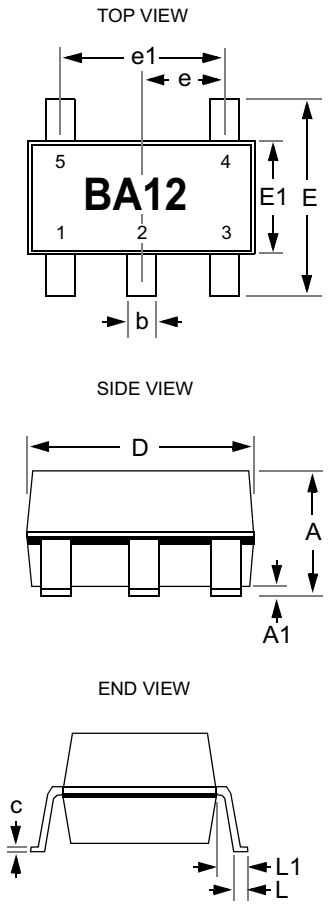
SOT23-5 Mechanical Specifications

Dimensions for CM3102-12ST device packaged in 5-pin SOT23 package are presented below.

For complete information on the SOT23-5 package, see the California Micro Devices SOT23 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT23-5 (JEDEC name is MO-178)			
Pins	5			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	--	1.45	--	0.0571
A1	0.00	0.15	0.0000	0.0059
b	0.30	0.50	0.0118	0.0197
c	0.08	0.22	0.0031	0.0087
D	2.75	3.05	0.1083	0.1201
E	2.60	3.00	0.1024	0.1181
E1	1.45	1.75	0.0571	0.0689
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.30	0.60	0.0118	0.0236
L1	0.60 REF		0.0236 REF	
# per tape and reel	3000 pieces			

Mechanical Package Diagrams



Package Dimensions for SOT23-5.