DATA SHEET

PCA9536
4-bit I^2C and SMBus I/O port

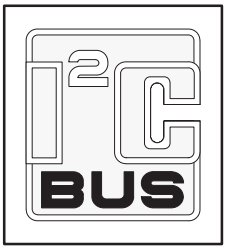
Objective data sheet

2004 Aug 20

Philips
Semiconductors

PHILIPS

4-bit I²C and SMBus I/O port PCA9536



FEATURES

- 4-bit I²C GPIO
- Operating power supply voltage range of 2.3 to 5.5 V
- 5 V tolerant I/Os
- Polarity inversion register
- Active low interrupt output
- Low stand-by current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 4 I/O pins which default to 4 inputs with 100 kΩ internal pull-up resistor
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Two packages offered: SO8 and TSSOP8

DESCRIPTION

The PCA9536 is 8-pin CMOS devices that provides 4 bits of General Purpose parallel Input/Output (GPIO) expansion for I²C/SMBus applications and were developed to enhance the Philips family of I²C I/O expanders. I/O expanders provides a simple solution when additional I/O is needed for ACPI power switches, sensors, pushbuttons, LEDs, fans, etc.

The PCA9536 consists of a 4-bit Configuration register (Input or Output selection); 4-bit Input register, 4-bit Output register and an 4-bit Polarity inversion register (Active-HIGH or Active-LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each Input or Output is kept in the corresponding Input or Output register. The polarity of the read register can be inverted with the Polarity Inversion Register. All registers can be read by the system master.

The power-on reset sets the registers to their default values and initializes the device state machine.

The I²C address is fixed and allows only one device on the same I²C/SMBus.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DRAWING NUMBER
8-Pin Plastic SO (wide)	–40 °C to +85 °C	PCA9536D	PCA9536	SOT96-1
8-Pin Plastic TSSOP	–40 °C to +85 °C	PCA9536DP	9536	SOT505-1

Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

PIN CONFIGURATION

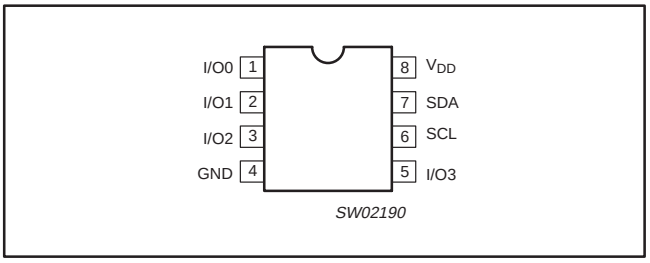


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 5	I/O0–3	I/O0 to I/O3
4	V_{SS}	Supply ground
6	SCL	Serial clock line
7	SDA	Serial data line
8	V_{DD}	Supply voltage

BLOCK DIAGRAM

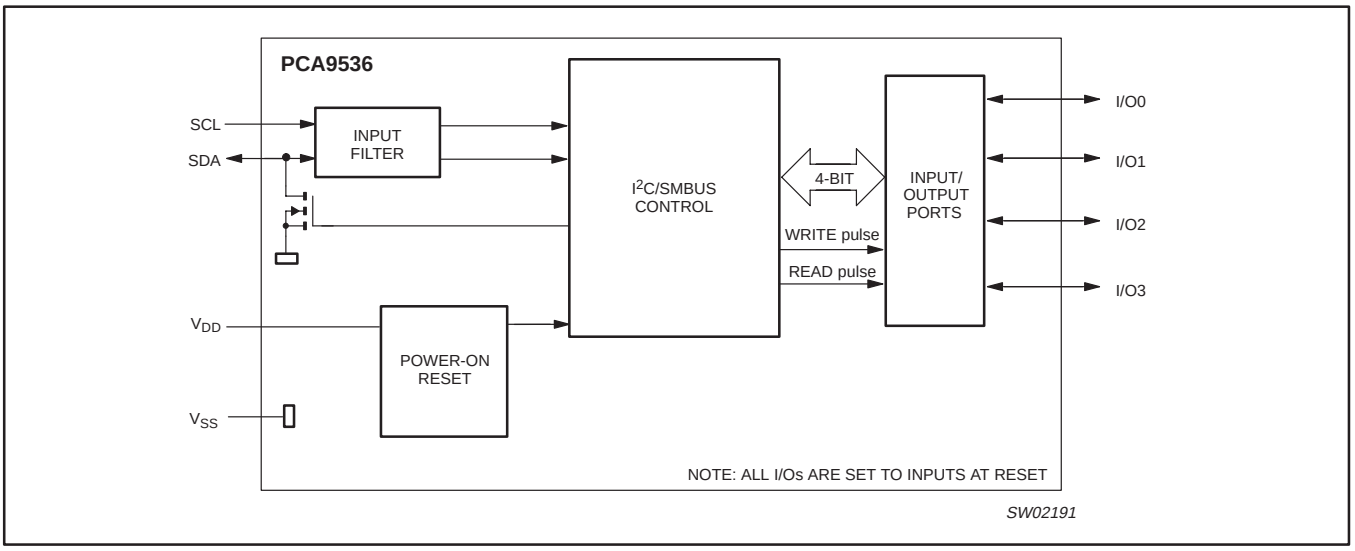


Figure 2. Block diagram

REGISTERS

Command Byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Register 0 – Input Port Register

bit	X	X	X	X	I3	I2	I1	I0
default	1	1	1	1	1	1	1	1

This register is a read only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

"X" are "don't care" bits and can be programmed with either "0" or "1".

Register 1 – Output Port Register

bit	X	X	X	X	O3	O2	O1	O0
default	1	1	1	1	1	1	1	1

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, NOT the actual pin value.

"X" are "don't care" bits and can be programmed with either "0" or "1".

Register 2 – Polarity Inversion Register

bit	X	X	X	X	N3	N2	N1	N0
default	0	0	0	0	0	0	0	0

This register allows the user to invert the polarity of the Input Port Register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

"X" are "don't care" bits and can be programmed with either "0" or "1".

Register 3 – Configuration Register

bit	X	X	X	X	C3	C2	C1	C0
default	1	1	1	1	1	1	1	1

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to V_{DD}.

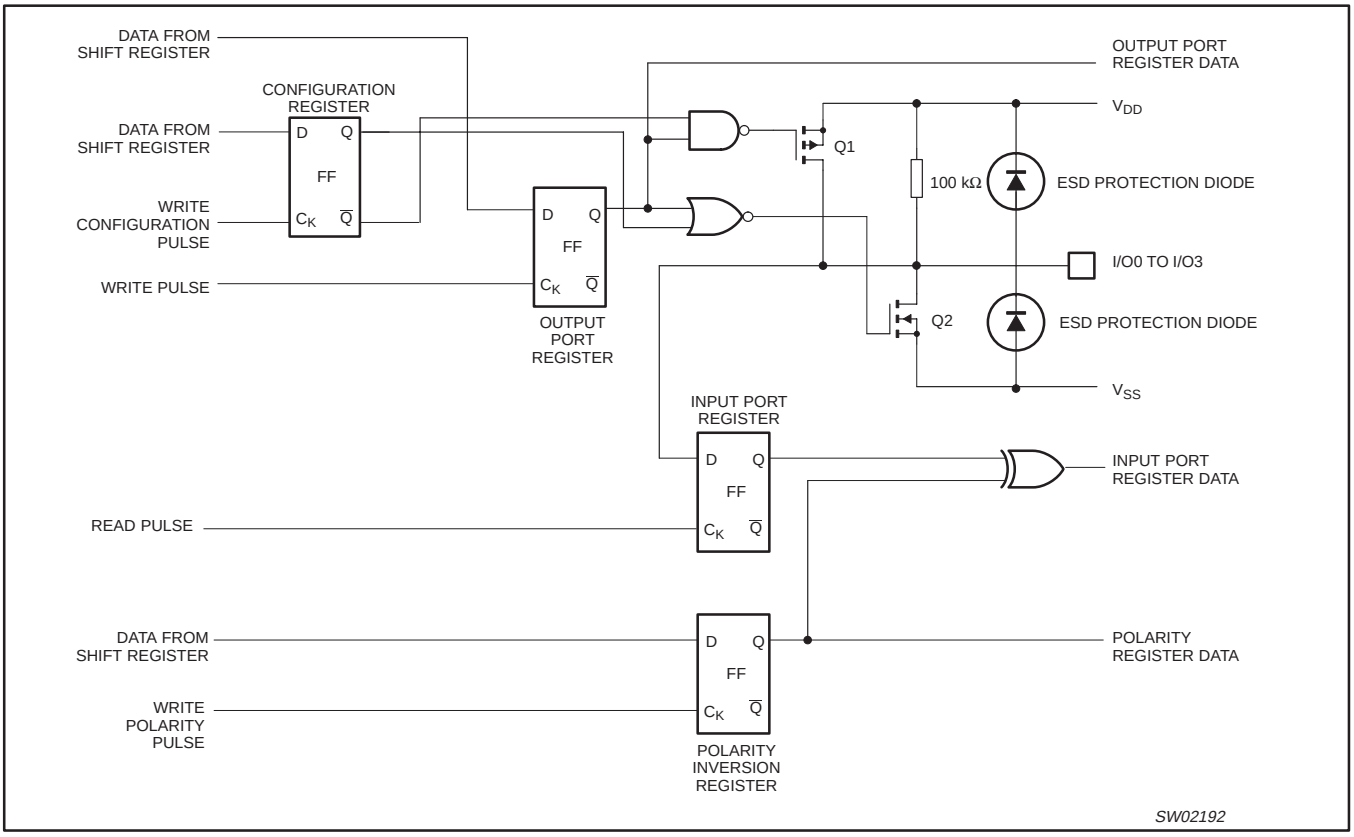
"X" are "don't care" bits and can be programmed with either "0" or "1".

Power-on Reset

When power is applied to V_{DD}, an internal power-on reset holds the PCA9536 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9536 registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

SIMPLIFIED SCHEMATIC OF I/O0 TO I/O3



NOTE: At Power-on Reset, all registers return to default values.

Figure 3. Simplified schematic of I/O0 to I/O3

I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high impedance input with a weak pull-up (100 kΩ typ.) to V_{DD}. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the output port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low impedance paths that exist between the pin and either V_{DD} or V_{SS}.

Device address

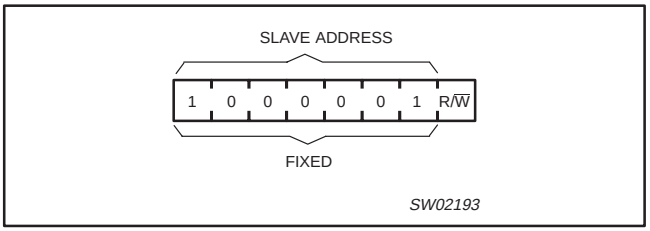


Figure 4. PCA9536 address

Bus transactions

Data is transmitted to the PCA9536 registers using the write mode as shown in Figures 5 and 6. Data is read from the PCA9536 registers using the read mode as shown in Figures 7 and 8. These devices do not implement an auto-increment function so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.

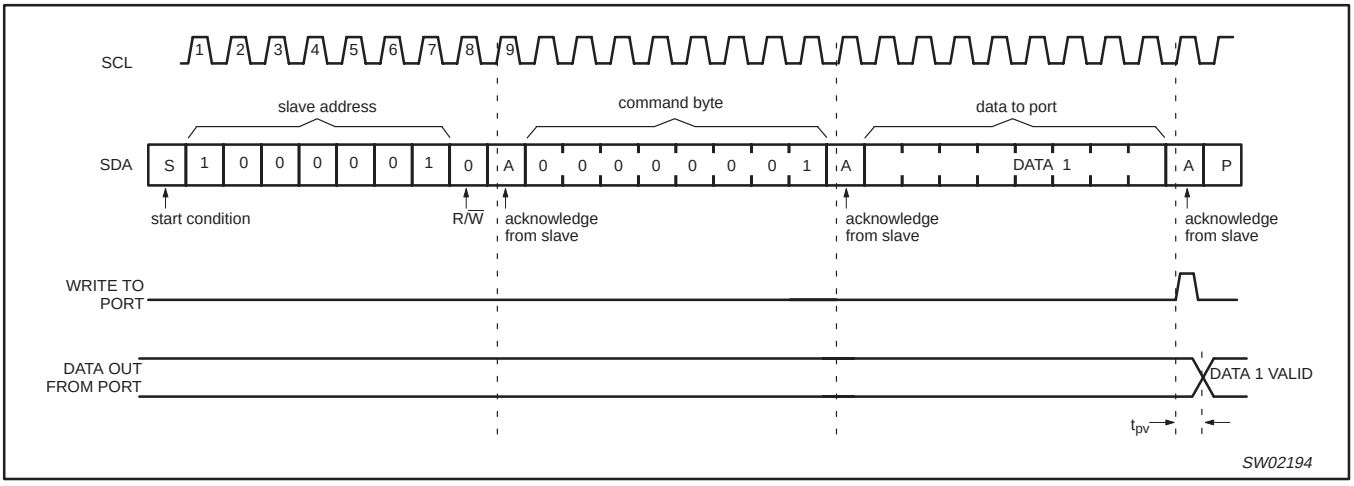


Figure 5. WRITE to output port register

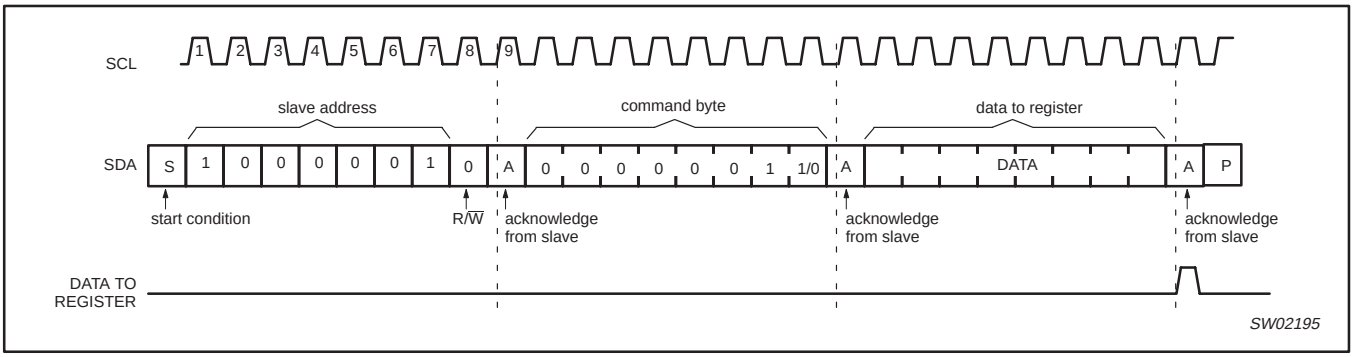


Figure 6. WRITE to configuration or polarity inversion registers

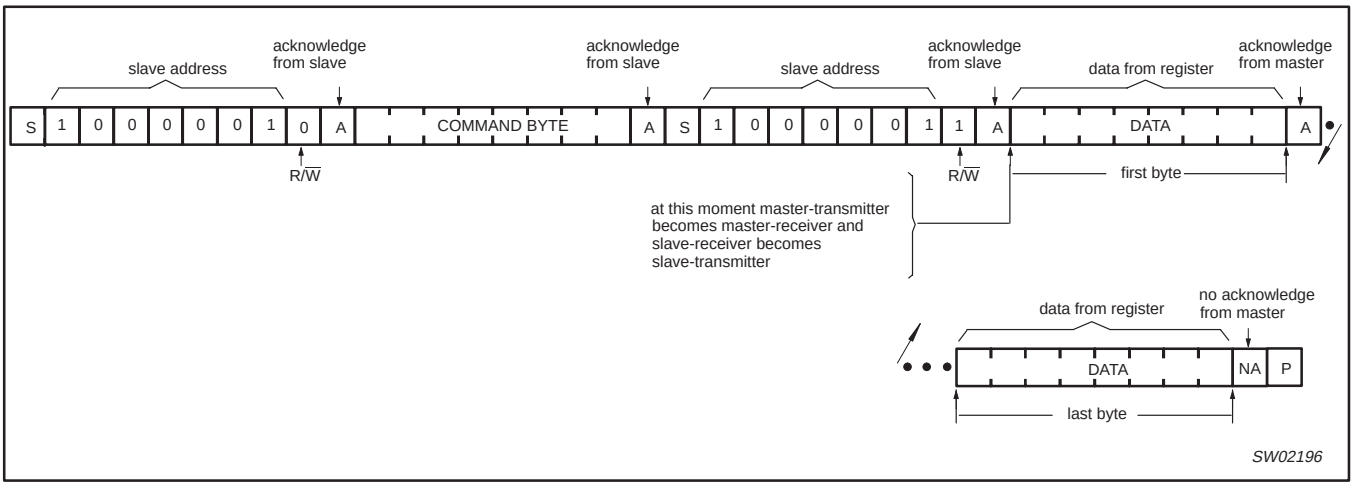
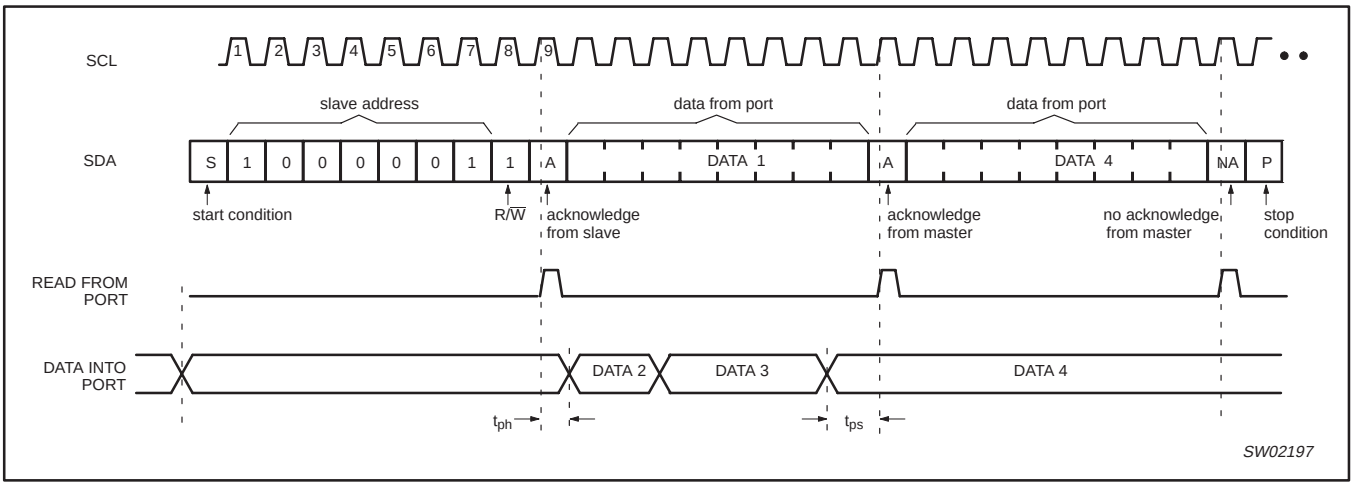


Figure 7. READ from register



NOTES:
1. This figure assumes the command byte has previously been programmed with 00h.
2. Transfer of data can be stopped at any moment by a stop condition.

Figure 8. READ input port register

TYPICAL APPLICATION

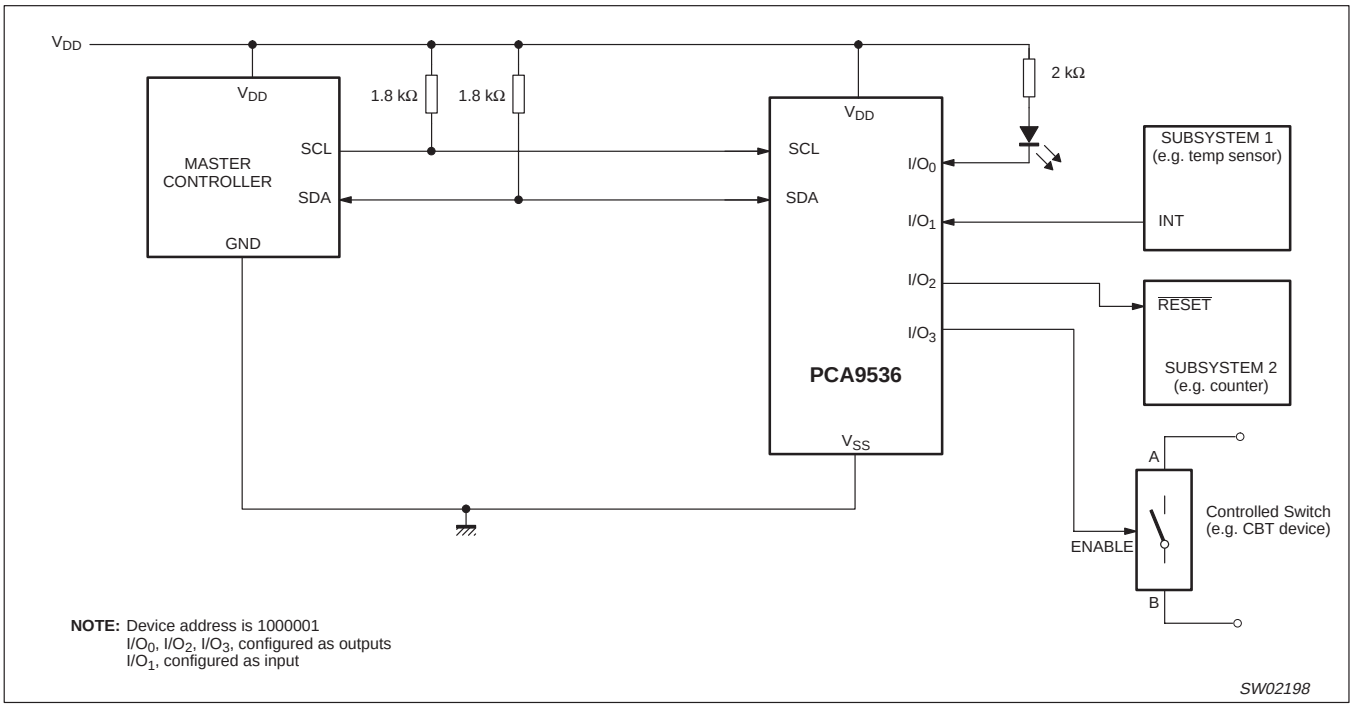


Figure 9. Typical application

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{DD}	Supply voltage		–0.5	6.0	V
I_I	DC input current		—	±20	mA
$V_{I/O}$	DC voltage on an I/O		V_{SS} – 0.5	5.5	V
$I_{I/O}$	DC output current on an I/O		—	±50	mA
I_{DD}	Supply current		—	85	mA
I_{SS}	Supply current		—	100	mA
P_{tot}	Total power dissipation		—	200	mW
T_{stg}	Storage temperature range		–65	+150	°C
T_{amb}	Operating ambient temperature		–40	+85	°C
$T_{J(MAX)}$	Maximum junction temperature		—	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "*Handling MOS devices*".

DC CHARACTERISTICS

V_{DD} = 2.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
V_{DD}	Supply voltage		2.3	—	5.5	V
I_{DD}	Supply current	Operating mode; V_{DD} = 5.5 V; no load; f_{SCL} = 100 kHz	—	104	175	µA
I_{stbl}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	—	225	350	µA
I_{stbh}	Standby current	Standby mode; V_{DD} = 5.5 V; no load; $V_I = V_{DD}$; f_{SCL} = 0 kHz; I/O = inputs	—	0.25	1	µA
V_{POR}	Power-on reset voltage (Note 1)	No load; $V_I = V_{DD}$ or V_{SS}	—	1.5	1.65	V
input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		–0.5	—	0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	tbd	—	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	–1	—	+1	µA
C_I	Input capacitance	$V_I = V_{SS}$	—	6	10	pF
I/Os						
V_{IL}	LOW-level input voltage		–0.5	—	0.8	V
V_{IH}	HIGH-level input voltage		2.0	—	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V; Note 2	8	10	—	mA
		V_{OL} = 0.7 V; V_{DD} = 2.3 V; Note 2	10	13	—	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V; Note 2	8	17	—	mA
		V_{OL} = 0.7 V; V_{DD} = 4.5 V; Note 2	10	24	—	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V; Note 2	8	14	—	mA
		V_{OL} = 0.7 V; V_{DD} = 3.0 V; Note 2	10	19	—	mA
V_{OH}	HIGH-level output voltage	I_{OH} = –8 mA; V_{DD} = 2.3 V; Note 3	1.8	—	—	V
		I_{OH} = –10 mA; V_{DD} = 2.3 V; Note 3	1.7	—	—	V
		I_{OH} = –8 mA; V_{DD} = 3.0 V; Note 3	2.6	—	—	V
		I_{OH} = –10 mA; V_{DD} = 3.0 V; Note 3	2.5	—	—	V
		I_{OH} = –8 mA; V_{DD} = 4.75 V; Note 3	4.1	—	—	V
		I_{OH} = –10 mA; V_{DD} = 4.75 V; Note 3	4.0	—	—	V
I_{IH}	Input leakage current	V_{DD} = 3.6 V; $V_I = V_{DD}$	—	—	1	µA
I_{IL}	Input leakage current	V_{DD} = 5.5 V; $V_I = V_{SS}$	—	—	–100	µA
C_I	Input capacitance		—	3.7	5	pF
C_O	Output capacitance		—	3.7	5	pF

NOTES:

1. V_{DD} must be lowered to 0.2 V in order to reset part.
2. The total current sunk by all I/Os must be limited to 100 mA.
3. The total current sourced by all I/Os must be limited to 85 mA.

AC SPECIFICATIONS

SYMBOL	PARAMETER	STANDARD MODE I²C-bus		FAST MODE I²C-bus		UNITS
		MIN	MAX	MIN	MAX	
f_{SCL}	Operating frequency	0	100	0	400	kHz
t_{BUF}	Bus free time between STOP and START conditions	4.7	—	1.3	—	µs
$t_{HD;STA}$	Hold time after (repeated) START condition	4.0	—	0.6	—	µs
$t_{SU;STA}$	Repeated START condition setup time	4.7	—	0.6	—	µs
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	µs
$t_{HD;DAT}$	Data in hold time	0	—	0	—	ns
$t_{VD;ACK}$	Valid time for ACK condition[2]	0.3	3.45	0.1	0.9	µs
$t_{VD;DAT}$	Data out valid time[3]	300	—	50	—	ns
$t_{SU;DAT}$	Data setup time	250	—	100	—	ns
t_{LOW}	Clock LOW period	4.7	—	1.3	—	µs
t_{HIGH}	Clock HIGH period	4.0	—	0.6	—	µs
t_F	Clock/Data fall time	—	300	20 + 0.1 C_b[1]	300	ns
t_R	Clock/Data rise time	—	1000	20 + 0.1 C_b[1]	300	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filters	—	50	—	50	ns
Port Timing						
t_{PV}	Output data valid	—	200	—	200	ns
t_{PS}	Input data setup time	100	—	100	—	ns
t_{PH}	Input data hold time	1	—	1	—	µs

NOTES:
1. C_b = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

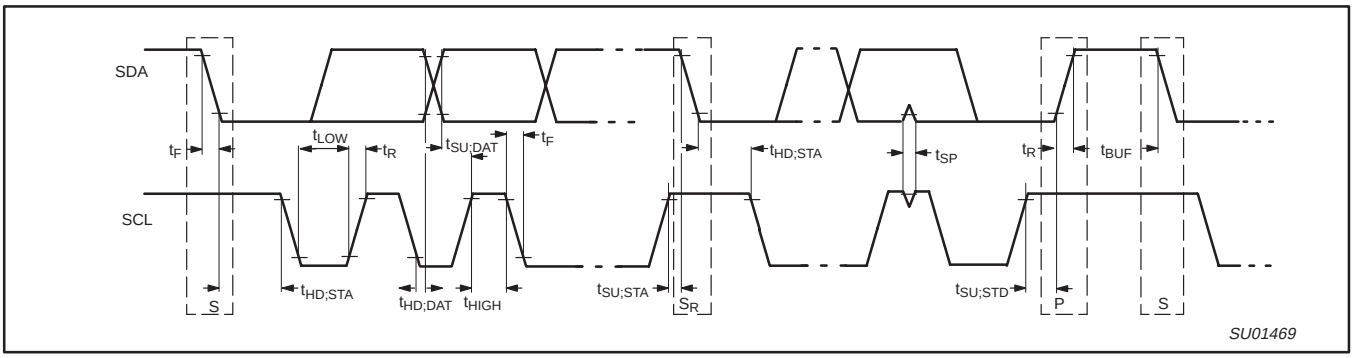


Figure 10. Definition of timing

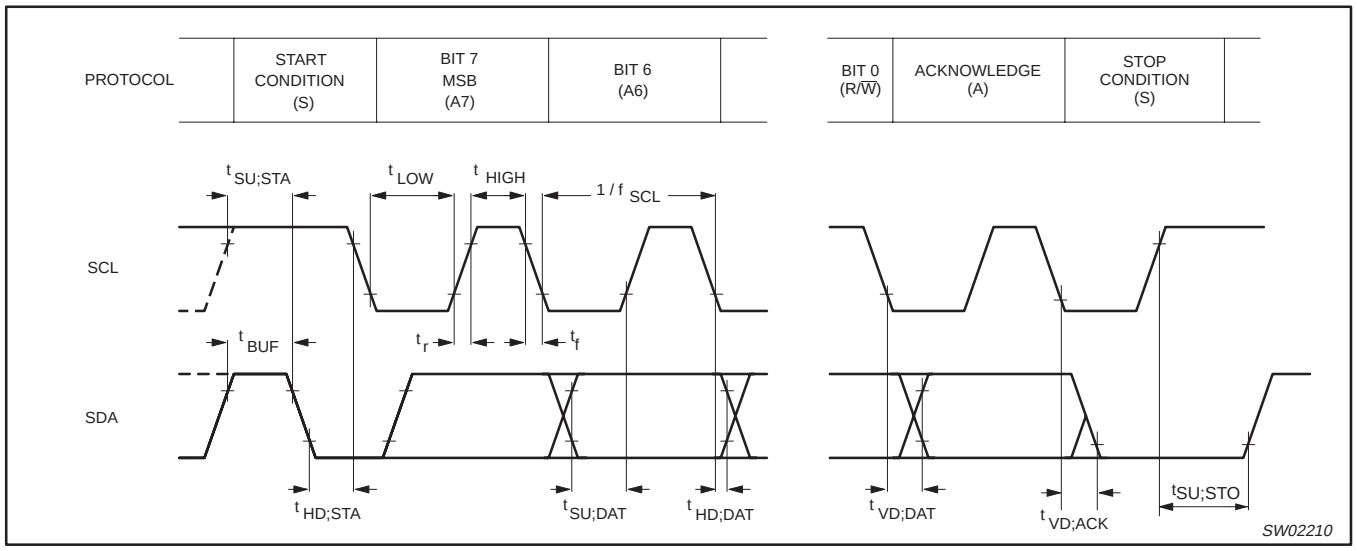
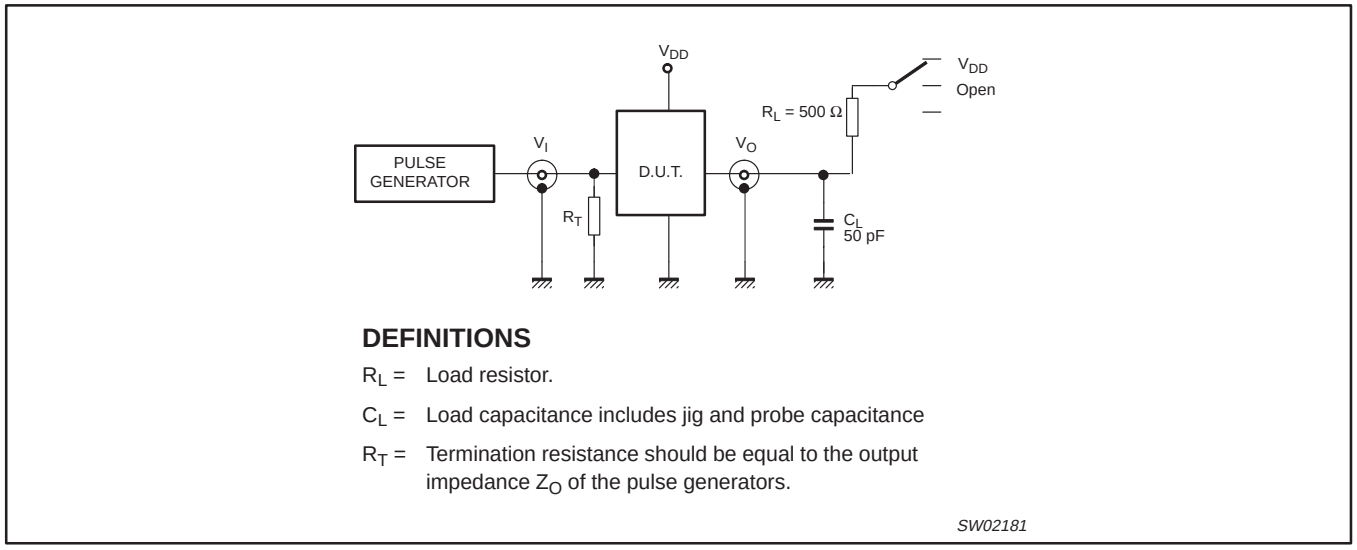


Figure 11. I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}



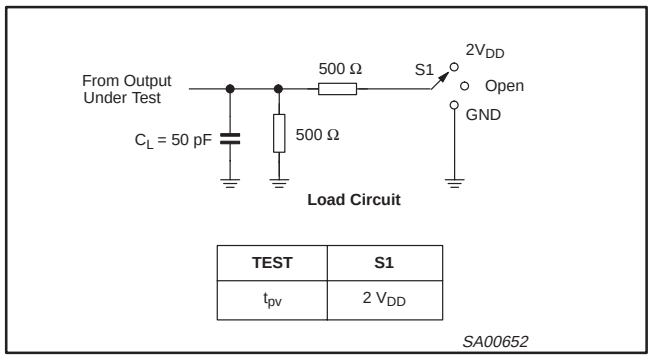
DEFINITIONS

R_L = Load resistor.

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generators.

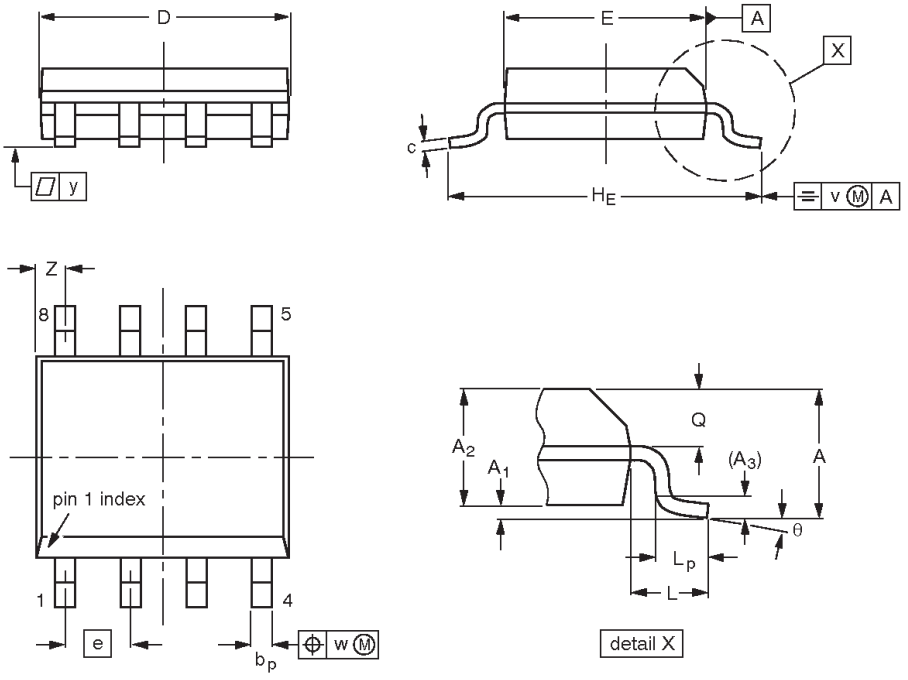
Figure 12. Test circuitry for switching times

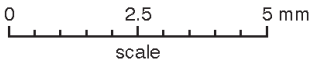


TEST	S1
t_{pv}	2 V_{DD}

Figure 13. Test circuit

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

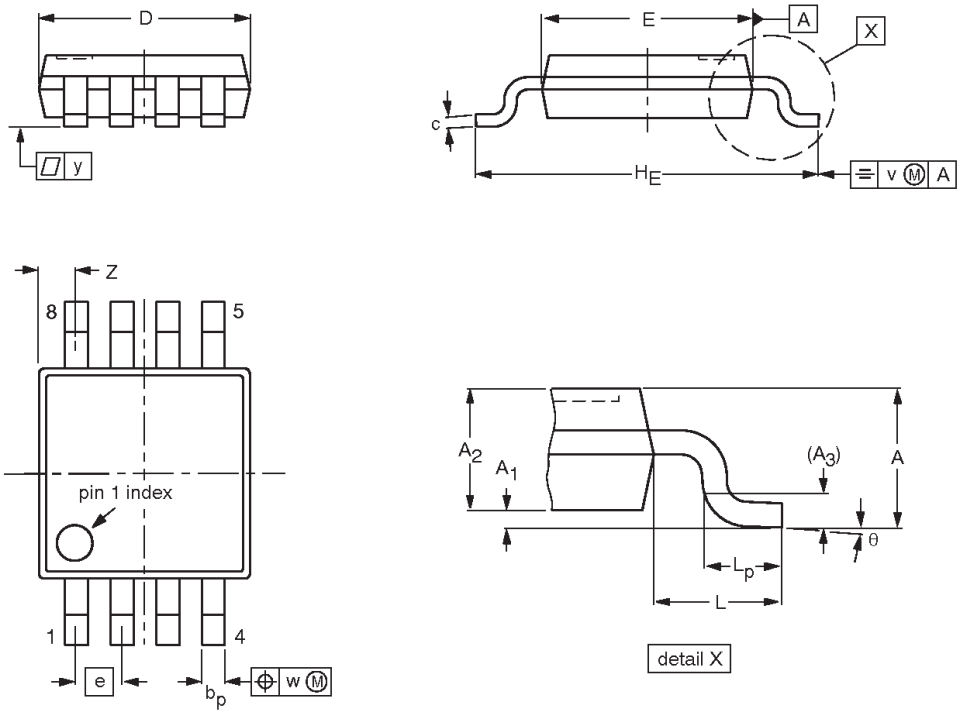
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

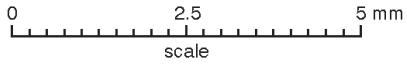
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

REVISION HISTORY

Rev	Date	Description
_1	20040820	**Objective data sheet (9397 750 12895).**

4-bit I²C and SMBus I/O port PCA9536

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data sheet	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data sheet	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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Date of release: 08-04

Document order number: 9397 750 12895

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