SIEMENS

Microcontrollers

ApNote AP2423

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AP242301.EXE available

New ASC Serial Interface
Async. Baudrate Calculation with the Fractional Divider

The new ASC Asynchronous/Synchronous Serial Interface allows programming of the desired baudrate very precisely in asynchronous modes, depending on the CPU clock rate. This ApNote describes the programming of the baudrate generator (fractional divider and baudrate reload timer) and provides an utility program for optimization of this step.

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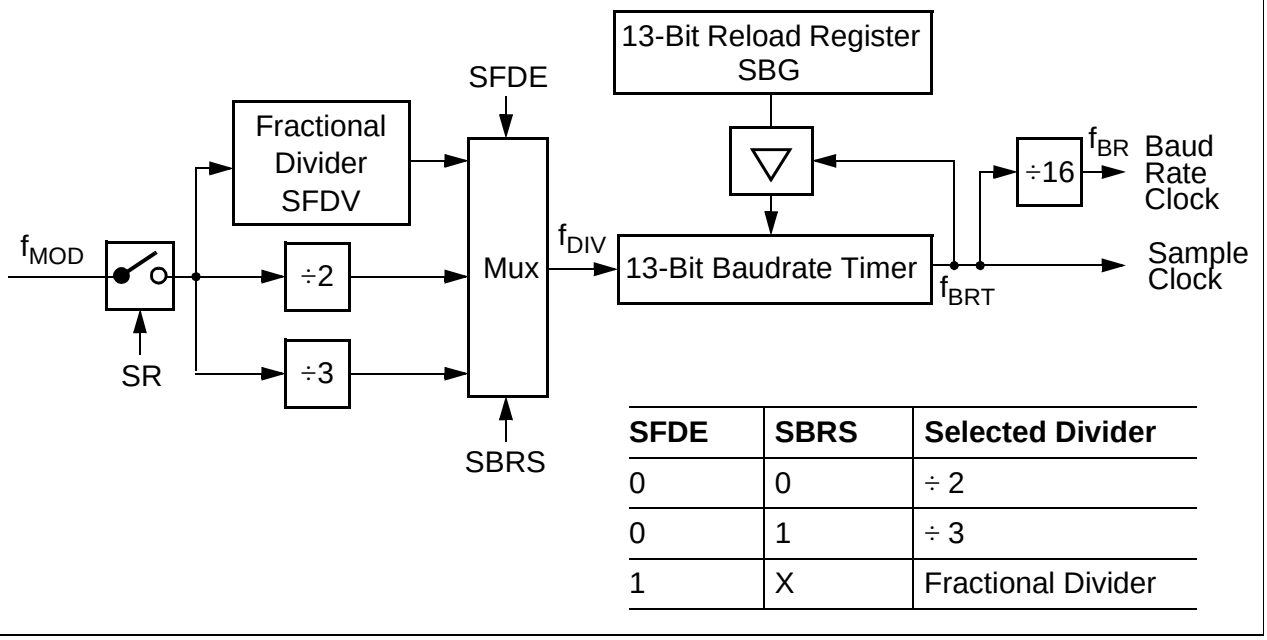
1 Baudrates in Asynchronous Mode

The baudrate generator of the new ASC serial interface has an improved baudrate generation circuitry as shown in **Figure 1**. Generally, the clock divider circuitry, which generates the input clock for the 13-bit baudrate timer, is extended by a fractional divider, which allows now the adjustment of more accurate baudrates and the extension of the baudrate range.



SFDE	SBRS	Selected Divider
0	0	÷ 2
0	1	÷ 3
1	X	Fractional Divider

Figure 1 :
ASC Baudrate Generator Circuitry in Asynchronous Modes

The frequency of the output clock of the baudrate generator depends on the following clock rates, bits, and register values :

- frequency of the input clock f_{MOD}
- selection of the baudrate timer input clock f_{DIV} by bits SFDE and SBRS (in SFR SCON)
- 9-bit value of register SFDV (if bit SFDE=1 - fractional divider enabled)
- value of the 13-bit reload register SBG

In the asynchronous modes of the ASC the output clock of the baudrate timer with its reload register is the sample clock f_{BRT}. For baudrate calculations, the baudrate clock f_{BR} is derived from this sample clock f_{BRT} by a division by 16.

Note: Abbreviations of bits and registers used in this ApNote
SBG : ASC Baud Rate Timer/Reload Register
SFDV: : ASC Fractional Divider Register
SCON : ASC Control Register
SFDE : bit SCON.11
SBRS : bit SCON.13

1.1 Using the fixed Input Clock Divider

The two fixed input clock dividers are still available for compatibility reason with the previous ASC serial interface. The baudrate for asynchronous operation of serial channel ASC when using the fixed input clock divider ratios (SFDE=0) and the required reload value for a given baudrate can be determined by the following formulas :

Table 1 :
Asynchronous Baudrate Formulas using the Fixed Input Clock Dividers

SFDE	SBRS	SBG	Formula
0	0	0 ... 8191	$\text{Baudrate} = \frac{f_{MOD}}{32 \times (SBG+1)}$ $SBG = \frac{f_{MOD}}{32 \times \text{Baudrate}} - 1$
	1		$\text{Baudrate} = \frac{f_{MOD}}{48 \times (SBG+1)}$ $SBG = \frac{f_{MOD}}{48 \times \text{Baudrate}} - 1$

SBG represents the content of the reload register SBG, taken as unsigned 13-bit integer.

1.2 Using the Fractional Divider

When the fractional divider is selected, the input clock f_{DIV} for the baudrate timer is derived from the module clock f_{MOD} by a programmable divider. If SFDE=1, the fractional divider is activated, It divides f_{MOD} by a fraction of n/512 for any value of n from 0 to 511. With n=0 (SBG=0), the divider ratio is 1 which means that $f_{DIV} = f_{MOD}$.

Table 2 :
Asynchronous Baudrate Formulas using the Fractional Input Clock Divider

SFDE	SBRS	SBG	SFDV	Formula
1	-	0 ... 8191	1 ... 511	$\text{Baudrate} = \frac{SFDV}{512} \times \frac{f_{MOD}}{16 \times (SBG+1)}$
			0	$\text{Baudrate} = \frac{f_{MOD}}{16 \times (SBG+1)}$

SBG represents the content of the reload register SBG, taken as unsigned 13-bit integer.
SFDV represents the content of the fractional divider register taken as unsigned 9-bit integer.

2 Comparision between Fractional Divider and Fixed Dividers

2.1 Improved Baudrate Range

The baudrate ranges that can be achieved for the asynchronous modes when using the two fixed clock dividers (±2 or ±3) and a module clock f_{MOD} of 25 MHz is :

– 781.25 kBaud down to 63.6 Baud
(maximum value = f_{MOD} / 32; minimum value = f_{MOD} / 393216)

With the fractional divider and a module clock f_{MOD} of 25 MHz the available baudrate range is :

– 1.5625 MBaud down to 0.373 Baud
(maximum value = f_{MOD} / 16; minimum value = f_{MOD} / 67108864)

This example shows the improved range of the new ASC serial interface in asynchronous mode when using the new fractional divider.

2.2 Improved Baudrate Accuracy

The accuracy of a requested baudrate derived from a fixed module clock f_{MOD} is also a feature which has been improved with the fractional divider.

Example : requested baudrate = 19.2 kBaud at f_{MOD} = 25 MHz

With the two fixed clock dividers (±2 or ±3) the accuracy is :

– - 0.76% (with ±2 prescaler selected and SBG = 40)
– + 0.45% (with ±3 prescaler selected and SBG = 26)

With the fractional divider the following accuracy can be achieved :

– ± 0.01% (see the example in **chapter 3**)

This example shows the drastically improved accuracy of the adjustment for baudrates of the new ASC serial interface in asynchronous mode when using the new fractional divider. For optimization of the fractional divider parameters (SFDV and SBG have to be calculated), an utility program has been created which allows to select the best SFDV/SBG parameter cobination for a specific accuracy.

3 Baudrate Calculation Program ASC.EXE

The program ASC.EXE calculates the two divide factors needed for the new ASC module when using the fractional divider for baudrate calculation.

The other baudrate generator modes (fixed dividers) are not considered, because they are included only for backward compatibility and provide much worse accuracy. The program is able to find any combination of the two parameters which satisfies the required baudrate based on the module input clock and the requested accuracy.

At the first time the program should be started with the maximum accuracy of 0.01% to limit the size of the output file. Only if there are no valid parameters the accuracy requirements can be reduced step by step.

The program file AP242301.EXE (selfextracting ZIP file) contains :

- the program ASC.EXE
- an example of the generated output file ASC.TXT
- a readme file README.TXT

It has to be noted, that the program currently makes no consistancy checks (like to ensure that the baudrate is less than $f_{MOD}/16$ etc.)

Note : ASC.EXE runs only on a PC (DOS, WINDOWS) not on SUN (UNIX) workstations !

The example below shows the content of the output file ASC.TXT (generated by ASC.EXE) when the follwing parameters are used :

- 25 MHz ASC module clock rate (f_{MOD})
- 19.2 kBaud baudrate requested
- accuracy at least 0.01 %

```
 Baudrate calculation program (V0.1) for the ASC module
 when using the fractional divider (SFDE=1)
================================================
 Selected module clock rate :  25000000 Hz
 Requested baudrate         :     19200 Baud
 Selected max. deviation    :      0.01 %
================================================
 SFDV    SBG   Baudrate    Deviation
                         abs.      rel.
------------------------------------------------
  151     23     19201     1    0.0000
  302     47     19201     1    0.0000
  346     54     19198    -2   -0.0001
  453     71     19201     1    0.0000
  497     78     19199    -1   -0.0001
------------------------------------------------
 5 combinations found
```

With this example, four combinations of SFDV and SBG values have been found with a minimum error of < ± 1 Baud within the limit of ± 0.01%. These combinations can be then used for baudrate programming.