AU9330
USB Secure Digital Card Reader
Technical Reference Manual

Revision 1.0

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1.0 Introduction

1.1 Description

The AU9330 is a single chip integrated USB Secure Digital (SD) card reader controller. It supports Secure Digital (SD) and Multimedia Card (MMC) with automatic card type detection capability. It can be used as a removable storage disk in enormous data exchange applications between PC and PC or PC and various consumer electronic devices.

The AU9330 can read Secure Digital card's contents created by handheld consumer electronic devices such as digital camera, MP3 player, PDA and mobile phone.., etc. It provides a faster and convenient way of data transfer scheme to meet the emerging need of a data exchange center between PC and various consumer devices. With AU9330, users' experience will be further enhanced by the Plug-and-Play nature built into latest operation systems such as Windows XP and MacOS X.

1.2 Features

- Fully compliant with USB v1.1 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Fully compliant with Secure Digital (SD) v1.0 Specification.
- Work with default driver from Windows ME, Windows 2000, Windows XP, Mac OS 9.1, and Mac OS X. Windows 98 is supported by vendor driver from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer to optimize performance
- LED for bus activity monitoring
- Runs at 12MHz, built-in 48 MHz PLL
- Built-in 3.3V regulator
- 44-pin LQFP package

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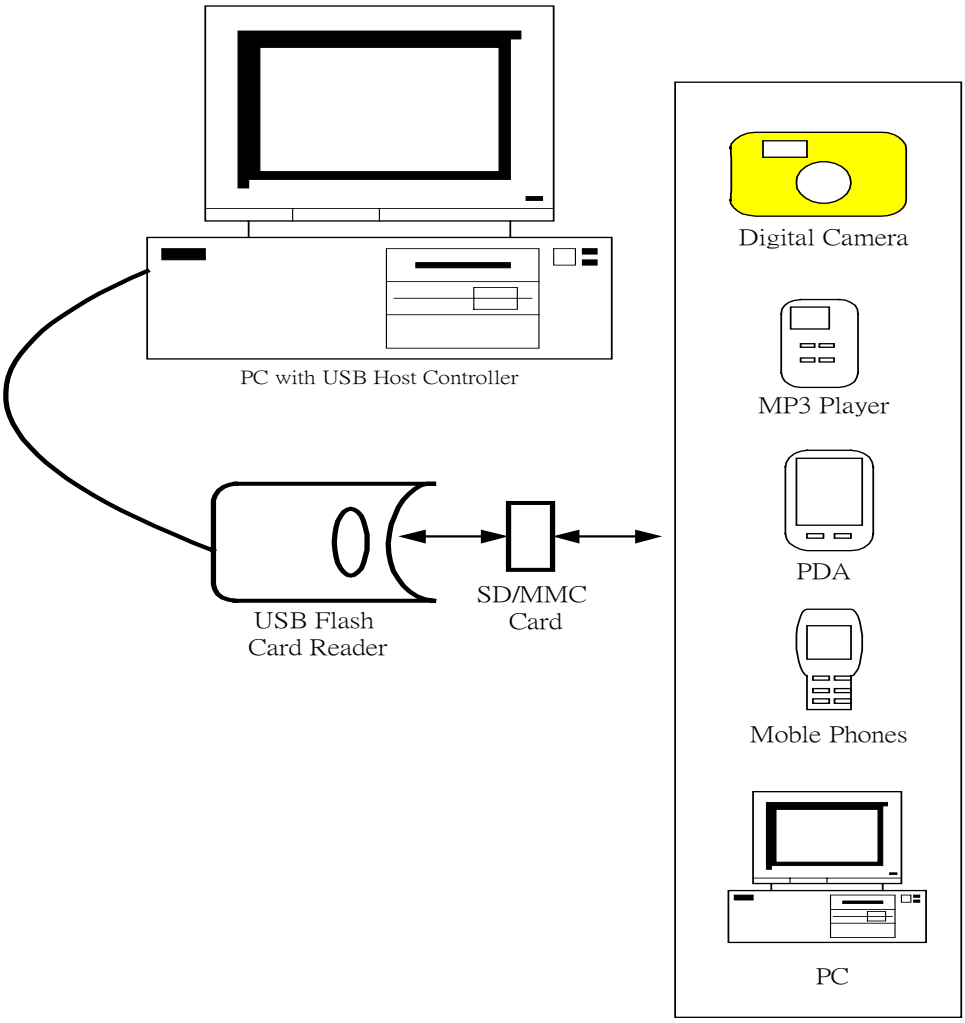
2.0 Application Block Diagram

Following is the application diagram of a typical flash memory card reader using AU9330. By connecting the reader to a PC through USB bus, the AU9330 is acting as a bridge between the flash memory card from digital camera, MP3 player, PDA or mobile phone and PC.



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3.0 Pin Assignment

The AU9330 is packed in 44-LQFP form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

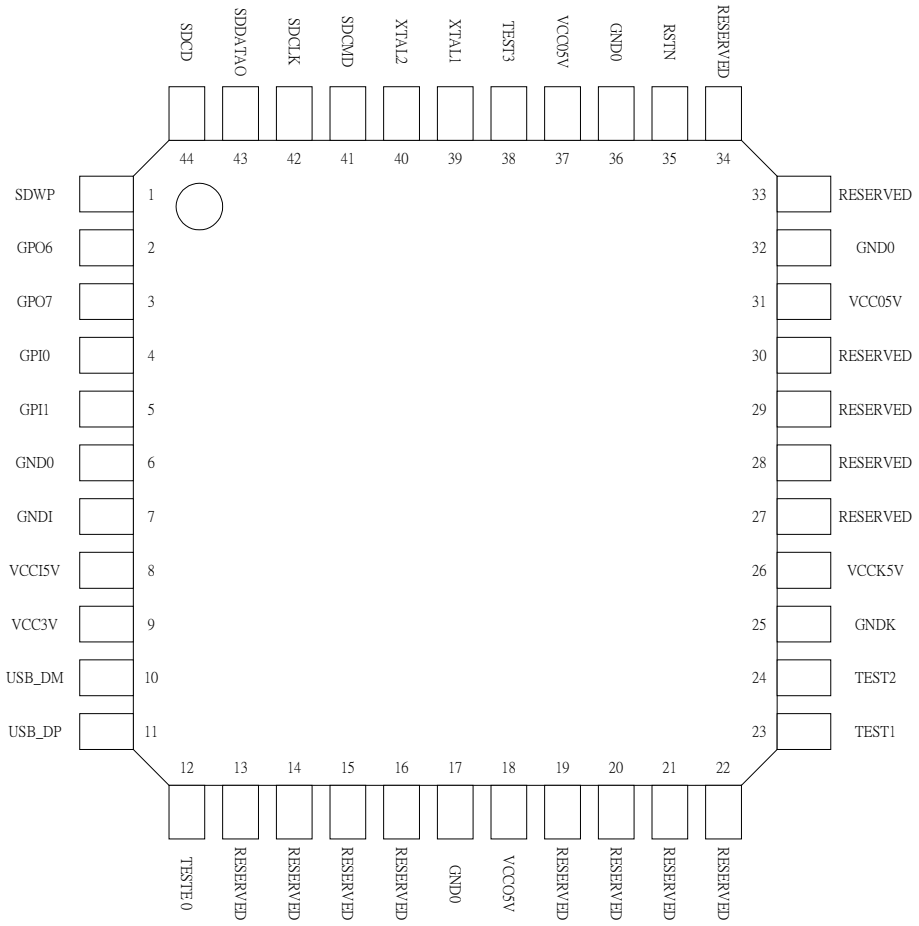
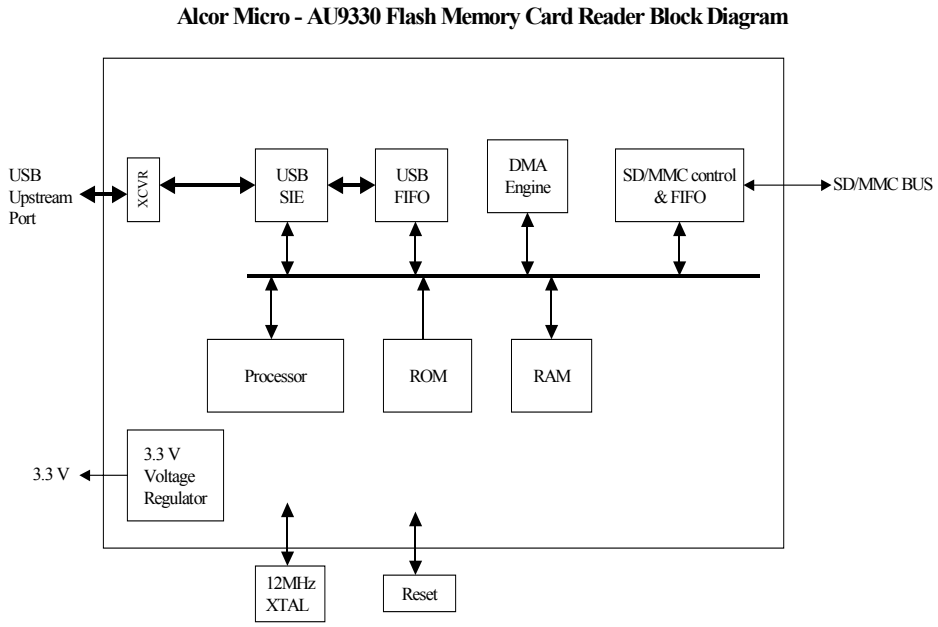


Table 3-1. Pin Descriptions

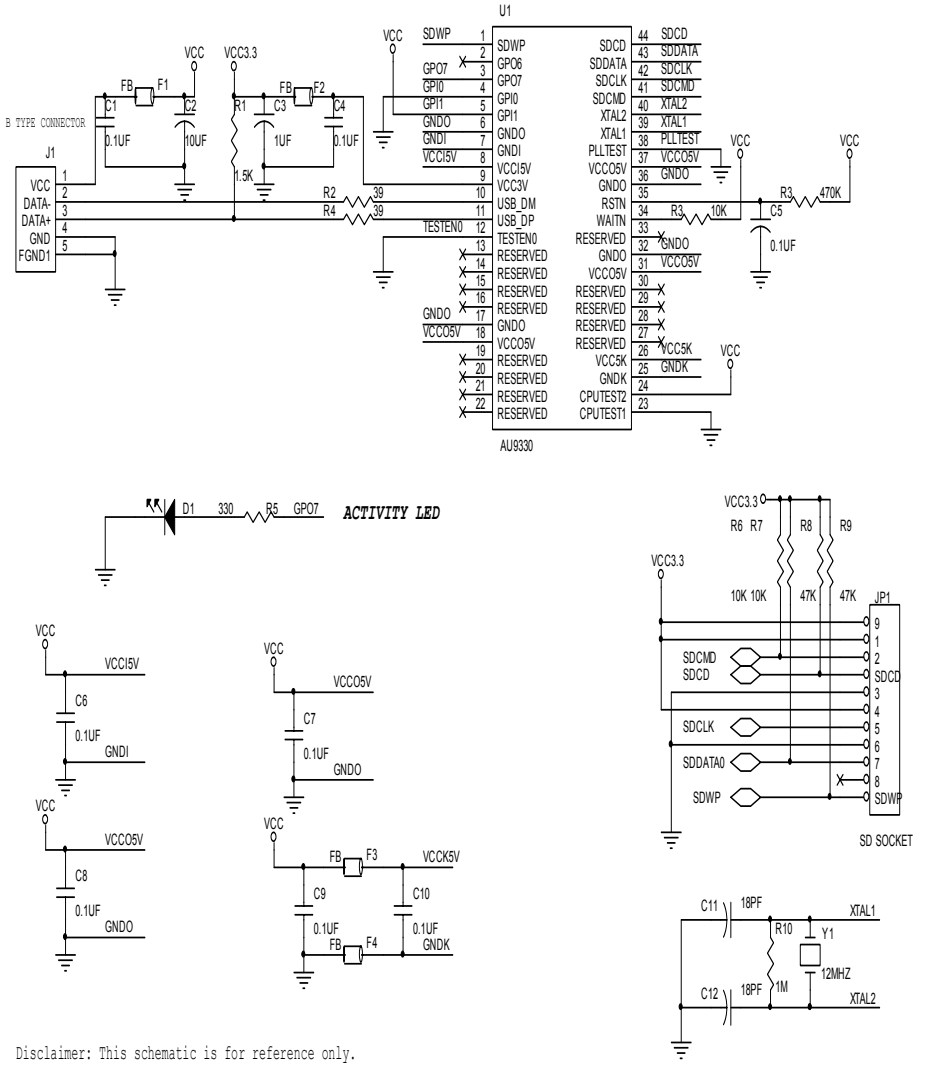
pin	Name	IO Type	Discription
1	SDWP	I	SD Write Protect
2	GPO6	O	General Purpose Output pin
3	GPO7	O	General Purpose Output pin, used as activity LED
4	GPI0	I	Should be connected to GND
5	GPI1	I	Should be connected to VCC
6	GNDO	PWR	
7	GNDI	PWR	
8	VCCI5V	PWR	
9	VCC3V	O	Regulated 3.3 Volt for DP pull up
10	USB_DM	I/O	USB D-
11	USB_DP	I/O	USB D+
12	TEST 0		Should connected to GND
13	RESERVED	NC	
14	RESERVED	NC	
15	RESERVED	NC	
16	RESERVED	NC	
17	GNDO	PWR	
18	VCC05V	PWR	5V input voltage
19	RESERVED	NC	
20	RESERVED	NC	
21	RESERVED	NC	
22	RESERVED	NC	
23	TEST1	I	Should connected to GND
24	TEST2	I	Should connected to VCC
25	GNDK	PWR	
26	VCCK5V	PWR	5V input voltage
27	RESERVED	NC	
28	RESERVED	NC	
29	RESERVED	NC	
30	RESERVED	NC	
31	VCC05V	PWR	5V input voltage
32	GNDO	PWR	
33	RESERVED	NC	
34	RESERVED	NC	
35	RSTN	I	Hardware reset (Active Low)
36	GNDO	PWR	
37	VCC05V	PWR	5V input voltage
38	TEST3	I	Should be connected to GND
39	XTAL1	I	Crystal Oscillator Input(12MHz)
40	XTAL2	O	Crystal Oscillator Output(12MHz)
41	SDCMD	I.O	SD Card Command
42	SDCLK	O	SD Card Clock
43	SDDATA0	I/O	SD Card Data 0
44	SDCD	I	SD Card Detect

4.0 System Architecture and Reference Design

4.1 AU9330 Block Diagram



4.2 Sample Schematics



Disclaimer: This schematic is for reference only. Alcor Micro Corp. makes no warranty for the use of its products and bears no responsibility for any error that appear in this document. Specifications are subject to change without notice.

Size	Document Number	Rev
A	AU9330 USB SD/MMC READER DEMO BOARD	1.0b
Date: Friday, December 14, 2001	Sheet 1 of 1	

5.0 Electrical Characteristics

5.1 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.75	5	5.25	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	0		85	^{O}C
T_{STG}	Storage Temperature	-40		125	^{O}C

5.2 General DC Characteristics

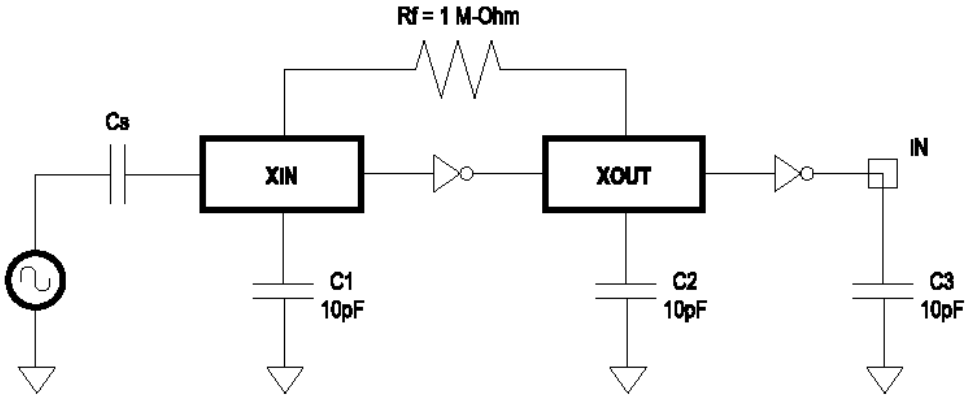
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	μA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	μA
I_{OZ}	Tri-state leakage current		-10		10	μA
C_{IN}	Input capacitance			5		ρF
C_{OUT}	Output capacitance			5		ρF
C_{BID}	Bi-directional buffer capacitance			5		ρF

5.3 DC Electrical Characteristics for 3.3 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS			0.9	V
V_{IH}	Input Hight Voltage	CMOS	2.3			V
V_{OL}	Output low voltage	I_{OL}=4mA, 16mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=4mA,16mA	2.4			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		10k/200k		KΩ

5.4 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.



5.5 ESD Test Results

Test Description : ESD Testing was performed on a Zapmaster system using the Human-Body –Model (HBM) and Machine-Model (MM), according to MIL_STD 883 and EIAJ IC_121 respectively.

- Human-Body-Model stress devices by sudden application of a high voltage supplied by a 100 PF capacitor through 1.5 Kohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200 PF capacitor through very low (0 ohm) resistance

Test circuit & condition

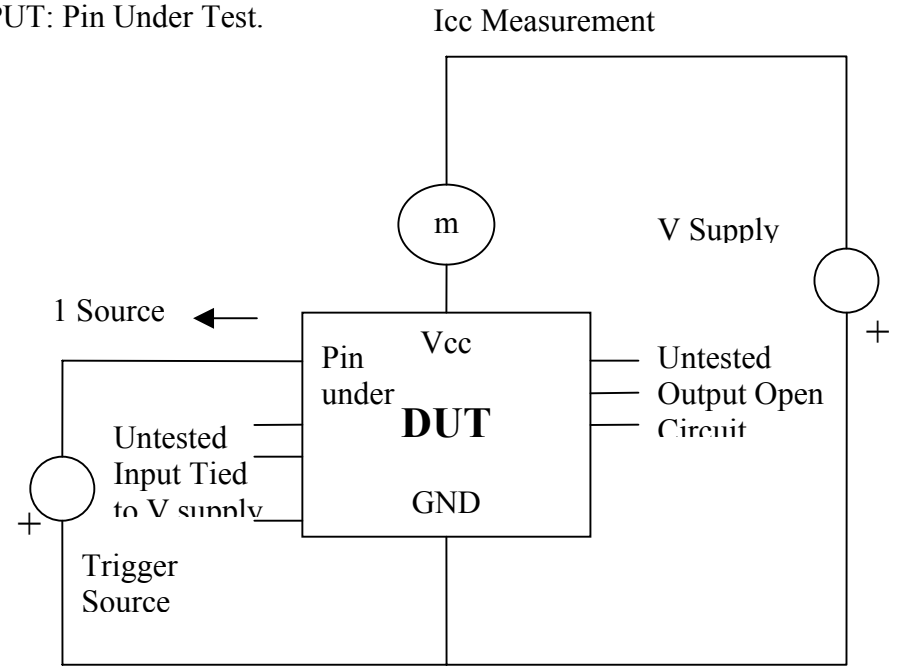
- Zap Interval : 1 second
- Number of Zaps : 3 positive and 3 negative at room temperature
- Critera : I-V Curve Tracing

Model	Model	S/S	TARGET	Results
HBM	Vdd, Vss, I/C	15	4000V	Pass
MM	Vdd, Vss, I/C	15	200V	Pass

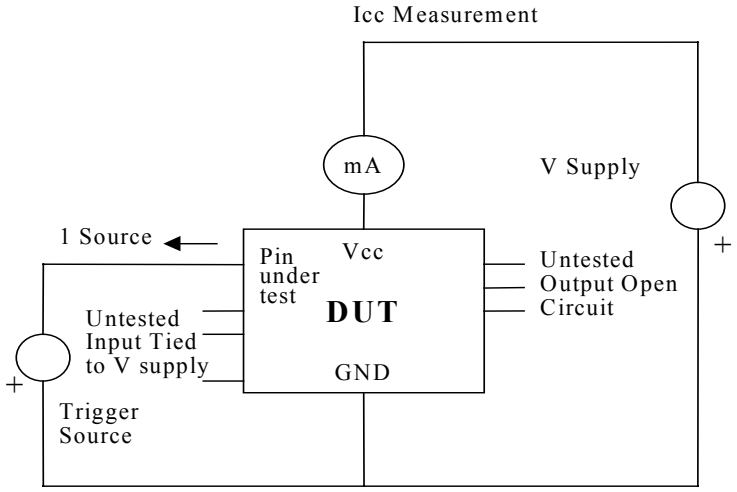
5.6 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5 Volts and ground respectively.
Testing was started at 5.0 V (Positive) or 0 V(Negative), and the DUT was biased for 0.5 seconds.
If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=0 mA , Icc=100 mA), then the voltage was increased by 0.1 Volts and the pin was tested again.
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

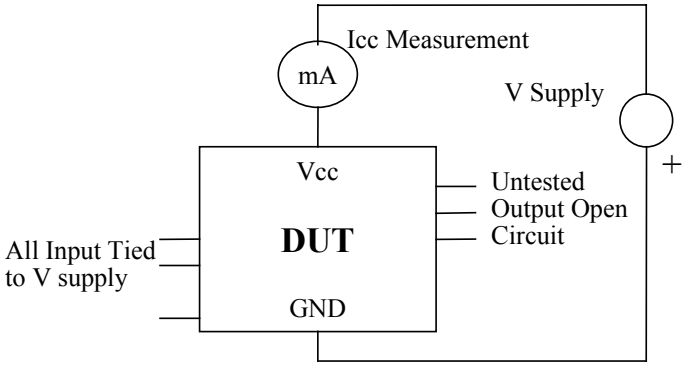
Notes:
1. DUT: Device Under Test.
2. PUT: Pin Under Test.



Test Circuit : Positive Input/ output Overvoltage /Overcurrent



Test Circuit : Negative Input/ Output Overvoltage /Overcurrent



Supply Voltage test

Latch–Up Data

Model	Model	Voltage (v)/ Current (mA)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0		
Current	+	200	5	
	-	200		
Vdd-Vxx		9.0	5	Pass

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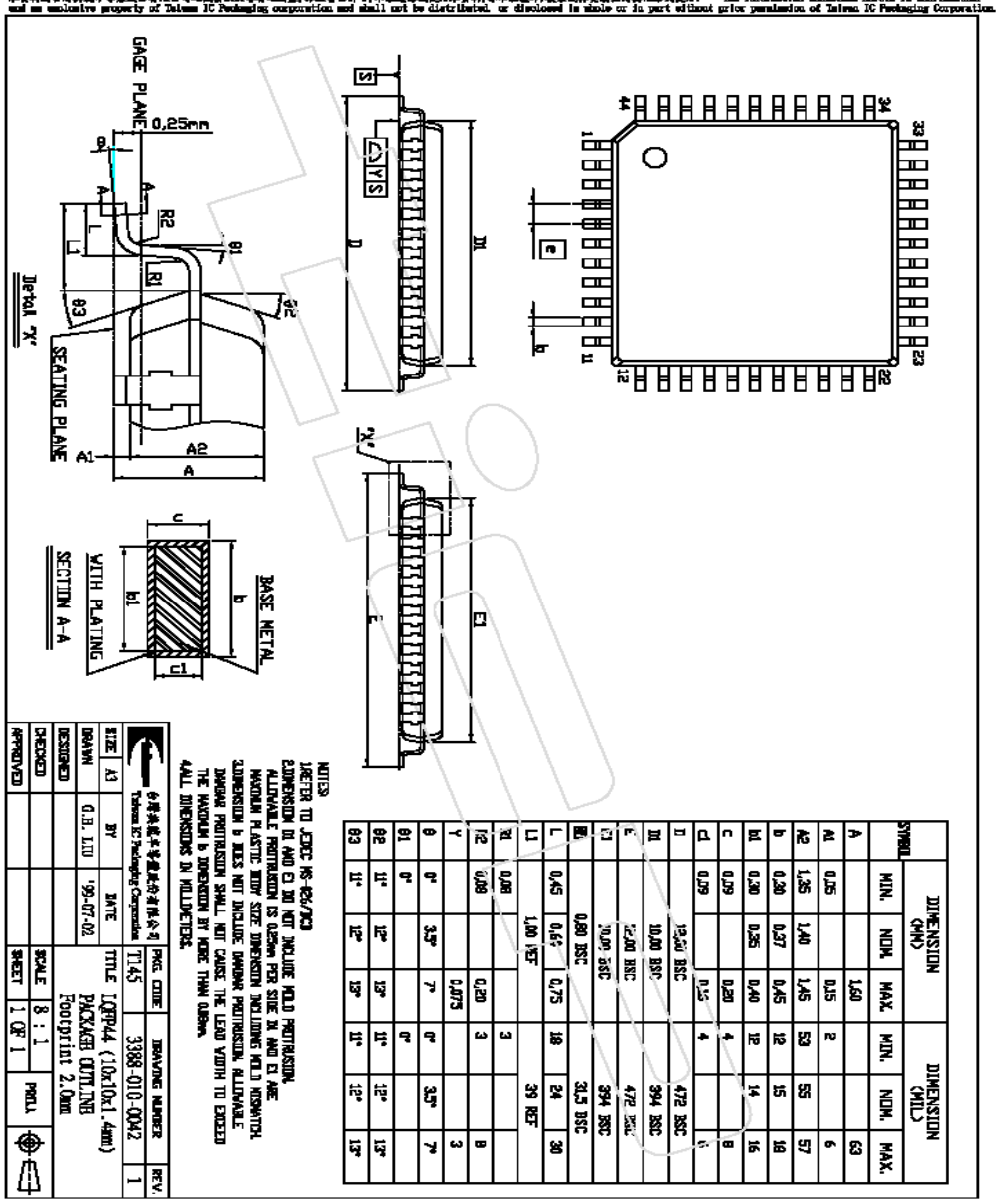
6.0 Mechanical Information



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.30	0.37	0.45	12	15	18
b1	0.30	0.35	0.40	12	14	16
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		12.00 BSC			472 BSC	
D1		10.00 BSC			394 BSC	
E		12.00 BSC			472 BSC	
E1		10.00 BSC			394 BSC	
e		0.80 BSC			31.5 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°