PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8520

LOW SKEW, 1-TO-16 DIFFERENTIAL-TO-3.3V LVHSTL FANOUT BUFFER

GENERAL DESCRIPTION

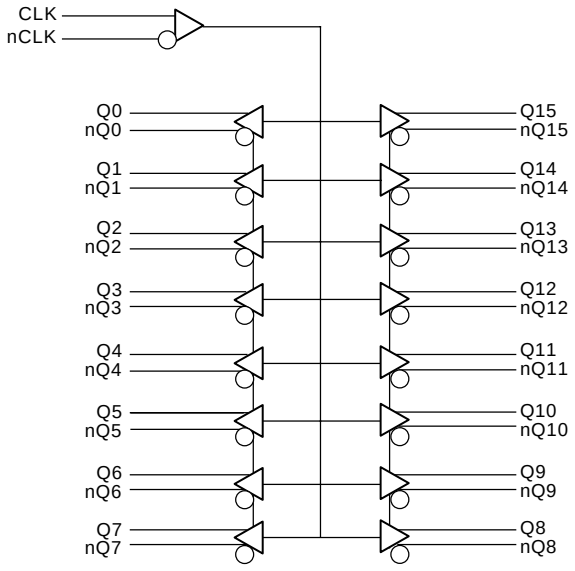
The ICS8520 is a low skew, high performance 1-to-16 Differential-to-3.3V LVHSTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8520 has 1 clock input pair. The CLK, nCLK pair can accept most standard differential input levels.

Guaranteed output skew, part-to-part skew and crossover voltage characteristics make the ICS8520 ideal for interfacing to today's most advanced microprocessor and static RAMs.

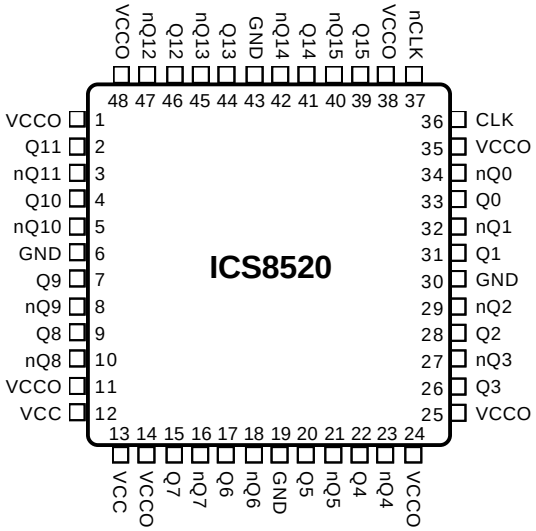
FEATURES

- 16 differential 3.3V LVHSTL outputs each with the ability to drive 50Ω to ground
- 1 differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum output frequency up to 500MHz
- Translates single ended input levels to LVHSTL levels with resistor bias nCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.6ns (maximum)
- VOH: 1.2V (maximum)
- 40% of VOH ≤ Vcrossover ≤ 60% of VOH
- 3.3V core, 1.8V output operating supply voltages
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP
7mm x 7mm x 1.4mm body package
Y Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 11, 14, 24, 25, 35, 38, 48	VCCO	Power		Output supply pins. Connect to 1.8V.
2, 3	Q11, nQ11	Output		Differential output pair. LVHSTL interface levels.
4, 5	Q10, nQ10	Output		Differential output pair. LVHSTL interface levels.
6, 19, 30, 43	VEE	Power		Negative supply pins. Connect to ground.
7, 8	Q9, nQ9	Output		Differential output pair. LVHSTL interface levels.
9, 10	Q8, nQ8	Output		Differential output pair. LVHSTL interface levels.
12, 13	VCC	Power		Positive supply pins. Connect to 3.3V.
15, 16	Q7, nQ7	Output		Differential output pair. LVHSTL interface levels.
17, 18	Q6, nQ6	Output		Differential output pair. LVHSTL interface levels.
20, 21	Q5, nQ5	Output		Differential output pair. LVHSTL interface levels.
22, 23	Q4, nQ4	Output		Differential output pair. LVHSTL interface levels.
26, 27	Q3, nQ3	Output		Differential output pair. LVHSTL interface levels.
28, 29	Q2, nQ2	Output		Differential output pair. LVHSTL interface levels.
36	CLK	Input	Pulldown	Non inverting differential clock input.
37	nCLK	Input	Pullup	Inverting differential clock input.
39, 40	Q15, nQ15	Output		Differential output pair. LVHSTL interface levels.
41, 42	Q14, nQ14	Output		Differential output pair. LVHSTL interface levels.
44, 45	Q13, nQ13	Output		Differential output pair. LVHSTL interface levels.
46, 47	Q12, nQ12	Output		Differential output pair. LVHSTL interface levels.

NOTE: *Pullup* and *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	CLK, nCLK				4	pF
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ

TABLE 3. FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0 thru Q15	nQ0 thru nQ15		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Single ended use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTL levels the recommended input bias network is a resistor to VCC, a resistor of equal value to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is approximately VCC/2 ± 300mV.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VCCx	4.6V
Inputs, V_I	-0.5V to VCC+0.5 V
Outputs, V_O	-0.5V to VCC+0.5V
Package Thermal Impedance, θ_{JA}	46°C/W (no air flow)
Storage Temperature, T_{STG}	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VCC = 3.3V±5%, VCCO = 1.8V±0.2V, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VCC	Positive Supply Voltage		3.135	3.3	3.465	V
VCCO	Output Supply Voltage		1.6	1.8	2.0	V
IEE	Power Supply Current				120	mA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, VCC = 3.3V±5%, VCCO = 1.8V±0.2V, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	CLK	VIN = VCC = 3.465V			150	µA
		nCLK	VIN = VCC = 3.465V			1	µA
IIL	Input Low Current	CLK	VIN = 0V, VCC = 3.465V	-1			µA
		nCLK	VIN = 0V, VCC = 3.465V	-150			µA
VPP	Peak-to-Peak Input Voltage			0.15		1.3	V
VCMR	Common Mode Voltage Range; NOTE 1, 2			VEE + 0.5		VCC - 0.85	V

NOTE 1: Common mode voltage is defined as VIH.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is VCC + 0.3V.

TABLE 4C. LVHSTL DC CHARACTERISTICS, VCC = 3.3V±5%, VCCO = 1.8V±0.2V, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VOH	Output High Voltage; NOTE 1		1.0		1.2	V
VOL	Output Low Voltage; NOTE 1		0		0.4	V
VOX	Output Crossover Voltage		40% x (VOH - VOL) + VOL		60% x (VOH - VOL) + VOL	V

NOTE 1:Outputs terminated with 50Ω to ground.

TABLE 5. AC CHARACTERISTICS, VCC = 3.3V±5%, VCCO = 1.8V±0.2V, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				500	MHz
tPD	Propagation Delay, Low-to-High; NOTE 1	0 < f ≤ 250MHz	1		1.6	ns
tsk(o)	Output Skew; NOTE 2, 4				50	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				250	ps
tR	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
tF	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47		53	%

All parameters measured at 250MHz unless noted otherwise
NOTE 1: Measured from the differential input crossing point to the differential ouput crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

FIGURE 1A, 1B, 1C - INPUT CLOCK WAVEFORMS

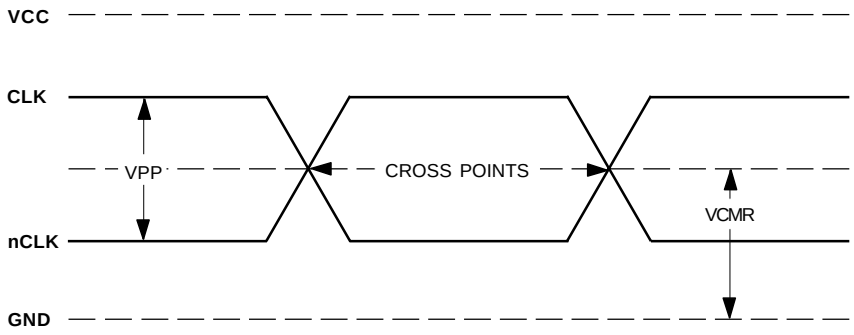


FIGURE 1A - LVDS, HSTL, SSTL DIFFERENTIAL INPUT LEVELS

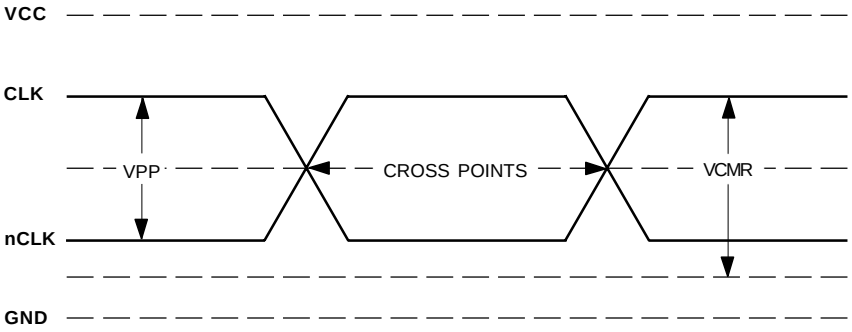


FIGURE 1B - LVPECL DIFFERENTIAL INPUT LEVEL

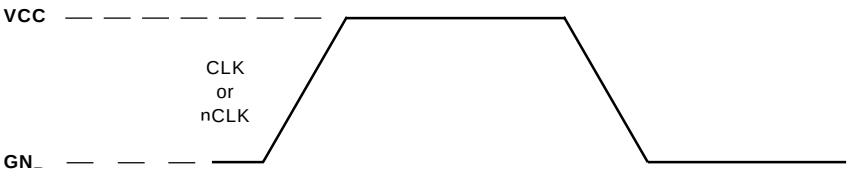


FIGURE 1C- LVCMOS AND LVTTL SINGLE ENDED INPUT LEVEL

PACKAGE OUTLINE - Y SUFFIX

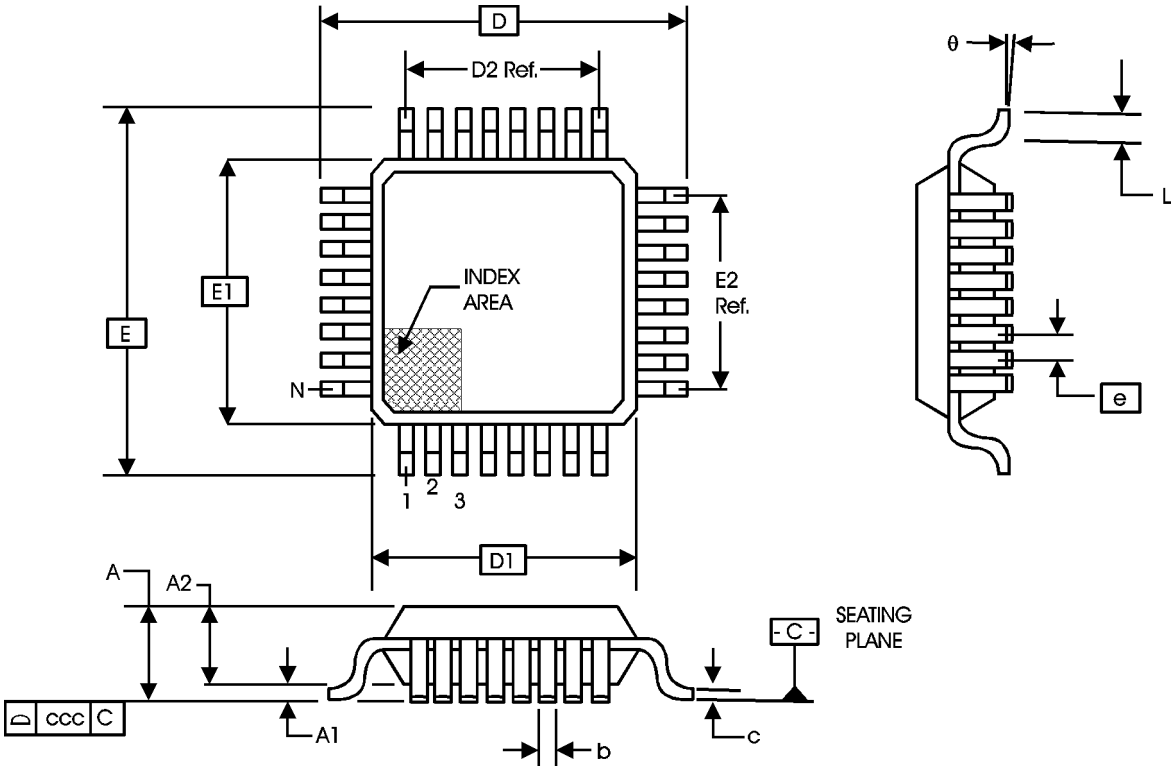


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8520DY	ICS8520DY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8520DYT	ICS8520DY	48 Lead LQFP on Tape and Reel	1000	0°C to 70°C