M66238FP

STANDARD CLOCK GENERATOR WITH PLL FREQUENCY SYNTHESIZER

DESCRIPTION

The M66238 is a LSI that incorporates a PLL synthesizer and a sync clock generator in it. The PLL synthesizer covers the range of 25MHz to 50MHz at the minimum steps of 3kHz. The sync circuit outputs a clock and a one-shot pulse which are synchronized with an external trigger signal. Setting a dividing ratio allows acquisition of sync clock outputs within the range of 0.78MHz to 25MHz.

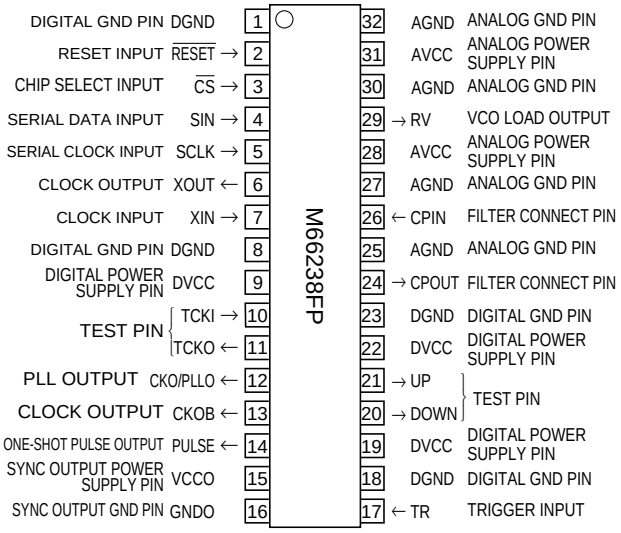
FEATURES

- Sync clock output frequency range: 1/1, 1/2, 1/4, 1/8, 1/16, 1/32 of 25 to 50MHz
- Sync accuracy (jitter): ±3ns
- Trigger input: Polarity selectable
- One-shot pulse output: Polarity and width selectable
- 5V power supply

APPLICATION

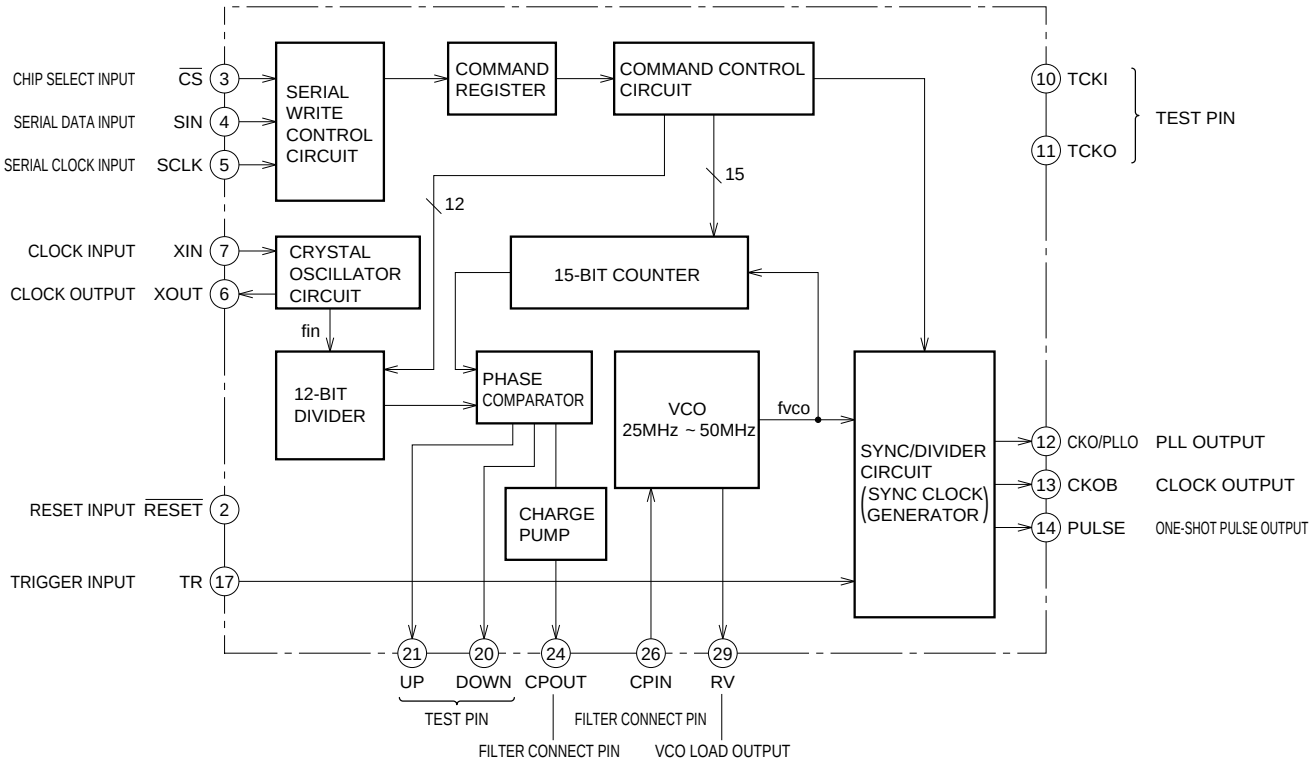
Pixel clock generator

PIN CONFIGURATION (TOP VIEW)



Outline 32P2W-A

BLOCK DIAGRAM



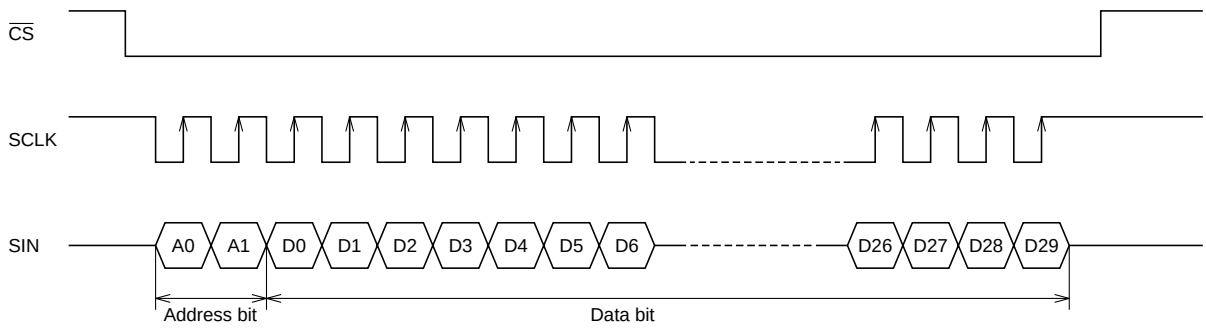
PIN DESCRIPTIONS

Pin name	Name	I/O	Function
$\overline{\text{RESET}}$	Reset input	Input	Initialize M66238 internal status.
$\overline{\text{CS}}$	Chip select input	Input	Transfer serial data when $\overline{\text{CS}}$="L".
SIN	Serial data input	Input	Synchronize 32-bit serial data from MCU with SCK, and enter.
SCLK	Serial clock input	Input	Enter a sync clock for writing 32-bit serial data.
XIN	Clock input	Input	Used by connecting crystal oscillator between XIN and XOUT. When using an external clock signal, connect the clock oscillator to XIN pin and open XOUT pin.
XOUT	Clock output	Output	
TR	Trigger input	Input	Trigger input for clock sync.
CKOB	Clock output	Output	Output an inverted CKO signal.
CKO/PLLO	PLL output	Output	CKO outputs a clock synchronized with a trigger signal and PLLO outputs a PLL oscillator clock as it is.
PULSE	One-shot pulse output	Output	Output a one-shot pulse synchronized with a CKO signal.
CPOUT	Filter connect pin	Output	Connect a low pass filter to charge pump output.
CPIN	Filter connect pin	Input	Low pass filter input pin.
RV	VCO load output	Output	Connect a load resistor for VCO circuit operation between RV and GND.
TCKI	Test pin	Input	Shipping test pin. Connect to GND when use.
TCKO	Test pin	Output	Shipping test pin. Keep open when use.
UP	Test pin	Output	Shipping test pin. Keep open when use.
DOWN	Test pin	Output	Shipping test pin. Keep open when use.
DVCC	Digital power supply pin	—	Digital power supply pin.
DGND	Digital GND pin	—	Digital GND pin.
VCCO	Sync output power supply pin	—	Power supply pin for sync output.
GNDO	Sync output GND pin	—	GND pin for sync output.
AVCC	Analog power supply pin	—	Analog power supply pin.
AGND	Analog GND pin	—	Analog GND pin.

LIST OF REGISTER SETTING COMMANDS

A1	A0	Setting
0	0	Setting of CKO/PLLO dividing ratio, PLL synthesizer 15-bit generation dividing ratio and reference clock generation 12-bit dividing ratio.
1	0	Setting of one-shot pulse polarity and width, setting of trigger edge, HALT of entire M66238, HALT of charge pump and VCO, phase comparator output UP/DOWN, CKO/PLLO switching.
1	1	Dummy trigger generation command

SERIAL DATA WRITE TIMING



REGISTER CONFIGURATION

1. Clock frequency setting command

Reference clock generation 12-bit division ratio, PLL synthesizer 15-bit division ratio and CKO/PLLO division ratio are set at address (A1, A0) = (0, 0).

<table>
<tr><th>Data bit</th><th></th><th>Description</th><th>Default</th></tr>
<tr><td>D0</td><td>0</td><td rowspan="12">12-bit reference clock dividing ratio is set.
D11 and D0 correspond to MSB and LSB, respectively.

$K = \sum_{k=0}^{11} (D_k \times 2^k)$

K: Reference clock dividing ratio</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D1</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D2</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D3</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D4</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D5</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D6</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D7</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D8</td><td>0</td><td rowspan="12">15-bit PLL synthesizer dividing ratio is set.
D26 and D12 correspond to MSB and LSB, respectively.

$N = \sum_{n=12}^{26} (D_n \times 2^{n-12})$

N: PLL synthesizer dividing ratio</td><td>1</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D9</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D10</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D11</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D12</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D13</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D14</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D15</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D16</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D17</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D18</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D19</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D20</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D21</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D22</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D23</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D24</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D25</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D26</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td></tr>
<tr><td>D27</td><td>0</td><td rowspan="6">Setting of CKO/PLLO dividing ratios
<table><tr><th>Dividing ratio</th><th>D29</th><th>D28</th><th>D27</th><th>PLLO/CKO oscillator frequency</th><th>Remarks</th></tr><tr><td>1/1</td><td>0</td><td>0</td><td>0</td><td>25MHz ~ 50MHz</td><td rowspan="6"></td></tr><tr><td>1/2</td><td>0</td><td>0</td><td>1</td><td>12.5MHz ~ 25MHz</td></tr><tr><td>1/4</td><td>0</td><td>1</td><td>0</td><td>6.25MHz ~ 12.5MHz</td></tr><tr><td>1/8</td><td>0</td><td>1</td><td>1</td><td>3.125MHz ~ 6.25MHz</td></tr><tr><td>1/16</td><td>1</td><td>0</td><td>0</td><td>1.563MHz ~ 3.125MHz</td></tr><tr><td>1/32</td><td>1</td><td>0</td><td>1</td><td>0.781MHz ~ 1.563MHz</td></tr></table></td><td>0</td></tr>
<tr><td></td><td>1</td><td>0</td></tr>
<tr><td>D28</td><td>0</td><td>1</td></tr>
<tr><td></td><td>1</td><td></td></tr>
<tr><td>D29</td><td>0</td><td>0</td></tr>
<tr><td></td><td>1</td><td></td></tr>
</table>

2. Operating mode setting commands
Address (A1, A0) = (1, 0) allows setting of one-shot pulse polarity and width, trigger edge, M66238 entire halt, charge pump and VCO halt, phase comparator UP/DOWN output, LPF cutoff, CKO/PLLO switching, VCO switching and charge pump switching.

<table>
<tr><th>Data bit</th><th></th><th>Description</th><th>Default</th></tr>
<tr><td rowspan="2">D0</td><td>0</td><td rowspan="4">Setting of trigger edge<table><tr><th>D1</th><th>D0</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>Synchronizes with TR ↓ CKO is stopped when TR=“H”.</td></tr><tr><td>0</td><td>1</td><td>Synchronizes with TR ↑ CKO is stopped when TR=“L”.</td></tr><tr><td>1</td><td>0</td><td>Synchronizes with TR ↑ CKO is output when TR=“H”.</td></tr><tr><td>1</td><td>1</td><td>Synchronizes with TR ↓ CKO is output when TR=“L”.</td></tr></table></td><td>0</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td rowspan="2">D1</td><td>0</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td rowspan="2">D2</td><td>0</td><td colspan="2">When trigger occurs: spike of sync clock is not eliminated.</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">When trigger occurs: spike of sync clock is eliminated (disabled when D1=1).</td></tr>
<tr><td rowspan="2">D3</td><td>0</td><td colspan="2">Polarity of one-shot pulse: Negative pulse</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Polarity of one-shot pulse: Positive pulse</td></tr>
<tr><td rowspan="2">D4</td><td>0</td><td rowspan="4">Setting of one-shot pulse width<table><tr><th>D5</th><th>D4</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>CKO 2-cycle width</td></tr><tr><td>0</td><td>1</td><td>CKO 4-cycle width</td></tr><tr><td>1</td><td>0</td><td>CKO 8-cycle width</td></tr><tr><td>1</td><td>1</td><td>CKO 16-cycle width</td></tr></table></td><td>0</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td rowspan="2">D5</td><td>0</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td>0</td></tr>
<tr><td rowspan="2">D6</td><td>0</td><td colspan="2">CKO/PLLO pin: CKO output</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">CKO/PLLO pin: PLLO output</td></tr>
<tr><td rowspan="2">D7</td><td>0</td><td colspan="2">Entire M66238: Operating state</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Entire M66238: Halt state</td></tr>
<tr><td rowspan="2">D8</td><td>0</td><td colspan="2">VCO: Operating state</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">VCO: Halt state</td></tr>
<tr><td rowspan="2">D9</td><td>0</td><td colspan="2">Charge pump: ON</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Charge pump: OFF</td></tr>
<tr><td rowspan="2">D10</td><td>0</td><td colspan="2">Low pass filter: Operating state</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Low pass filter: Separated</td></tr>
<tr><td rowspan="2">D11</td><td>0</td><td colspan="2">Normal use: Not output to outside</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Phase comparator UP/DOWN output enable</td></tr>
<tr><td rowspan="2">D12</td><td>0</td><td colspan="2">Normal use</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">VCO test circuit set</td></tr>
<tr><td rowspan="2">D13</td><td>0</td><td colspan="2">Normal use</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Charge pump test circuit set</td></tr>
<tr><td rowspan="2">D14</td><td>0</td><td colspan="2">Normal use</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">15-bit counter test clock enable</td></tr>
<tr><td rowspan="2">D15</td><td>0</td><td colspan="2">Normal use</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Sync clock generator test clock enable</td></tr>
<tr><td rowspan="2">D16</td><td>0</td><td colspan="2">Normal use</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Sync clock generator test input enable</td></tr>
<tr><td rowspan="2">D17</td><td>0</td><td colspan="2">Normal use</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">12-bit counter test output enable</td></tr>
<tr><td rowspan="2">D18</td><td>0</td><td colspan="2">Normal use</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">15-bit counter test output enable</td></tr>
<tr><td rowspan="2">D19</td><td>0</td><td colspan="2">Normal use</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Sync clock generator trigger test output enable</td></tr>
<tr><td rowspan="2">D20</td><td>0</td><td colspan="2">Normal use</td><td rowspan="2">0</td></tr>
<tr><td>1</td><td colspan="2">Sync clock generator test output enable</td></tr>
<tr><td>D21
⋮
D29</td><td></td><td colspan="2">In normal use: “0” set</td><td>0
⋮
0</td></tr>
</table>

3. Dummy trigger generating command

The internal status of sync clock generator becomes unstable and a stable sync clock output (CKO) is not obtained after the power is turned on, after a reset is cleared or after an internal VCO oscillator frequency is set. To obtain a stable sync clock output, enter a trigger signal from the TR input after VCO oscillator becomes stable, or enter a dummy trigger generating command from the MCU. The PLL synthesizer oscillator frequency after the cancellation of a reset depends on a default (See the register configuration).

Set the command for address (A1, A0) = (1, 1).

Data bit		Description	Default
D0	0	The command must be stored two times continuously when a dummy trigger is generated. For the first time, set the dummy trigger generating command with D0=1. For the second time, set the dummy trigger generating command with D0=0. The second setting becomes a sync edge and a clock begins to be output from CKO. After the first setting, CKO is in the halt state.	0
	1		
D1	0	In normal use: “0”	0
	1		
⋮	⋮		⋮
D29	0		0
	1		

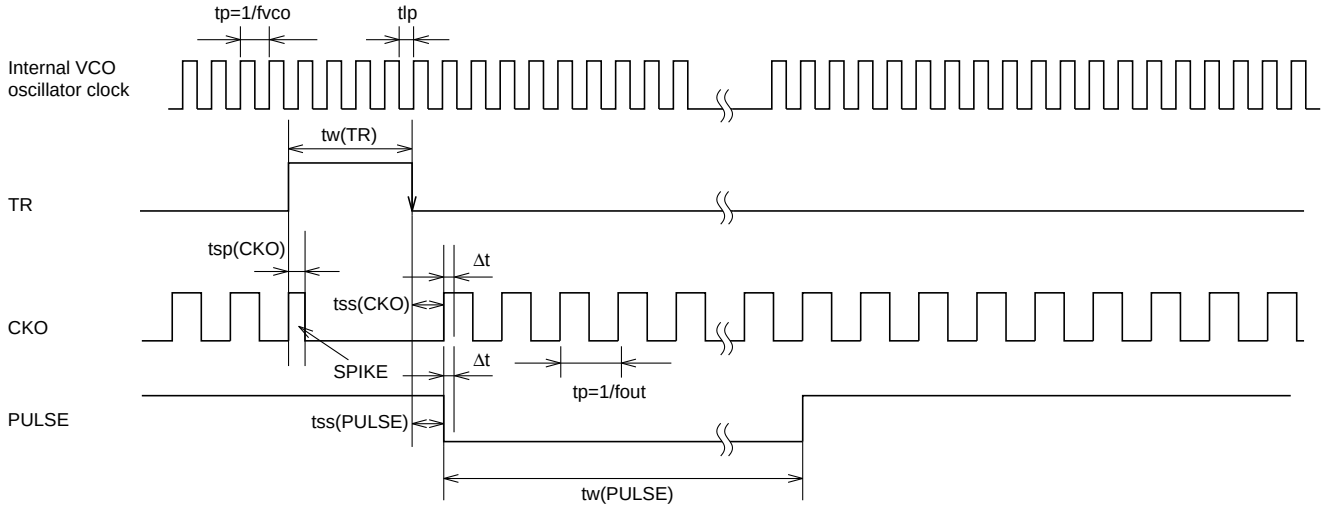
OPERATING TIMING

1. Sync clock spike non-removal mode upon occurrence of trigger

1-1 Setting of trigger edge when D1=0

One-shot pulse start timing: 1st leading edge of CKO after TR fall
One-shot pulse polarity: Negative pulse
One-shot pulse width: 16 cycles of CKO

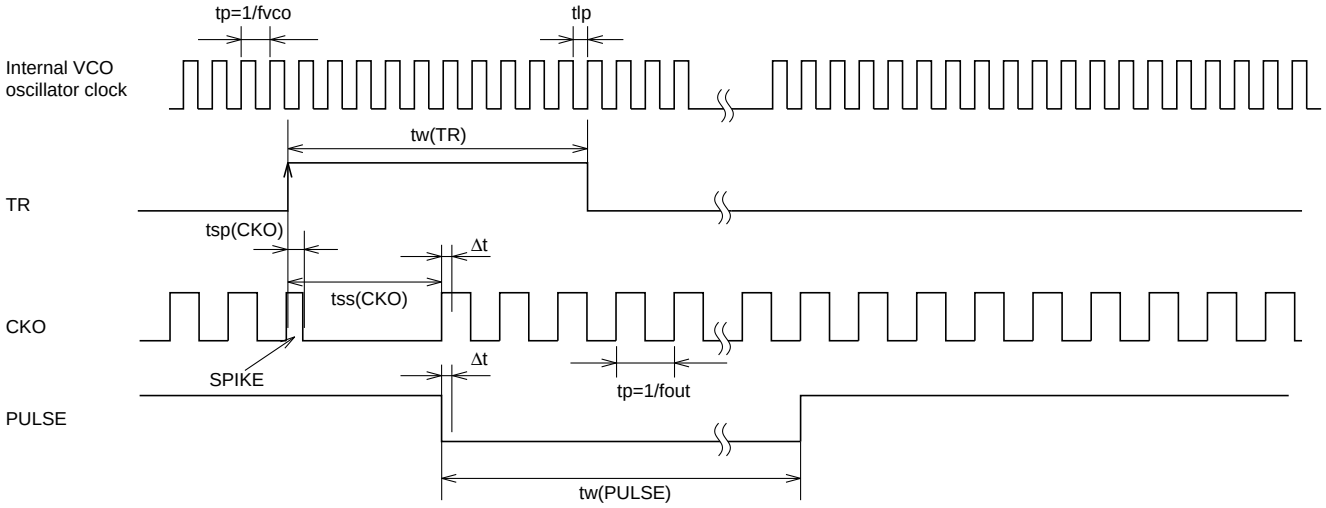
CKO output dividing ratio: 1/2 division
An example set for the condition of address (A1, A0)=(1, 0), data (D6, D5, D4, D3, D2, D1, D0)=(0, 1, 1, 0, 0, 0, 0) is shown below. CKO is a clock output synchronized by TR and PULSE is a one-shot pulse synchronized with the rise of CKO.



1-2 Setting of trigger edge when D1=1

One-shot pulse start timing: 1st leading edge of CKO after TR rise (except the rise of a spike which occurs when CKO is stopped).
One-shot pulse polarity: Negative pulse
One-shot pulse width: 16 cycles of CKO

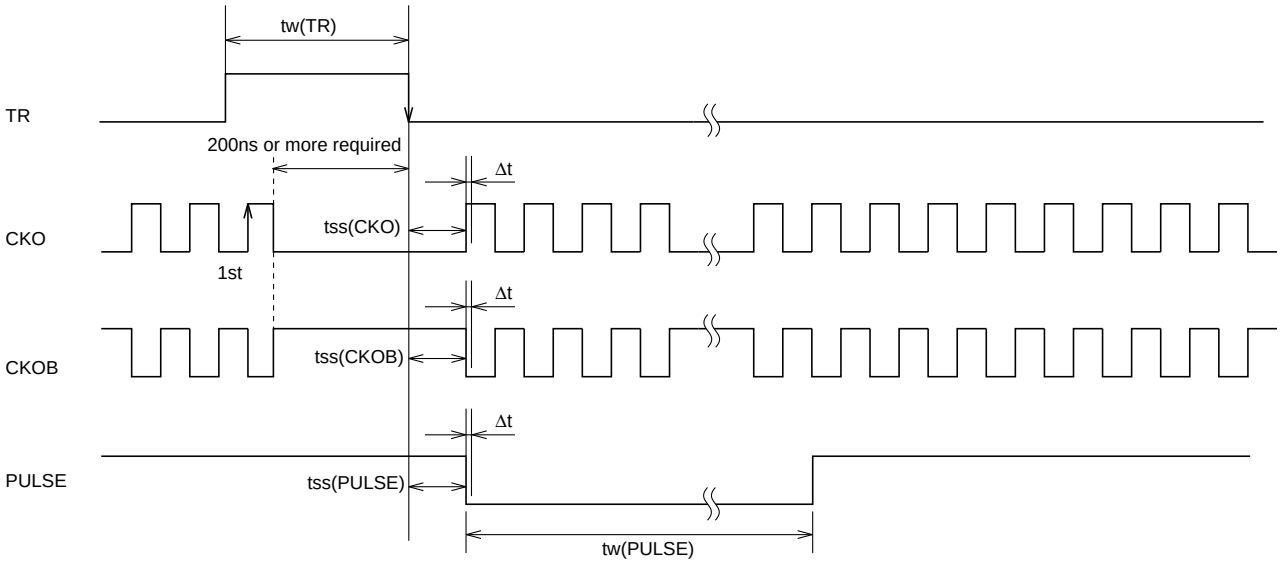
CKO output dividing ratio: 1/2 division
An example set for the condition of address (A1, A0)=(1, 0), data (D6, D5, D4, D3, D2, D1, D0)=(0, 1, 1, 0, 0, 1, 0) is shown below. CKO is a clock output synchronized by TR and PULSE is a one-shot pulse synchronized with the rise of CKO.



2. Sync clock spike removal mode upon occurrence of trigger

When address (A1, A0)=(1, 0) and data (D6, D5, D4, D3, D2, D1, D0)=(0, 1, 1, 0, 1, 0, 0), CKO with the first rise after occurrence of a trigger is output and then CKO stops.

However, this mode is not available when D1=1 in trigger edge setting. Set a wide TR so that TR sync edge is entered 200ns or more after CKO stops.



1) 200ns or more required

2) Note: tss (CKO, CKOB, PULSE) is defined by input clock width "L" + α. In addition, the value of α denotes IC internal delay, and the values of α and tss are definite unless temperature, Vcc, etc. are changed, and tss variations at that time is defined as Δt (sync accuracy: jitter).

CKO/PLLO output frequency range

The M66238 requires an internal VCO oscillator frequency of 25MHz to 50MHz.

Settings of dividing ratio K of 12-bit divider and dividing ratio N of 15-bit counter are required in order to determine the internal VCO oscillator frequency. The relation between the settings and the internal VCO oscillator frequency is shown below.

Oscillator frequency $f_{VCO} = \frac{fin \times N}{K}$ (MHz)

$$K = \sum_{k=0}^{11} (D_k \times 2^k)$$

$$N = \sum_{n=12}^{26} (D_n \times 2^{n-12})$$

3) Note: Setting of fin/K≥100kHz is recommended in consideration of the frequency accuracy characteristics of PLL output.

Therefore, set the division ratio K of the 12 bit divider and the division ratio N of the 15 bit counter to meet the following conditions:

25MHz≤fvco≤50MHz

In addition, for PLLO and CKO, setting the division ratios of the sync/division circuit (synchronous clock generating area) to 1/1, 1/2, 1/4, 1/8, 1/16, 1/32 will allow the frequencies of 0.78Hz - 50MHz to be accommodated.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		–0.5 ~ +7.0	V
Vi	Input voltage		–0.5 ~ Vcc + 0.5	V
Vo	Output voltage		–0.5 ~ Vcc + 0.5	V
Pd	Power dissipation	When board is mounted	650	mW
Tstg	Storage temperature		–65 ~ 150	°C

Remarks: All voltages adopt the GND pin of the circuit as the base (0V) and absolute values are displayed for maximum and minimum values.

RECOMMENDED OPERATING CONDITIONS (Ta=0 to 70°C)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vcc	Supply voltage	4.75	5	5.25	V
GND	Supply voltage		0		V
Vi	Input voltage	0		Vcc	V
Vo	Output voltage	0		Vcc	V
Topr	Operating ambient temperature	0		70	°C

Remarks: The direction of current flowing into a circuit is defined to be positive (no sign) and the direction of current flowing out is defined to be negative (– sign). Absolute values are displayed for maximum and minimum values.

ELECTRICAL CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±5%, GND=0V)

Symbol	Parameter	Conditions	Limits			Unit	Measurement circuit
			Min.	Typ.	Max.		
VIH	High-level input voltage	TR	2			V	(Note)
VIL	Low-level input voltage				0.8	V	
VIH	High-level input voltage	XIN	0.8×Vcc			V	
VIL	Low-level input voltage				0.2×Vcc	V	
VOH	High-level output voltage	GND=0V, IOH=–4mA	Vcc–0.8			V	
VOL	Low-level output voltage	GND=0V, IOL=4mA			0.55	V	
ICC(S)	Supply current (at time of standstill)	GND=0V, Vl=Vcc or GND			50	μA	
ICC(a)	Supply current (at time of operation)	GND=0V, CKO=50MHz Vl=Vcc or GND			120	mA	
IIH	High-level input current	GND=0V, VI=Vcc			10	μA	
IIL	Low-level input current	GND=0V, VI=0V			–10	μA	
CI	Input capacitance				10	pF	

Remarks: The direction of current flowing to the circuit is specified to be positive (no sign).

TIMING REQUIREMENTS (Ta=0 to 70°C, Vcc=5V±5%, GND=0V)

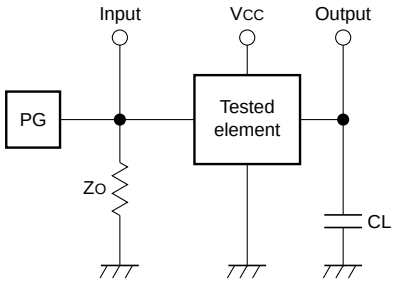
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
tw($\overline{CS}$)	CS width		1			µs
tsu($\overline{CS}$-SCK)	CS set up time		50			ns
th(SCK-$\overline{CS}$)	CS hold time		50			ns
tw(SCK)	SCK width		25			ns
tsu(SIN-SCK)	SIN set up time		25			ns
th(SCK-SIN)	SIN hold time		25			ns
fin	Clock input frequency		7		12	MHz
fiDUTY	Clock input duty		40		60	%
tw(TR)	Trigger input "H" pulse width		200			ns
tr	Clock input rising time				5	ns
tf	Clock input falling time				5	ns

SWITCHING CHARACTERISTICS (Ta=0 to 70°C, Vcc=5V±5%, GND=0V)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
fvco	VCO oscillation frequency	CL=15pF	25		50	MHz
fout	Synchronous output frequency				50	MHz
Δt	Synchronous accuracy (jitter)				±3	ns
tss(CKO)	Synchronous clock output start				tlp+200	ns
tss(CKOB)	Synchronous clock reversible output start				tlp+200	ns
tss(PULSE)	One-shot pulse output start				tlp+200	ns
tsp(CKO)	Synchronous clock output stop				40	ns
tsp(CKOB)	Synchronous clock reversible output stop				40	ns
tw(PULSE)	One-shot pulse output width		n • tp–10		n • tp+10	ns
f_{oDUTY}(CKO)	Synchronous clock output duty		40		60	%
f_{oDUT}(CKOB)	Synchronous clock reversible output duty		40		60	%

(Notes)
• tp=1/fout, tlp=tp × (100 – fvcoduty)/100
• The n value of one-shot pulse output width is set in the register.

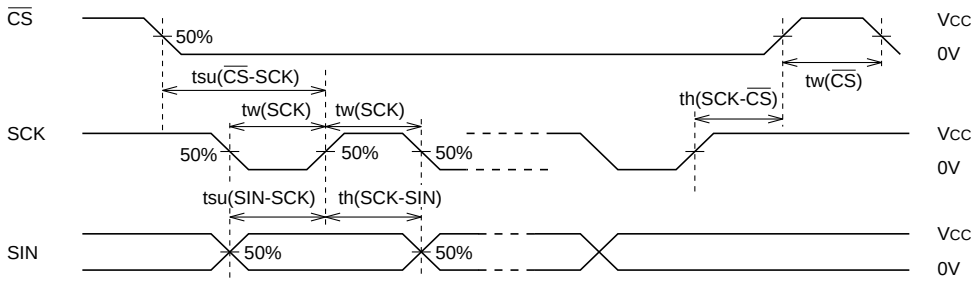
MEASUREMENT CIRCUIT



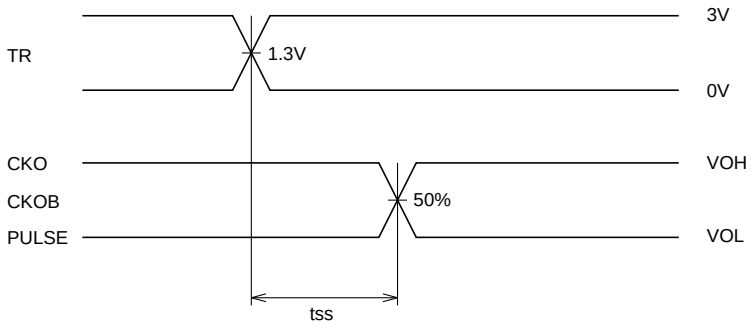
• Waveform for switching test
  Input pulse level XIN: 0 to Vcc, TR: 0 to 3V
  Input pulse rising time: 3 ns
  Input pulse falling time: 3 ns
  Zo: 50Ω
  Decision voltage Input voltage XIN: Vcc/2, Tr: 1.3V
  Output voltage All outputs: Vcc/2
• Electrostatic capacitance: CL includes floating capacitance of connection and probe input capacitance.

INPUT TIMING

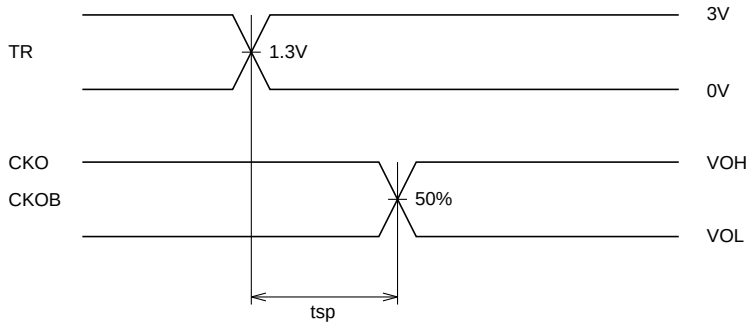
(1) Register setting



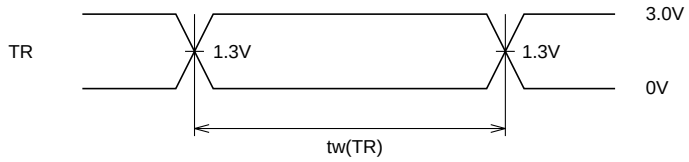
(2) Clock from trigger input and one-shot pulse output



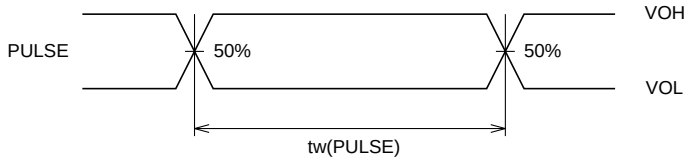
(3) Stop of clock from trigger input



(4) Trigger input width



(5) One-shot pulse width



APPLICATION CIRCUIT EXAMPLE