MX29F016

16M-BIT [2M X 8] CMOS EQUAL SECTOR FLASH MEMORY

FEATURES

- Single power supply 5V operation for read, erase and program
- Fast access time: 70/90/120ns
- Low power consumption
  - 30mA maximum active current
  - 0.2uA typical standby current
- Command register architecture
  - Byte Programming (7us typical)
  - Sector Erase:32 equal sector with of 64KByte each
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors with Erase Suspend capability.
  - Automatically program and verify data at specified address
- Erase suspend/Erase Resume
  - Suspends an erase operation to read data from, or program data to, another sector that is not being erased, then resumes the erase.
- Status Reply
  - Data polling & Toggle bit for detection of program and erase cycle completion.
- Group Sector protect/unprotect for 5V/12V system.
- Group Sector protection
  - Hardware sector protect/unprotect method for each group which consists of two adjacent sectors
  - Temporary group sector unprotect allows code changes in previously locked sectors
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1V to VCC+1V
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 40-pin TSOP, 44-pin SOP, 48-pin TSOP
- Compatibility with JEDEC standard
  - Pinout and software compatible with single-power supply Flash

GENERAL DESCRIPTION

The MX29F016 is a 16-mega bit Flash memory organized as 2M bytes of 8 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F016 is packaged in 40-pin TSOP or 44-pin SOP, 48-pin TSOP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The standard MX29F016 offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F016 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

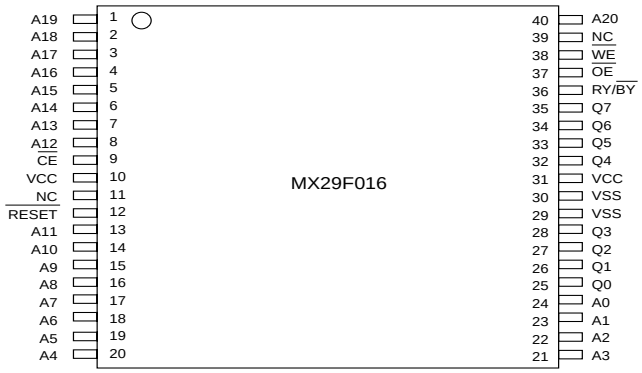
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F016 uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F016 uses a 5.0V±10% VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

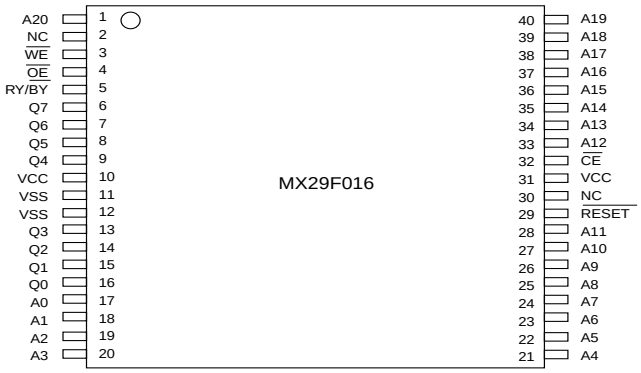
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATIONS

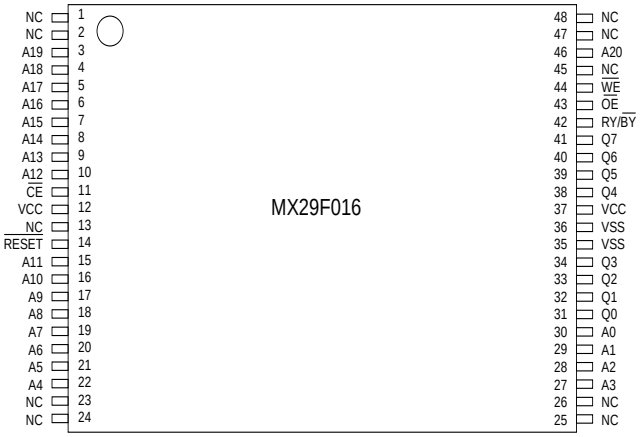
40 TSOP (Standard Type) (10mm x 20mm)



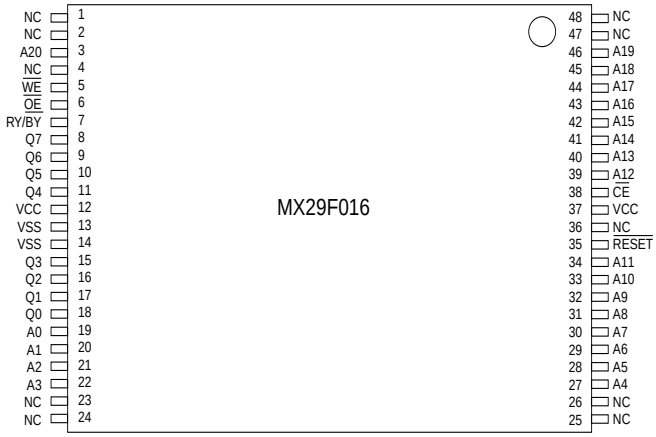
40 TSOP (Reverse Type) (10mm x 20mm)



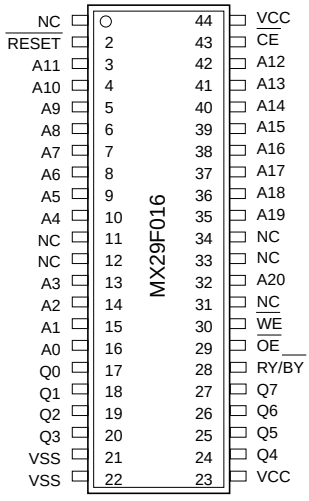
48 TSOP (Standard Type) (12mm x 20mm)



48 TSOP (Reverse Type) (12mm x 20mm)



44 SOP



PIN DESCRIPTION

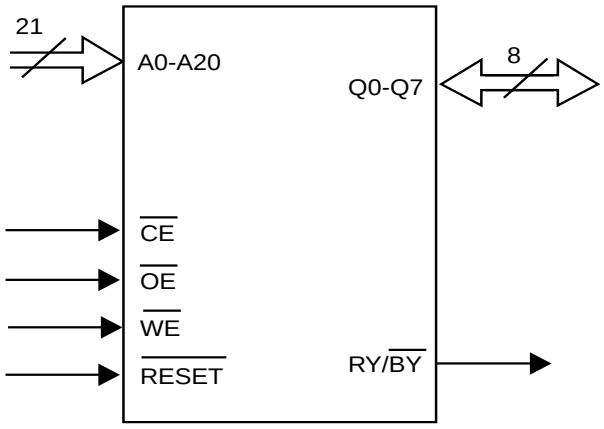
SYMBOL	PIN NAME
A0~A20	Address Input
Q0~Q7	8 Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{RESET}$	Hardware Reset Pin, Active Low
RY/$\overline{BY}$	Read/Busy Output
VCC	+5.0V single power supply
VSS	Device Ground
NC	Pin Not Connected Internally

MX29F016 SECTOR ADDRESS TABLE

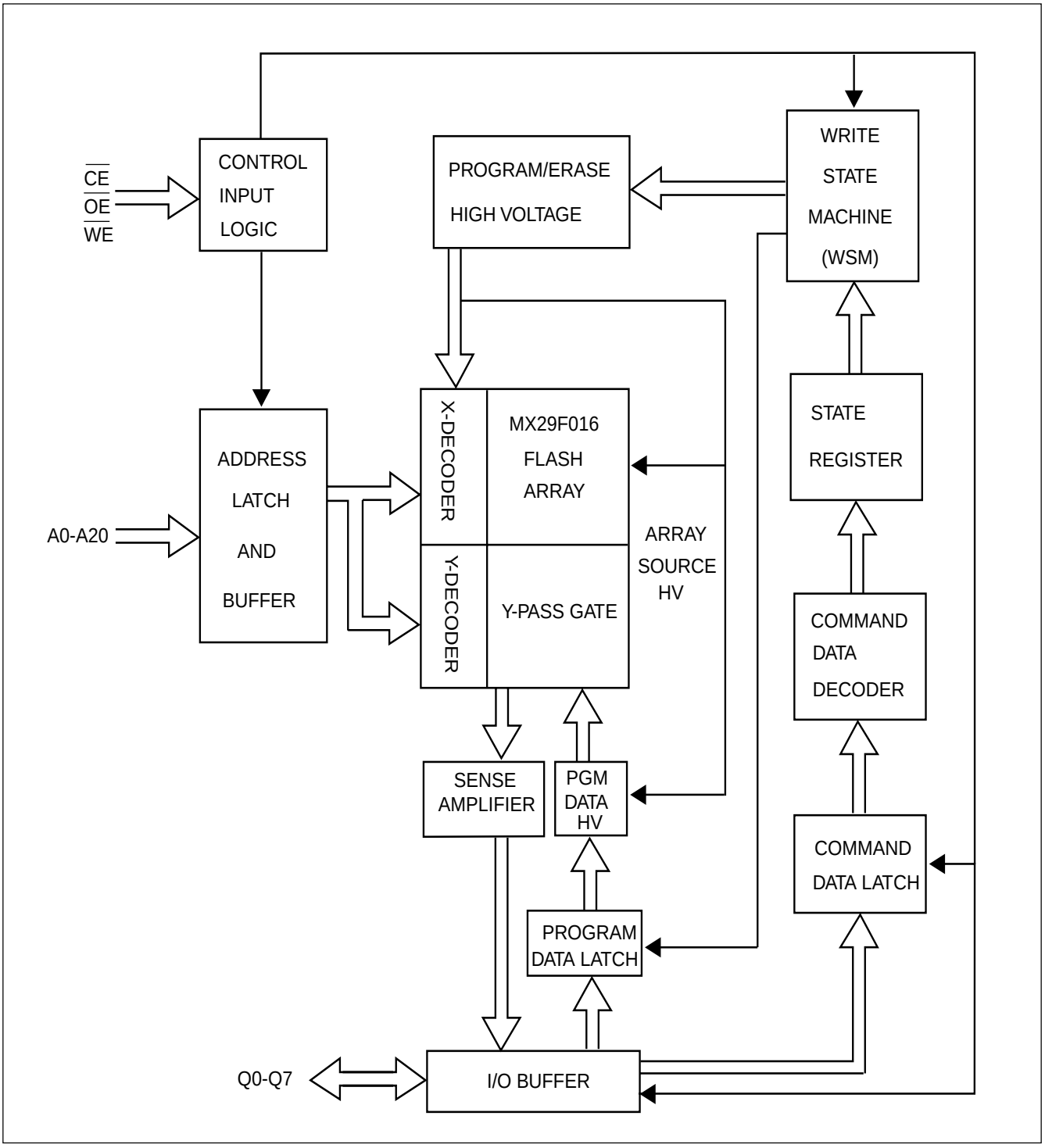
Group Sector	Sector	A20	A19	A18	A17	A16	Address Range
SGA0	SA0	0	0	0	0	0	000000h-00FFFFh
SGA0	SA1	0	0	0	0	1	010000h-01FFFFh
SGA0	SA2	0	0	0	1	0	020000h-02FFFFh
SGA0	SA3	0	0	0	1	1	030000h-03FFFFh
SGA1	SA4	0	0	1	0	0	040000h-04FFFFh
SGA1	SA5	0	0	1	0	1	050000h-05FFFFh
SGA1	SA6	0	0	1	1	0	060000h-06FFFFh
SGA1	SA7	0	0	1	1	1	070000h-07FFFFh
SGA2	SA8	0	1	0	0	0	080000h-08FFFFh
SGA2	SA9	0	1	0	0	1	090000h-09FFFFh
SGA2	SA10	0	1	0	1	0	0A0000h-0AFFFFh
SGA2	SA11	0	1	0	1	1	0B0000h-0BFFFFh
SGA3	SA12	0	1	1	0	0	0C0000h-0CFFFFh
SGA3	SA13	0	1	1	0	1	0D0000h-0DFFFFh
SGA3	SA14	0	1	1	1	0	0E0000h-0EFFFFh
SGA3	SA15	0	1	1	1	1	0F0000h-0FFFFFh
SGA4	SA16	1	0	0	0	0	100000h-10FFFFh
SGA4	SA17	1	0	0	0	1	110000h-11FFFFh
SGA4	SA18	1	0	0	1	0	120000h-12FFFFh
SGA4	SA19	1	0	0	1	1	130000h-13FFFFh
SGA5	SA20	1	0	1	0	0	140000h-14FFFFh
SGA5	SA21	1	0	1	0	1	150000h-15FFFFh
SGA5	SA22	1	0	1	1	0	160000h-16FFFFh
SGA5	SA23	1	0	1	1	1	170000h-17FFFFh
SGA6	SA24	1	1	0	0	0	180000h-18FFFFh
SGA6	SA25	1	1	0	0	1	190000h-19FFFFh
SGA6	SA26	1	1	0	1	0	1A0000h-1AFFFFh
SGA6	SA27	1	1	0	1	1	1B0000h-1BFFFFh
SGA7	SA28	1	1	1	0	0	1C0000h-1CFFFFh
SGA7	SA29	1	1	1	0	1	1D0000h-1DFFFFh
SGA7	SA30	1	1	1	1	0	1E0000h-1EFFFFh
SGA7	SA31	1	1	1	1	1	1F0000h-1FFFFFh

Legend:SA=Sector Address ; SGA=Sector Group Address
Note:All sectors are 64 Kbytes in size.

LOGIC SYMBOL



BLOCK DIAGRAM



AUTOMATIC PROGRAMMING

The MX29F016 is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed. The typical chip programming time at room temperature of the MX29F016 is less than 14 seconds.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 10 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. Typical erasure at room temperature is accomplished in less than 19 seconds. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29F016 is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm require the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to $\overline{\text{DATA}}$ polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of $\overline{\text{WE}}$.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F016 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

TABLE1. SOFTWARE COMMAND DEFINITIONS

Command	Bus Cycle	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXXH	F0H										
Read	1	RA	RD										
Read Silicon ID	4	555H	AAH	2AAH	55H	555H	90H	ADI	DDI				
Sector Group Protect Verify	4	555H	AAH	2AAH	55H	555H	90H	SGA X02H	00H 01H				
Porgram	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector Erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector Erase Suspend	1	XXXH	B0H										
Sector Erase Resume	1	XXXH	30H										

Note:
1. ADI = Address of Device identifier; A1=0, A0 = 0 for manufacture code,A1=0, A0 = 1 for device code.
   (Refer to Table 3)
   DDI = Data of Device identifier : C2H for manufacture code, ADH for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
2.PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address of the sector to be erased.
   SGA = Address of the Sector Group Address bits A18-A20 select a uniqul sector group.
3.The system should generate the following address patterns: 555H or 2AAH to Address A10~A0 .
  Address bit A11~A20=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequence may be initiated with A11~A20 in either state.
4.For Sector Group Protect Verify Operation : If read out data is 01H, it means the sector has been protected.If read out data is 00H,it means the sector is still not being protected.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 1 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device(when applicable).

TABLE 2. MX29F016 BUS OPERATION

Mode	Pins							
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	Q0 ~ Q7
Read Silicon ID Manfacturer Code(1)	L	L	H	L	L	X	V_{ID}(2)	C2H
Read Silicon ID Device Code(1)	L	L	H	H	L	X	V_{ID}(2)	ADH
Read	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D_{IN}(3)
Sector Protect with 12V system(6)	L	V_{ID}(2)	L	X	X	L	V_{ID}(2)	X
Chip Unprotect with 12V system(6)	L	V_{ID}(2)	L	X	X	H	V_{ID}(2)	X
Verify Sector Group Protect with 12V system	L	L	H	X	H	X	V_{ID}(2)	Code(5)
Reset	X	X	X	X	X	X	X	HIGH Z

NOTES:
1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 13V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H means unprotected.
   Code=01H means protected.
   A20~A18=Sector Group address for protect.
6. Refer to sector protect/unprotect algorithm and waveform.

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F016 contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL,A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of ADH for MX29F016.

SET-UP AUTOMATIC CHIP/SECTOR ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verification command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

TABLE 3. SILICON ID CODE

Pins	A0	A1	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Code(Hex)
Manufacture code	VIL	VIL	1	1	0	0	0	0	1	0	C2H
Device code for MX29F016	VIH	VIL	1	1	0	1	0	1	0	1	ADH

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of $\overline{WE}$, while the command(data) is latched on the rising edge of $\overline{WE}$. Sector addresses selected are loaded into internal register on the sixth falling edge of $\overline{WE}$. Each successive sector load cycle started by the falling edge of $\overline{WE}$ must begin within 80ms from the rising edge of the preceding $\overline{WE}$. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

Table 4. Write Operation Status

	Status		**Q7**	**Q6**	**Q5**	**Q3**	**Q2**
In Progress	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	0	0	1
	Auto Erase Algorithm		0	Toggle	0	1	Toggle
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle (Note1)
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{Q7}$	Toggle (Note2)	0	0	1 (Note3)
Exceeded Time Limits	Byte Program in Auto Program Algorithm		$\overline{Q7}$	Toggle	1	0	1
	Program/Erase in Auto Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{Q7}$	Toggle	1	0	N/A

Notes:
1.Performing successive read operations from the erase-suspended sector will cause Q2 to toggle.
2.Performing successive read operations from any address will cause Q6 to toggle.
3.Reading the byte address being programmed while in the erase-suspend program mode will indicate logic "1" at the Q2 bit. However, successive reads from the erase-suspended sector will cause Q2 to toggle.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and program commands.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended blocks.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions.Another Erase Suspend command can be written after the chip has resumed erasing.

SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, A three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on therising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program opetation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode(no program verify command is required).

$\overline{\text{DATA}}$ POLLING-Q7

The MX29F016 also features $\overline{Data}$ Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The $\overline{Data}$ Polling feature is valid after the rising edge of the fourth $\overline{WE}$ pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1". The $\overline{Data}$ Polling feature is valid after the rising edge of the sixth $\overline{WE}$ pulse of six write pulse sequences for automatic chip/sector erase.

The $\overline{Data}$ Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out.(see section Q3 Sector Erase Timer)

Q6:Toggle BIT I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence(prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 4 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively eraseing (that is, the Automatic Erase alorithm is in process), or whether that sector is erase-suspended. Toggle Bit I is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 4 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfuly completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5
Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits(internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector maynot be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

DATA PROTECTION

The MX29F016 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

Q3
Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

SECTOR PROTECTION WITH 12V SYSTEM

The MX29F016 features hardware group sector protection. This feature will disable both program and erase operations for these group sector protected. To activate this mode, the programming equipment must force VID on address pin A9 and control pin $\overline{OE}$, (suggest VID = 12V) A6 = VIL and $\overline{CE}$ = VIL.(see Table 2) Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated on the rising edge. Please refer to group sector protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with $\overline{CE}$ and $\overline{OE}$ at VIL and $\overline{WE}$ at VIH). When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses, except for A1, are don't care. Address locations with A1 = VIL are reserved to read manufacturer and device codes.(Read Silicon ID)

It is also possible to determine if the group is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT WITH 12V SYSTEM

The MX29F016 also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin $\overline{OE}$ and address pin A9. The $\overline{CE}$ pins must be set at VIL. Pins A6 must be set to VIH.(see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated on the rising edge.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs(Q0-Q7) for an unprotected sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

POWER-UP SEQUENCE

The MX29F016 powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

CAPACITANCE (TA = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			8	pF	VIN = 0V
COUT	Output Capacitance			12	pF	VOUT = 0V

READ OPERATION

DC CHARACTERISTICS (TA = 0°C TO 70°C, VCC = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ILI	Input Leakage Current			1	uA	VIN = GND to VCC
ILO	Output Leakage Current			± 1	uA	VOUT = GND to VCC
ISB1	Standby VCC current			1	mA	CE = VIH
ISB2			0.2	5	uA	CE = VCC + 0.3V
ICC1	Operating VCC current			30	mA	IOUT = 0mA, f=1MHz
ICC2				50	mA	IOUT = 0mA, f=10MHz
VIL	Input Low Voltage	-0.3(NOTE 1)		0.8	V	
VIH	Input High Voltage	2.0		VCC + 0.3	V	
VOL	Output Low Voltage			0.45	V	IOL = 2.1mA
VOH	Output High Voltage	2.4			V	IOH = -2mA

NOTES:

1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns
   If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS (TA = 0°C to 70°C, VCC = 5V±10%*)

		29F016-70*		29F016-90		29F016-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		70		90		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		70		90		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		40		40		50	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Float (Note1)	0	20	0	30	0	30	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL

TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V*
- Input rise and fall times is equal to or less than 20ns
- Output load: 1 TTL gate + 100pF *(Including scope and jig)
- Reference levels for measuring timing*: 0.8V, 2.0V

NOTE:

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

* For -70 pats :
  - the input pulse levels : 0.0V/3.0V
  - the output load: 1 TTL gate +30pF(Including scope and jig)
  - reference level for measuring timing:1.5V
  - Vcc=5V± 5%

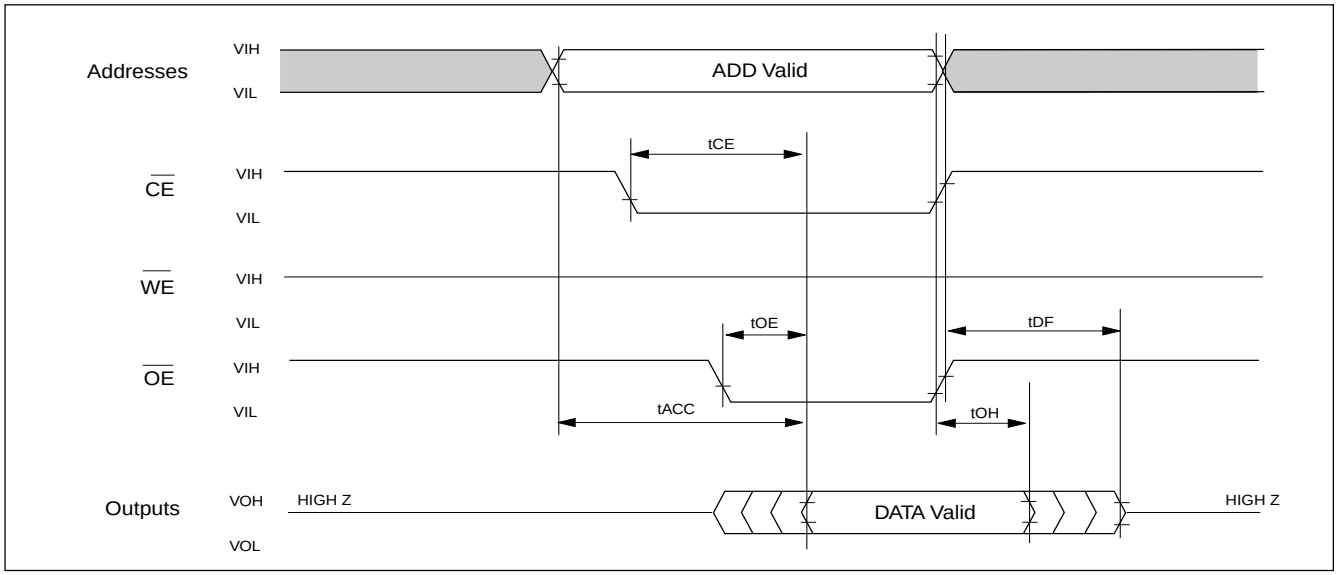
ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to 7.0V
VCC to Ground Potential	-0.5V to 7.0V
A9 & $\overline{OE}$	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

READ TIMING WAVEFORMS



COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

DC CHARACTERISTICS (TA = 0°C to 70°C, VCC = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
ICC1 (Read)	Operating VCC Current			30	mA	IOUT=0mA, f=1MHz
ICC2				50	mA	IOUT=0mA, F=10MHz
ICC3 (Program)				50	mA	In Programming
ICC4 (Erase)				50	mA	In Erase
ICCES	VCC Erase Suspend Current		2		mA	$\overline{CE}$=VIH, Erase Suspended

NOTES:

1. VIL min. = -0.6V for pulse width is equal to or less than 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.

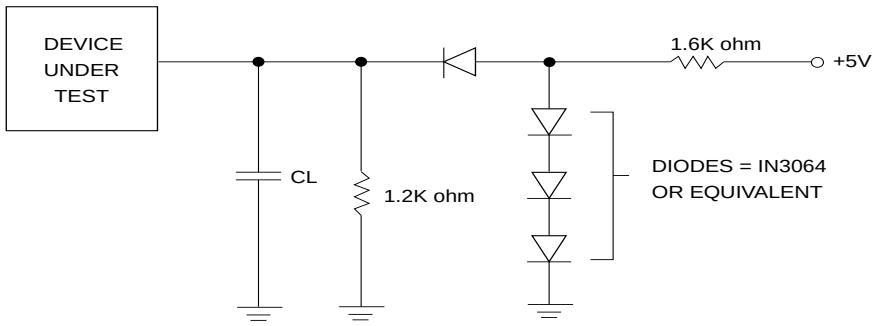
AC CHARACTERISTICS TA = 0°C to 70°C, VCC = 5V ± 10%

		29F016-70		29F016-90		29F016-12			
SYMBOL	PARAMETER	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tOES	$\overline{OE}$ setup time	50		50		50		ns	
tCWC	Command programming cycle	70		90		120		ns	
tCEP	$\overline{WE}$ programming pulse width	35		45		50		ns	
tCEPH1	$\overline{WE}$ programming pluse width High	20		20		20		ns	
tCEPH2	$\overline{WE}$ programming pluse width High	20		20		20		ns	
tAS	Address setup time	0		0		0		ns	
tAH	Address hold time	45		45		50		ns	
tDS	Data setup time	30		45		50		ns	
tDH	Data hold time	0		0		0		ns	
tCESC	$\overline{CE}$ setup time before command write	0		0		0		ns	
tDF	Output disable time (Note 1)		30		40		40	ns	
tAETC	Total erase time in auto chip erase	19(TYP.)		19(TYP.)		19(TYP.)		s	
tAETB	Total erase time in auto block erase	1(TYP.)		1(TYP.)		1(TYP.)		s	
tAVT	Total programming time in auto verify	7		7		7		us	
tBAL	Block address load time	80		80		80		us	
tCH	$\overline{CE}$ Hold Time	0		0		0		ns	
tCS	$\overline{CE}$ setup to WE going low	0		0		0		ns	
tVLHT	Voltge Transition Time	4		4		4		us	
tOESP	$\overline{OE}$ Setup Time to $\overline{WE}$ Active	4		4		4		us	
tWPP1	Write pulse width for sector protect	10		10		10		us	
tWPP2	Write pulse width for sector unprotect	12		12		12		ms	

NOTES:

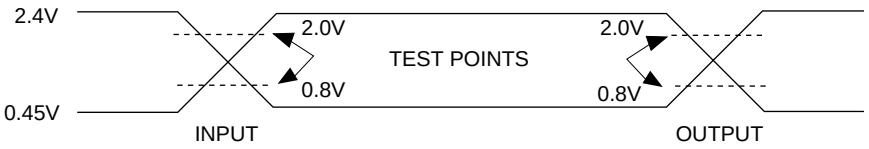
1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

SWITCHING TEST CIRCUITS



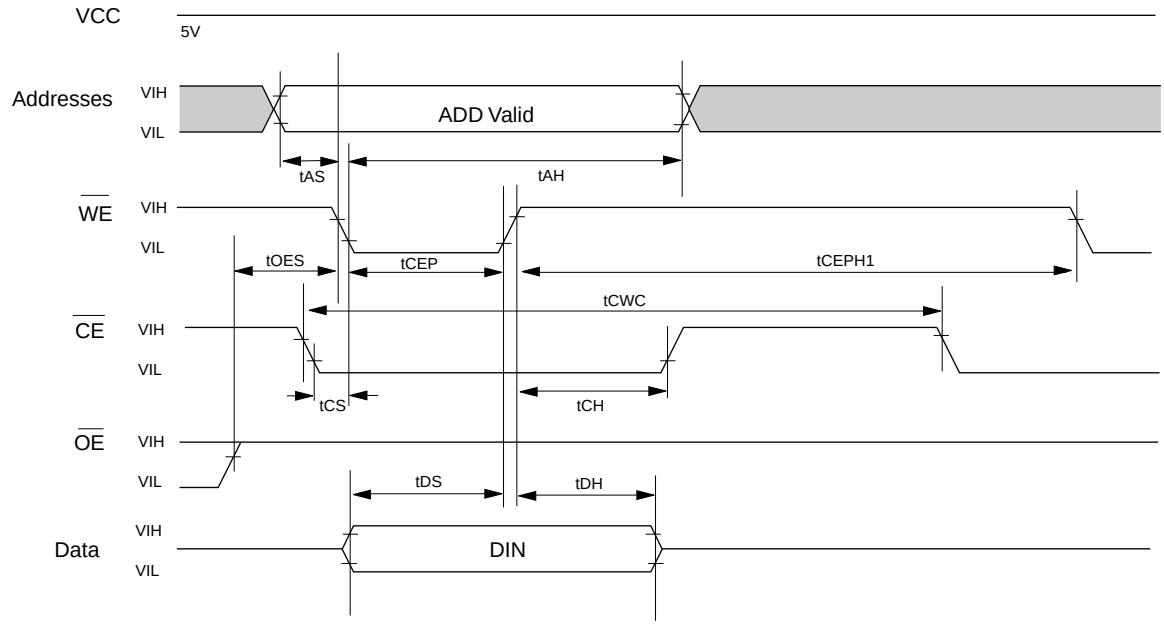
CL = 30 pF including jig capacitance for 70 grade
CL=100pF for others

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are <20ns.

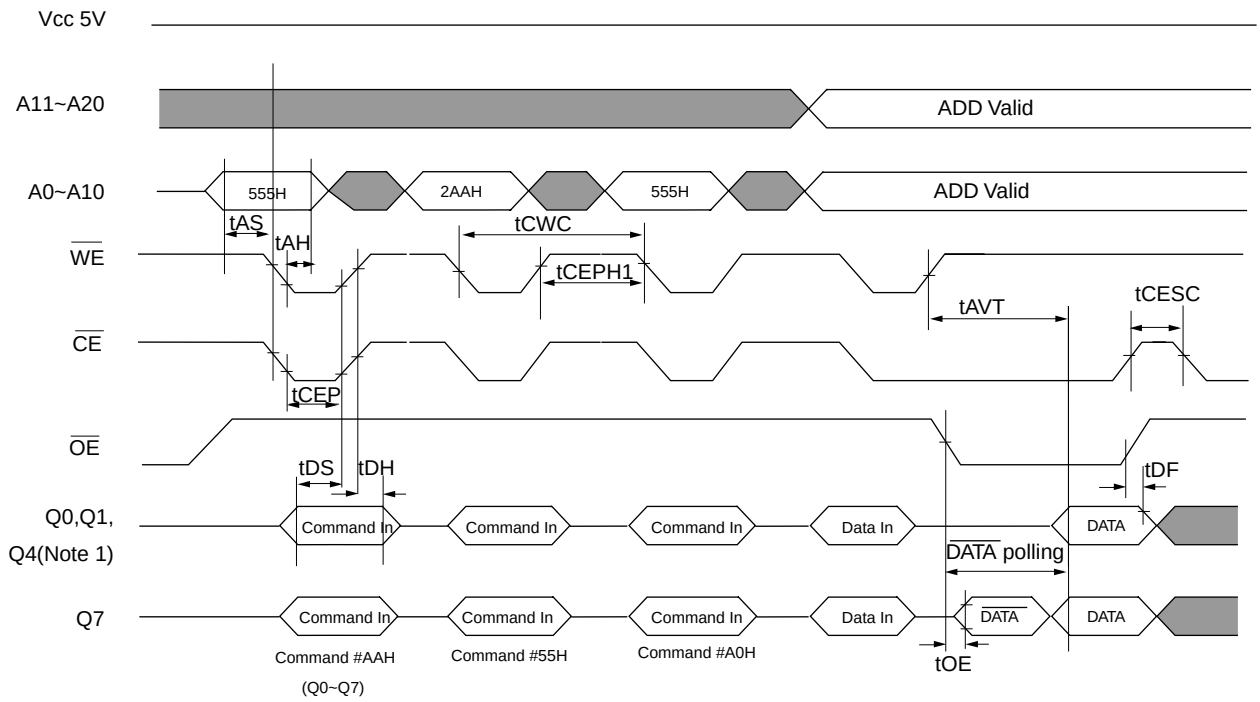
COMMAND WRITE TIMING WAVEFORM



AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic verification starts. Device outputs $\overline{DATA}$ during programming and $\overline{DATA}$ after programming on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

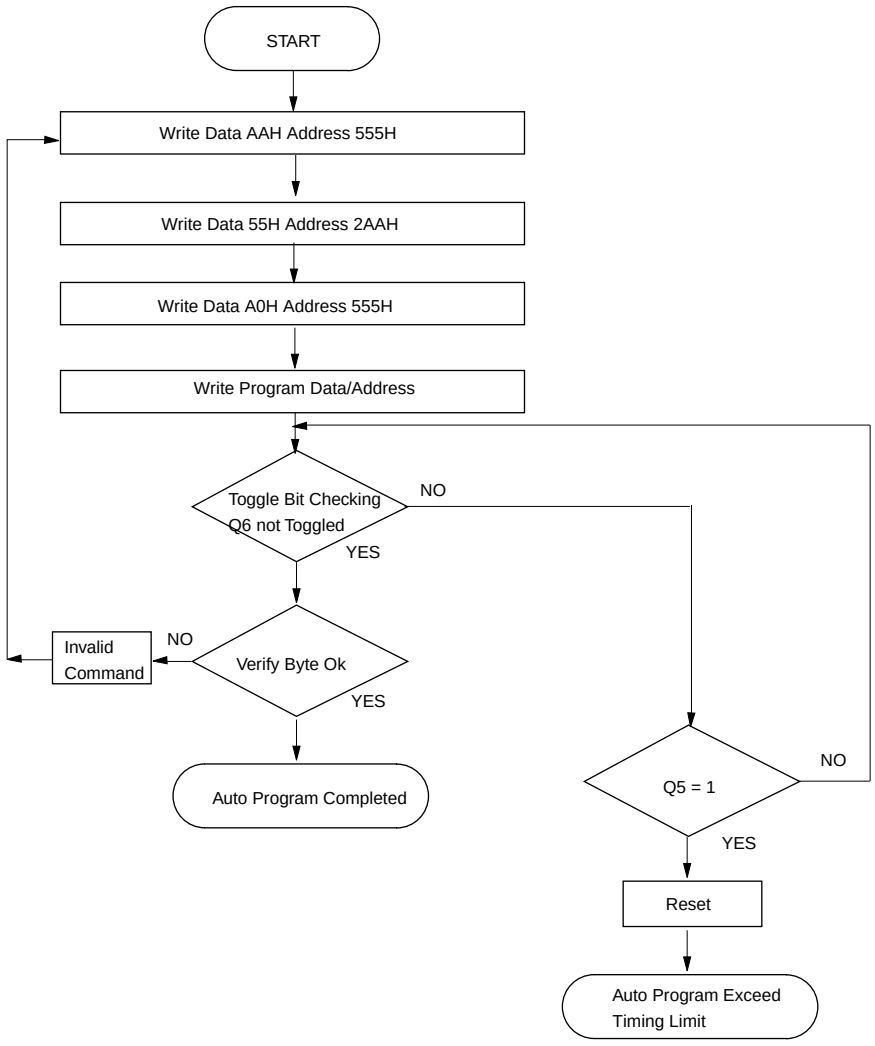
AUTOMATIC PROGRAMMING TIMING WAVEFORM



Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

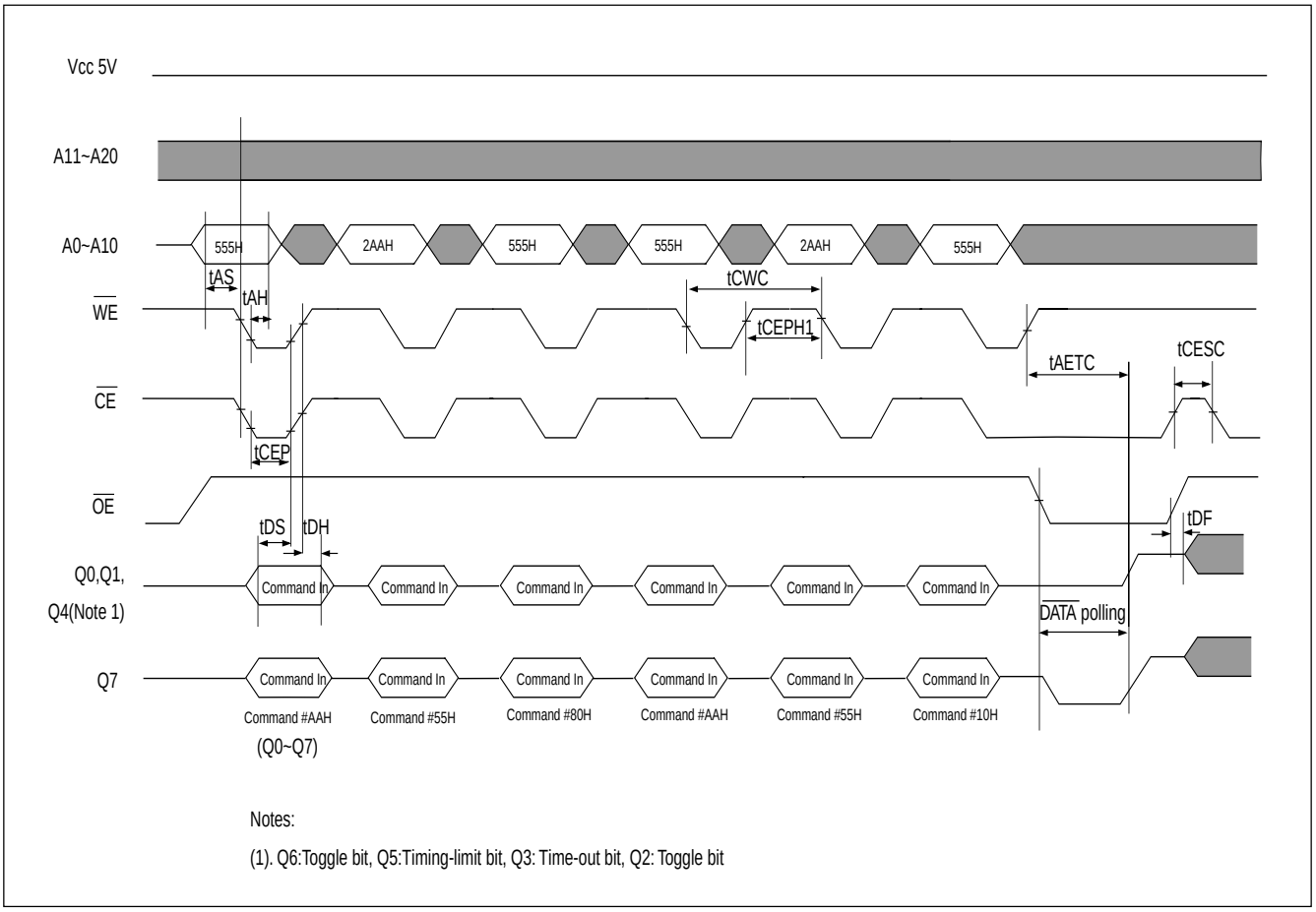
AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



AUTOMATIC CHIP ERASE TIMING WAVEFORM

All data in chip are erased. External erase verification is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

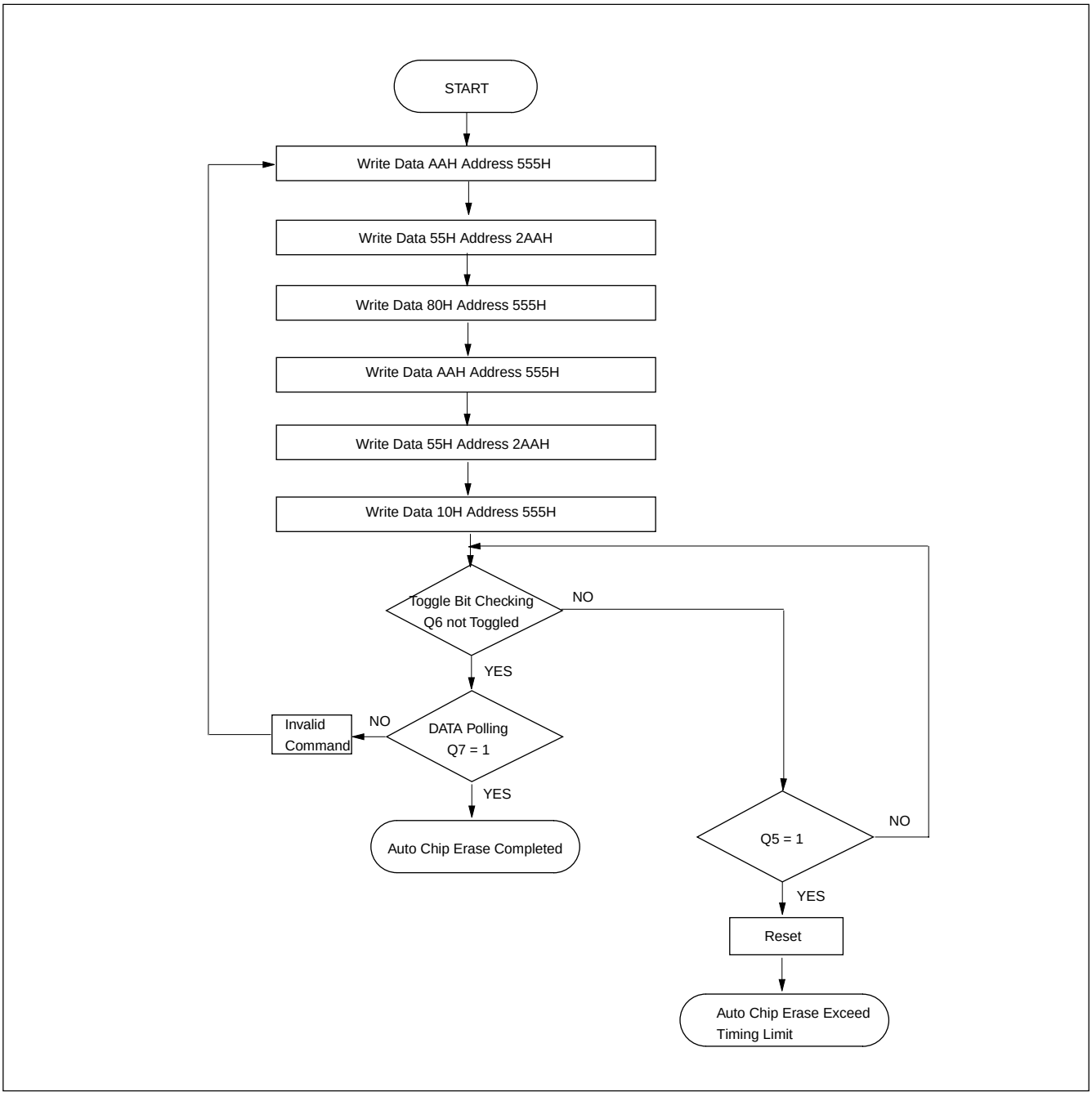
AUTOMATIC CHIP ERASE TIMING WAVEFORM



Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

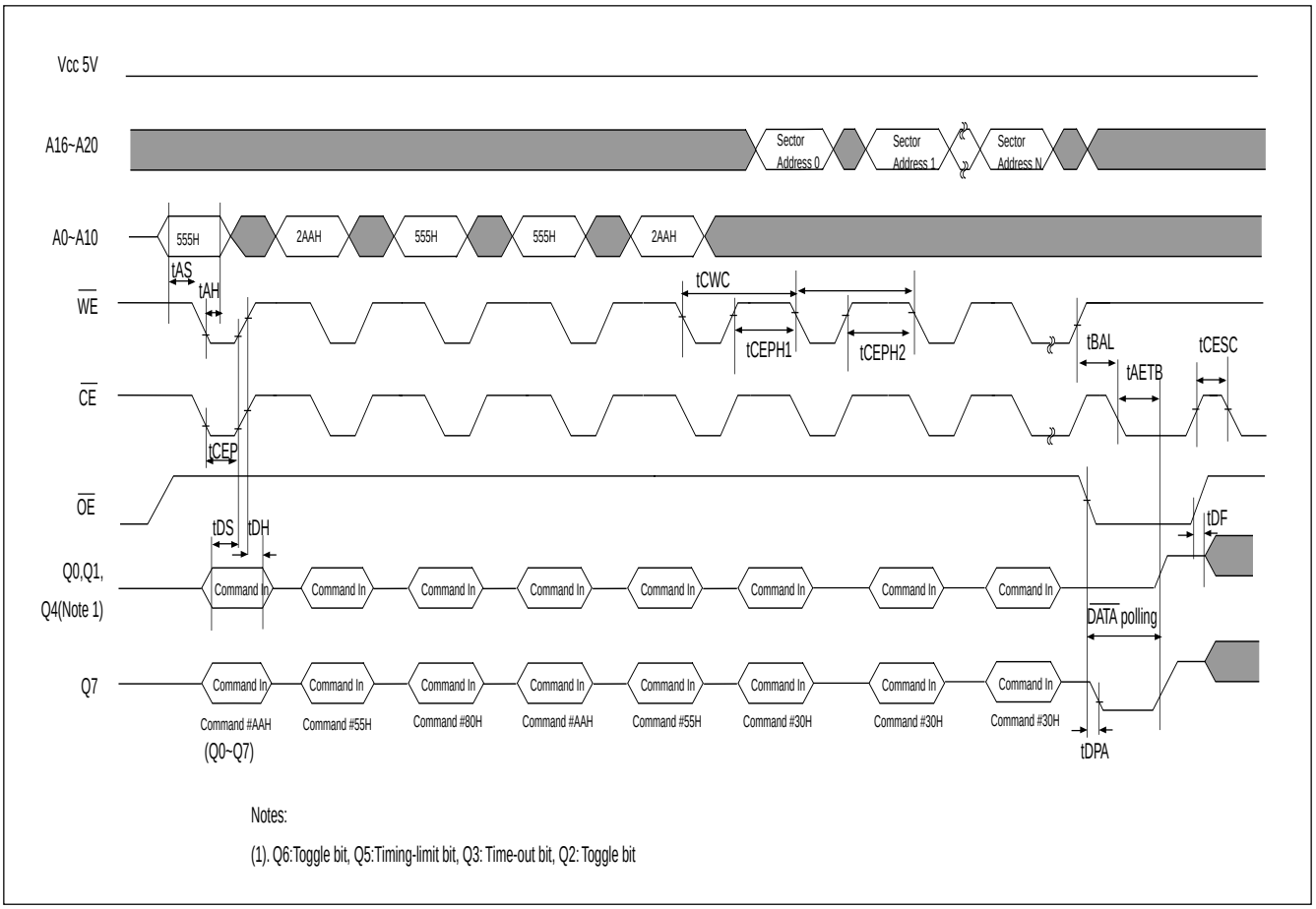
AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART



AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Block data indicated by A16 to A20 are erased. External erase verify is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by $\overline{\text{DATA}}$ polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{\text{DATA}}$ polling, timing waveform)

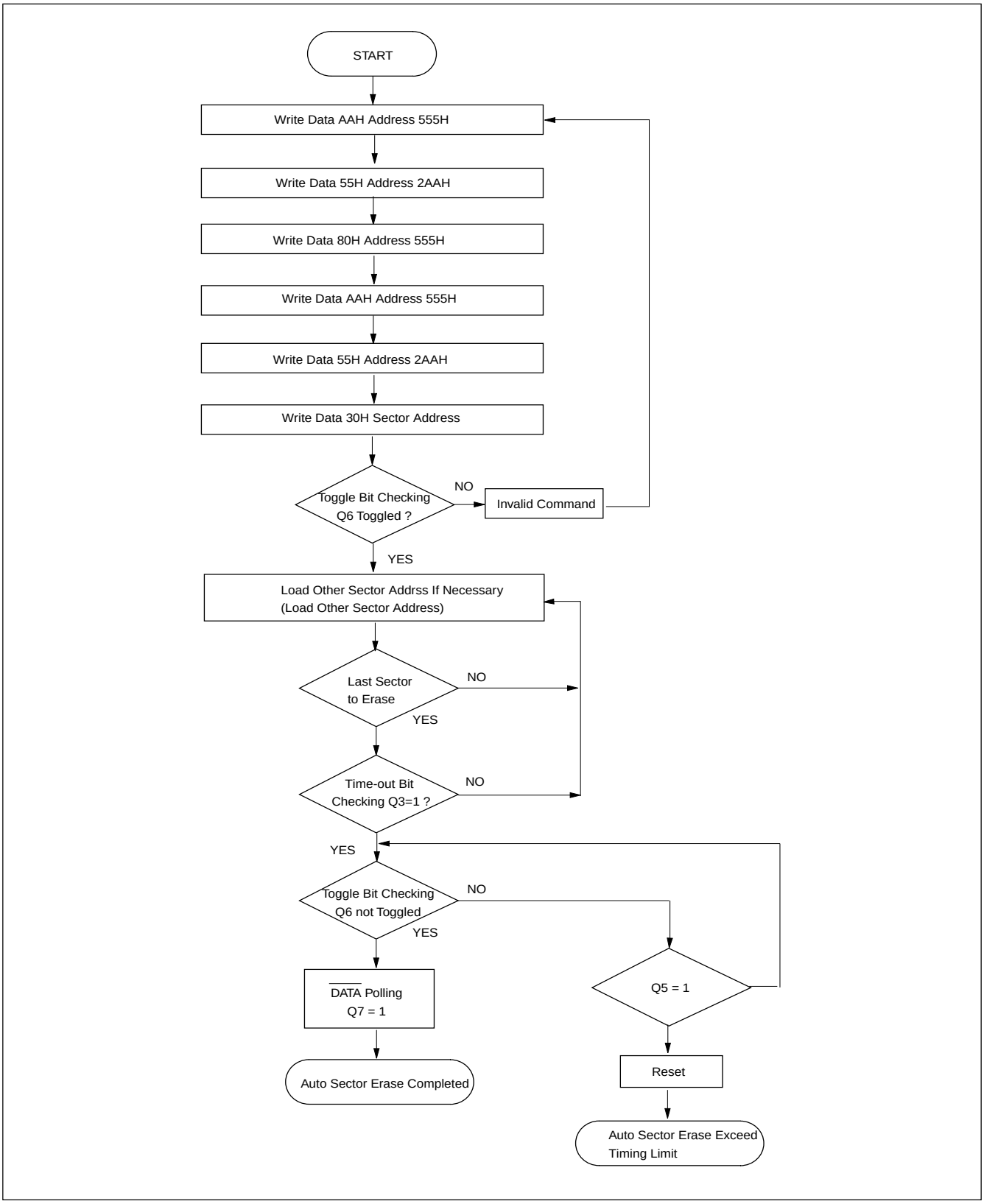
AUTOMATIC SECTOR ERASE TIMING WAVEFORM



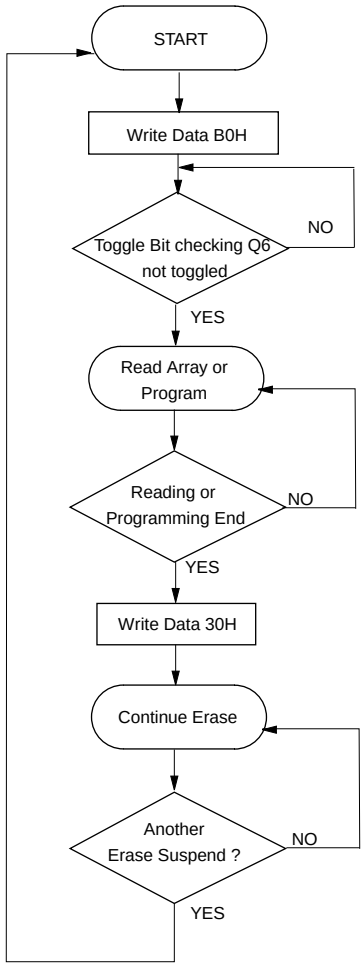
Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

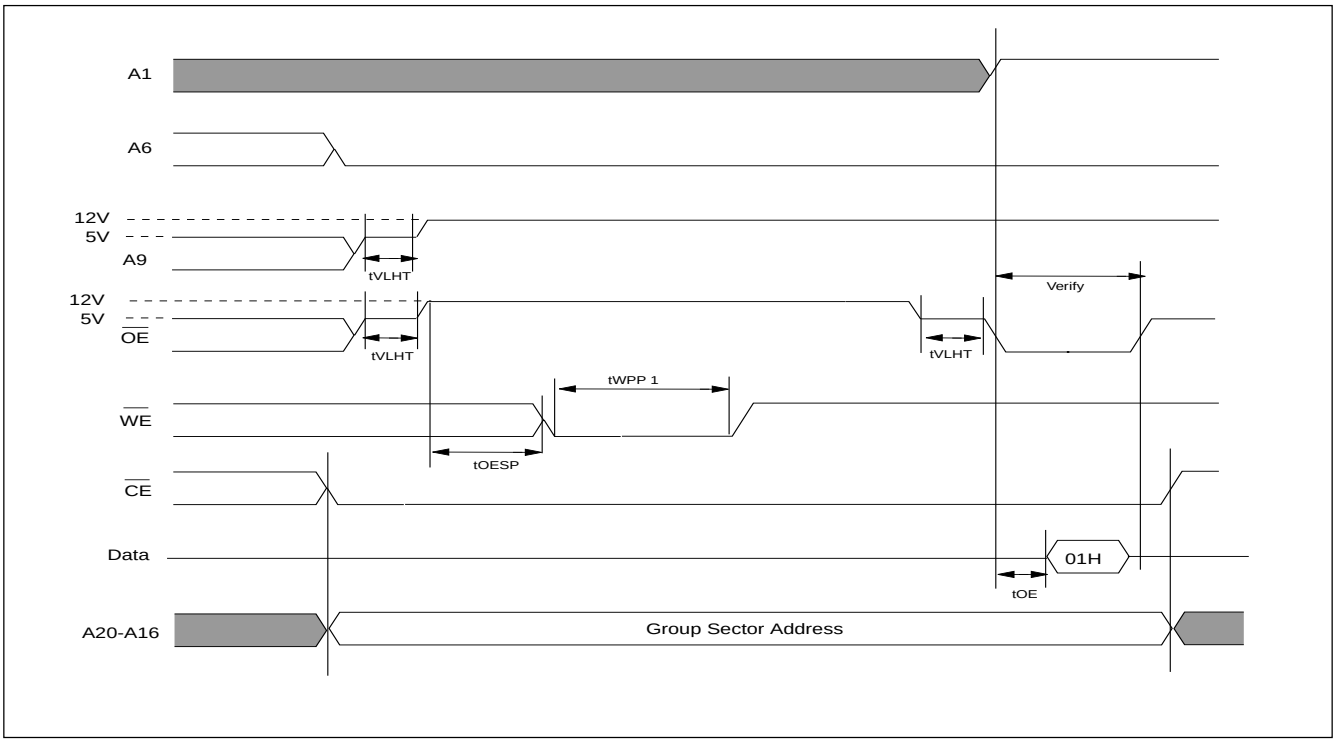
AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART



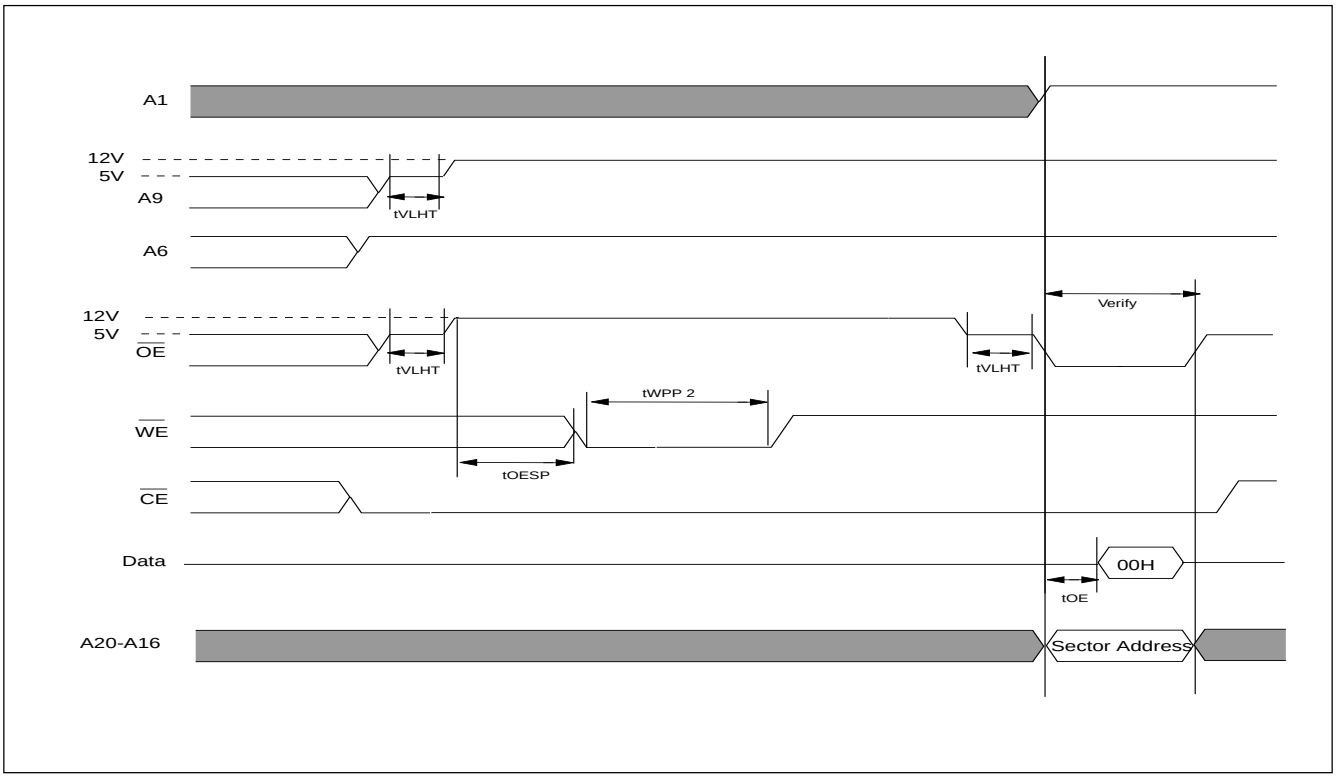
ERASE SUSPEND/ERASE RESUME FLOWCHART



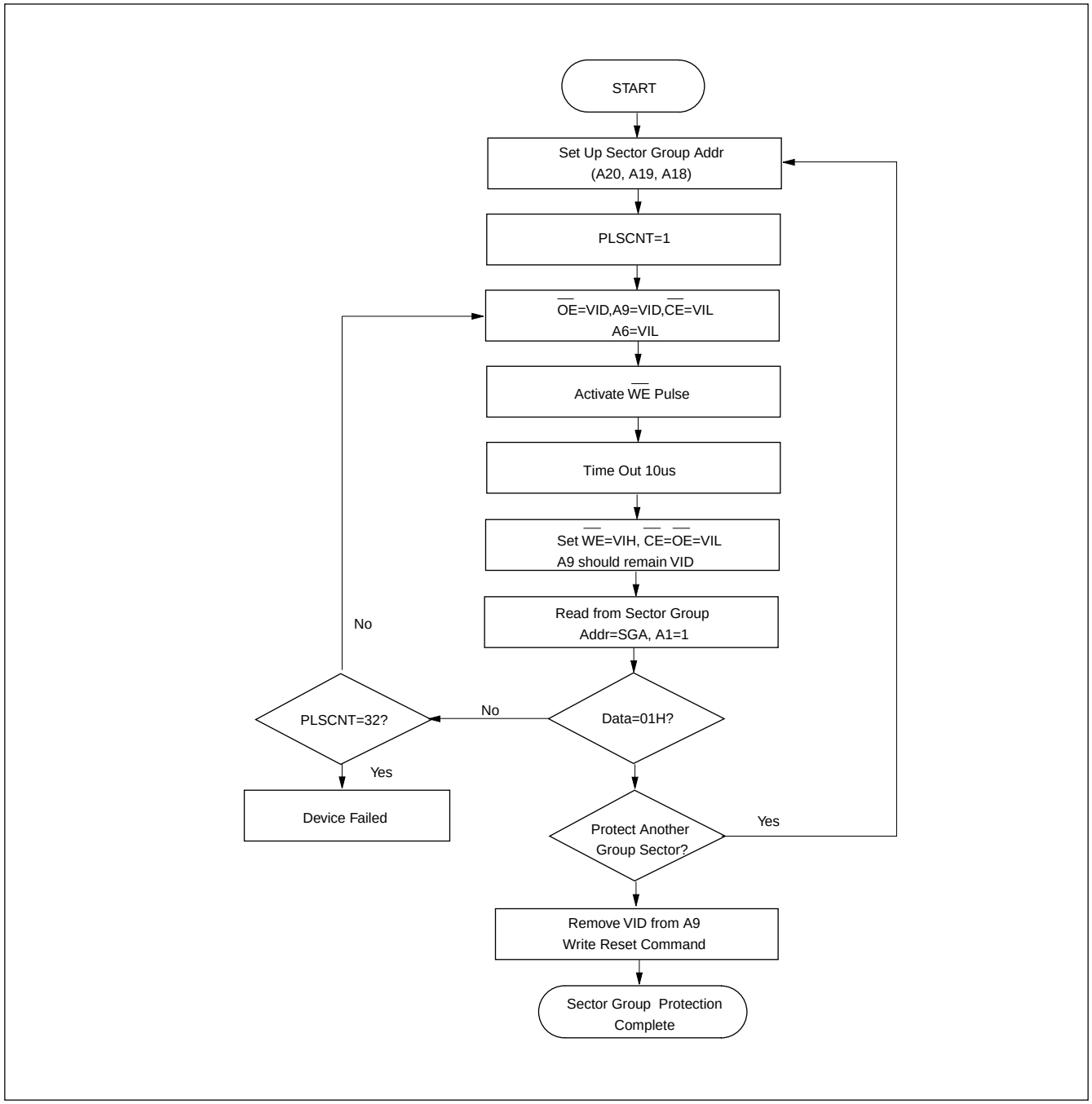
TIMING WAVEFORM FOR GROUP SECTOR PROTECTION FOR SYSTEM WITH 12V



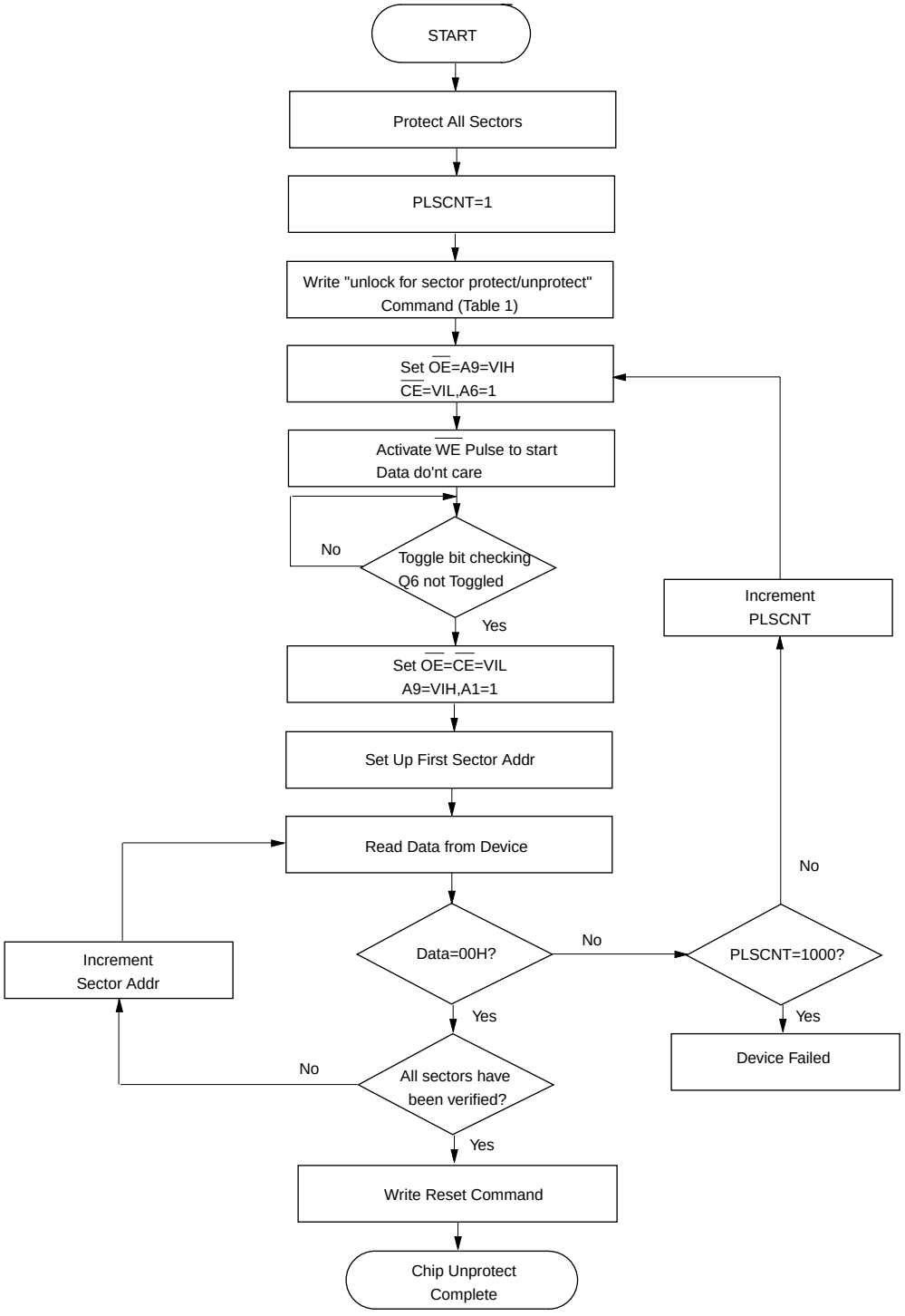
TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITH 12V



SECTOR GROUP PROTECTION ALGORITHM FOR SYSTEM WITH 12V

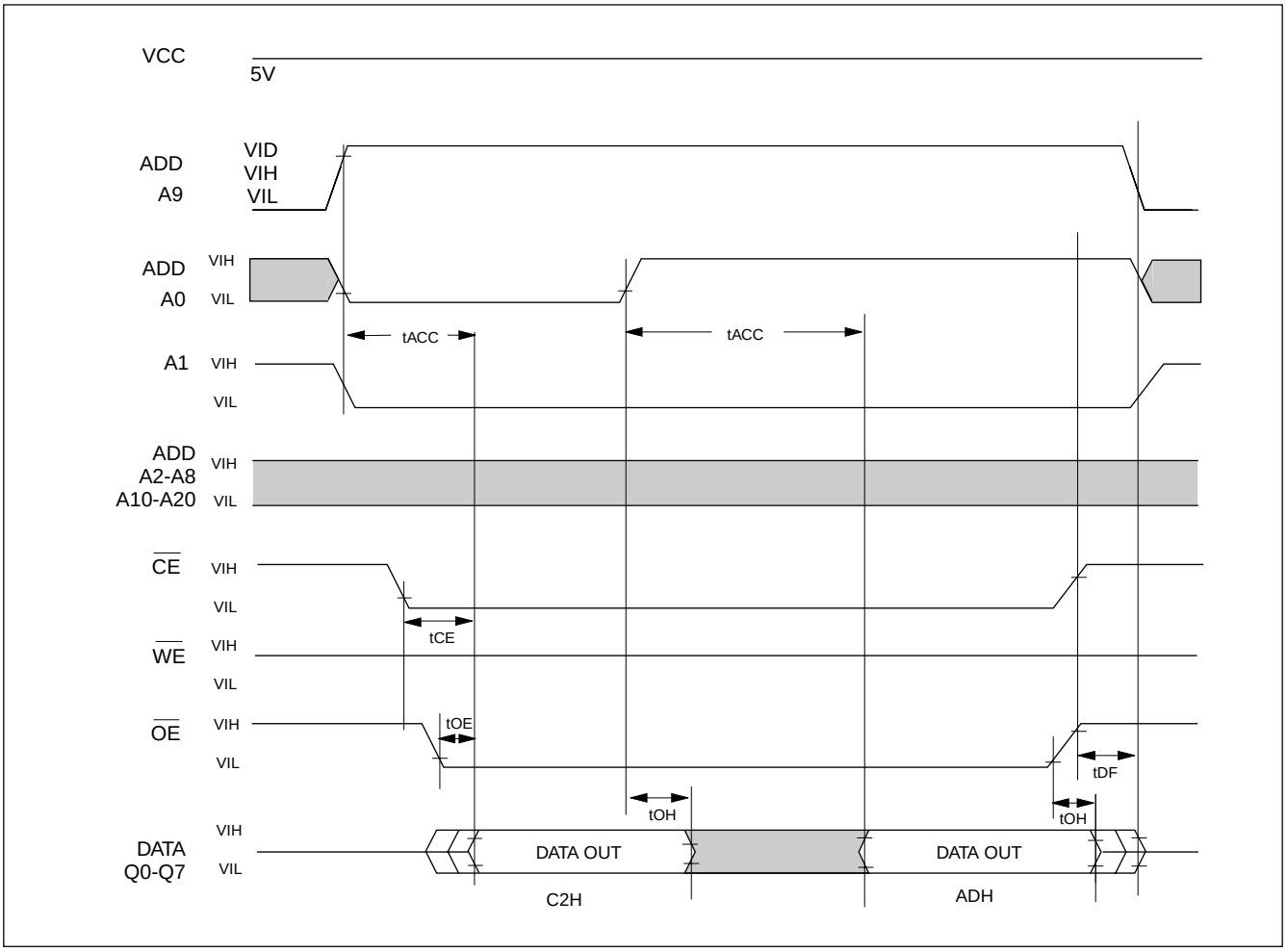


CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITH 12V



* It is recommended before unprotect whole chip, all sectors should be protected in advance.

ID CODE READ TIMING WAVEFORM



ORDERING INFORMATION

PLASTIC PACKAGE

PART NO.	ACCESS TIME (ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	PACKAGE
MX29F016T4C-70	70	50	100	40 Pin TSOP (Normal Type)
MX29F016T4C-90	90	50	100	40 Pin TSOP (Normal Type)
MX29F016T4C-12	120	50	100	40 Pin TSOP (Normal Type)
MX29F016R4C-70	70	50	100	40 Pin TSOP (Reverse Type)
MX29F016R4C-90	90	50	100	40 Pin TSOP (Reverse Type)
MX29F016R4C-12	120	50	100	40 Pin TSOP (Reverse Type)
MX29F016MC-70	70	50	100	44 Pin SOP
MX29F016MC-90	90	50	100	44 Pin SOP
MX29F016MC-12	120	50	100	44 Pin SOP
MX29F016TC-70	70	50	100	48 Pin TSOP (Normal Type)
MX29F016TC-90	90	50	100	48 Pin TSOP (Normal Type)
MX29F016TC-12	120	50	100	48 Pin TSOP (Normal Type)
MX29F016RC-70	70	50	100	48 Pin TSOP (Reverse Type)
MX29F016RC-90	90	50	100	48 Pin TSOP (Reverse Type)
MX29F016RC-12	120	50	100	48 Pin TSOP (Reverse Type)

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