# Wide Dynamic Range Image Reject MOPLL

Data Sheet

## Features

October 2004

- Single chip mixer/oscillator PLL combination for multi band tuner for DTT applications
- Each mixer oscillator band optimized for wide dynamic range
- RF input stages allow for either single-ended or differential drive
- PLL frequency synthesizer designed for low phase noise performance
- Broadband output level detect with onset adjust
- PLL frequency synthesizer compatible with standard digital terrestrial offsets
- Four integrated switching ports
- $I^2C$ fast mode compliant
- ESD protection (Normal ESD handling procedures should be observed)

## Applications

- Terrestrial digital receiver systems
- Terrestrial analogue receiver systems
- Cable receiver systems
- Data communications systems

**Ordering Information**

| | | |
|---|---|---|
| SL2610/IG/LH1Q | 40 Pin MLP | Tape & Reel, Bake & Drypack |
| SL2610/IG/LH1N | 40 Pin MLP | Trays, Bake & Drypack |
| SL2610/IG/LH2Q | 40 Pin MLP | Tape & Reel, Bake & Drypack* |
| SL2610/IG/LH2N | 40 Pin MLP | Trays, Bake & Drypack* |

*Leadfree

**-40°C to +85°C**

## Description

The SL2610 is a mixer oscillator intended primarily for application in all band tuners, where it performs image reject downconversion of the RF channel to a standard 36 MHz or 44 MHz IF.

Each band consists of a low noise preamplifier/mixer and local oscillator with an external varactor tuned tank. The band outputs share a common low impedance SAWF driver stage.

Frequency selection is controlled by the on-board $I^2C$ bus frequency synthesizer. This block also controls four general purpose switching ports for selecting the prefilter/AGC stages.

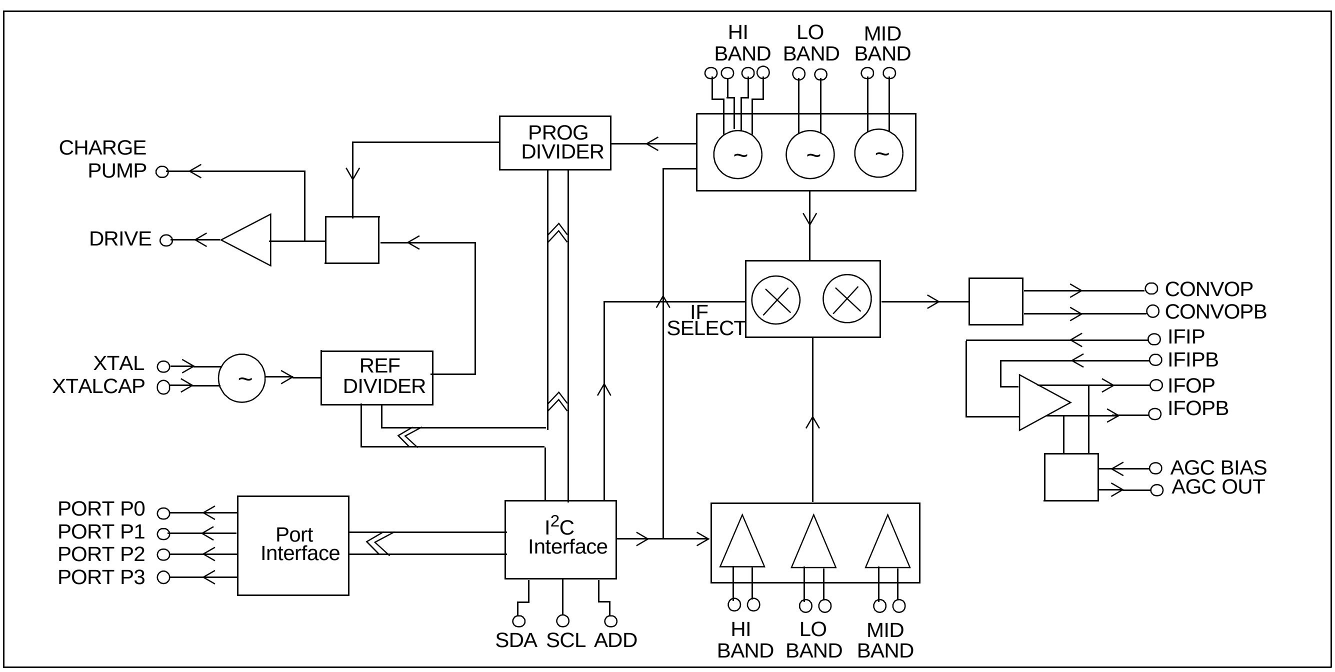



**Figure 1 - SL2610 Block Diagram**

The SL2610 has high intermodulation intercept performance so offering high signal to spurious performance in the presence of higher amplitude interferers or in the presence of a wide bandwidth composite input signal.

An output broadband level detect circuit is included for control of the tuner front end AGC.

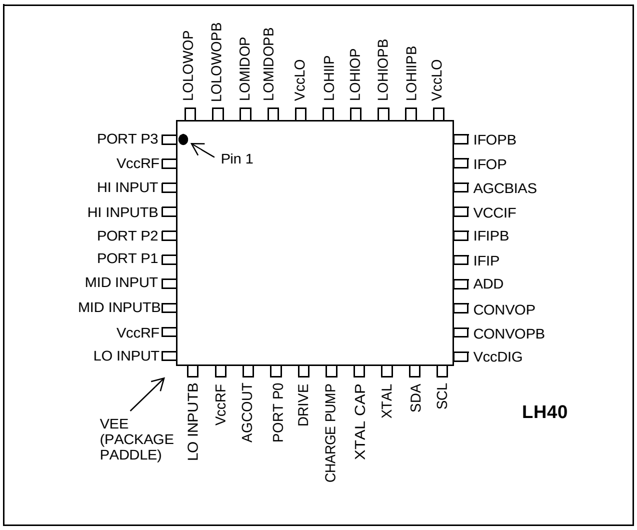



**Figure 2 - Pin Allocation Diagram**

**Quick Reference Data**

| Characteristics | | | Units |
|---|---|---|---|
| Frequency range: | LOW band | 50-500 | MHz |
| | MID band | 50-500 | MHz |
| | HIGH band | 200-900 | MHz |
| Conversion gain * | | $32 \pm 2$ | dB |
| Noise figure | | 13 | dB |
| Typical Image Reject | | 35 | dB |
| P1dB input referred, Converter section only | | 106 | dBuV |
| IP3 input referred, Converter section only | | 14 | dBm |
| IP2 input referred, Converter section only | | 48 | dBm |
| LO phase noise (free running) | @ 10 kHz offset | -90 | dBc/Hz |
| | @ 100 kHz offset | -110 | dBc/Hz |
| PLL phase noise | | -158 | dBc/Hz |
| Maximum composite output amplitude | | 3 | dBm |

* Assuming 2 dB shaping filter loss in external IF path.

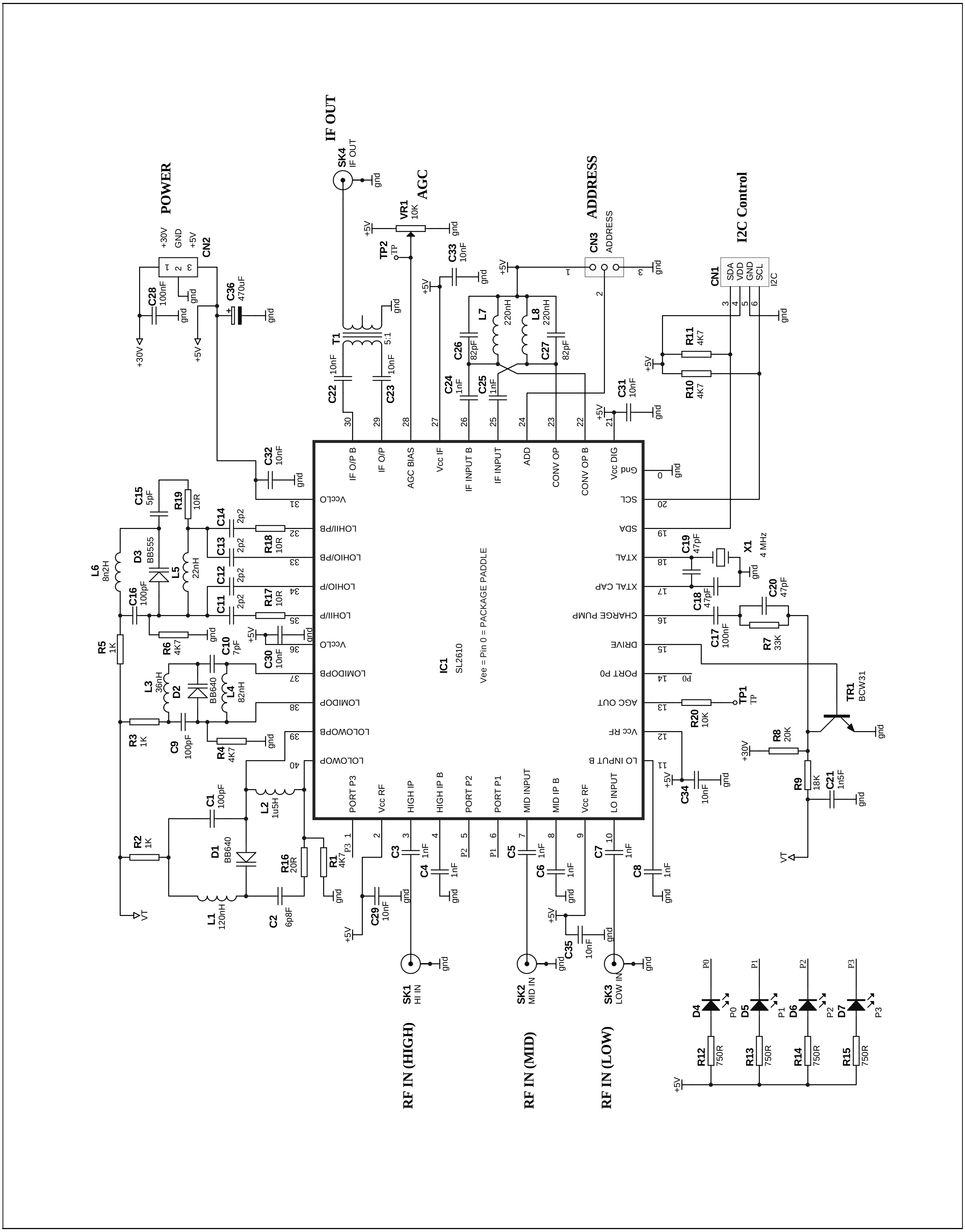



**Figure 3 - SL2610 Evaluation Board Schematic**

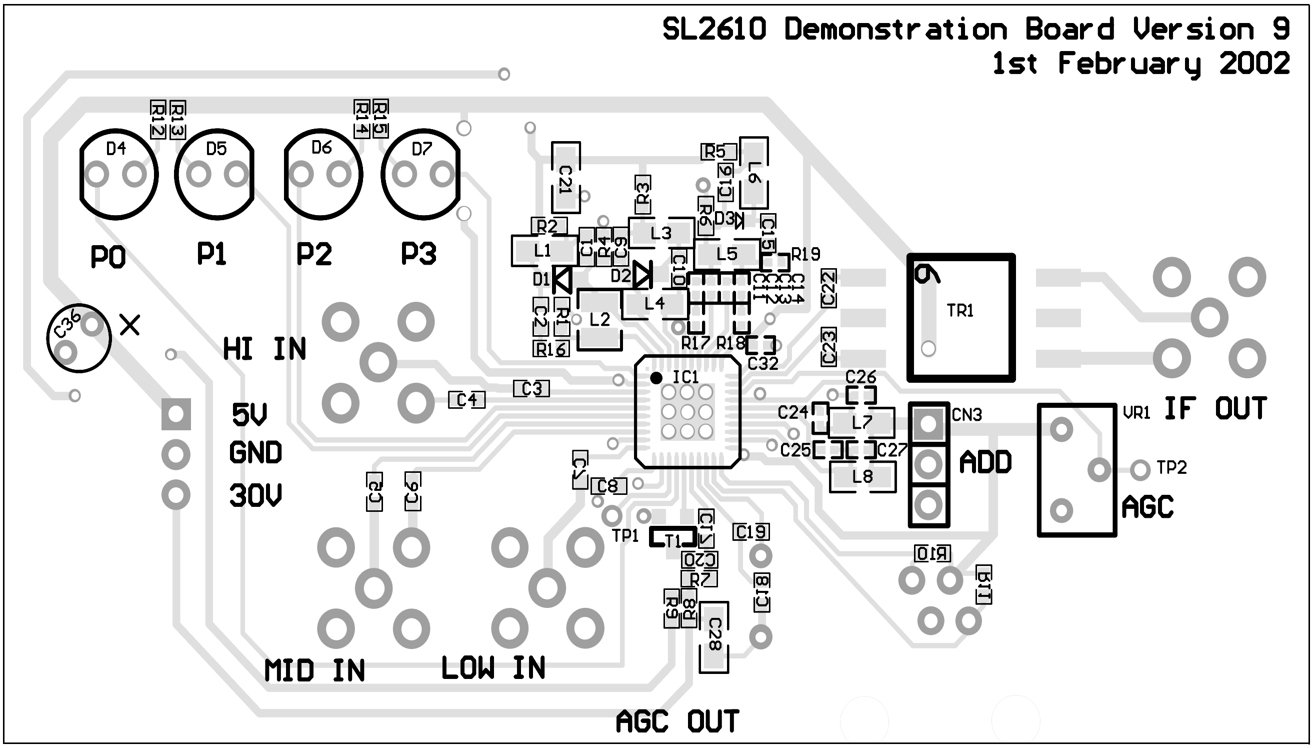



**Figure 4 - SL2610 Evaluation Board Layout (Top)**

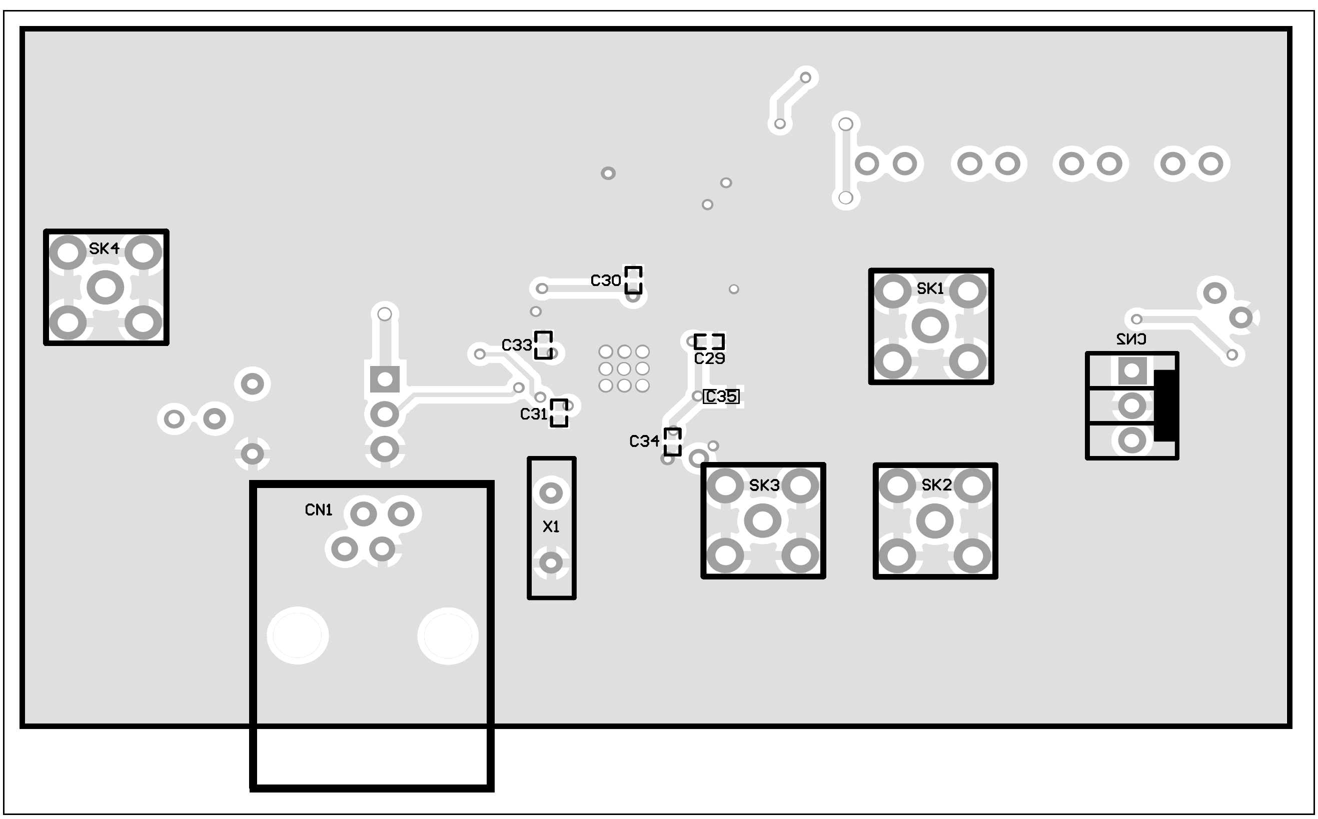



**Figure 5 - SL2610 Evaluation Board Layout (Bottom)**

# 1.0 Functional Description

The SL2610 is a multi band RF mixer oscillator with image reject and on-board frequency synthesizer. It is intended primarily for application in all band terrestrial tuners and requires a minimum external component count. It contains all elements required for RF downconversion to a standard IF with the exception of external VCO tank circuits.

The pin allocation is contained in Figure 2 and the block diagram in Figure 1.

## 1.1 Mixer/oscillator section

In normal application the RF input is interfaced to the selected mixer oscillator preamplifier through the tuner prefilter and AGC stages. The mixer input is arranged such that the signal can be coupled either differentially or single-ended, and achieves the specified minimum performance in both configurations. Band input impedances and NF are contained in Figure 11 and Figure 12 respectively. The converter two tone input spectra are contained in Figure 13 and Figure 14.

The preamplifier output then feeds the mixer stage where the required channel is image reject downconverted to the IF frequency. The local oscillator frequency for the downconversion is obtained from the on board local oscillator, which uses an external varactor tuned tank. Typical VCO applications are contained in Figures 8, 9 and 10.

The output of the mixer is then fed to the converter output driver which presents a matched 200 $\Omega$ differential load to an external IF shaping filter.

The output of the shaping filter is then coupled into the IFAMP stage, which provides further gain and offers a 50 $\Omega$ output impedance to interface direct with the tuner SAW filter.

The SL2610 contains a broadband level detect circuit whose output can be used to control the tuner AGC. The target level of the AGC detector is controlled by the voltage applied to the AGCBIAS pin. The characteristic of the target level is given in Figure 18.

## 1.2 PLL Frequency Synthesizer

The PLL frequency synthesizer section contains all the elements necessary, with the exception of a frequency reference and loop filter, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. It can also be operated with comparison frequencies appropriate for frequency offsets as required in digital terrestrial (DTT) receivers.

The LO signal is multiplexed from the selected oscillator section to an internal preamplifier which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces direct with the 15-bit fully programmable divider which is of MN+A architecture, where the dual modulus prescaler is 16/17, the A counter is 4-bits and the M counter is 11 bits.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on-board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into 1 of 29 ratios as detailed in Table 1.

The output of the phase detector feeds a charge pump and loop amplifier section which when used with an external loop filter integrates the current pulses into the varactor line voltage.

The programmable divider output Fpd, divided by two and the reference divider output Fcomp, can be switched to port P0 by programming the device into test mode. The test modes are described in Table 5.

## 2.0 Programming

The SL2610 is controlled by an $I^2C$ data bus and is compatible with both standard and fast mode formats.

Data and Clock are fed in on the SDA and SCL lines respectively as defined by $I^2C$ bus format. The synthesizer can either accept data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. Tables 2 and 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesizer in an $I^2C$ bus system (Tables 2 and 3). Table 4 shows how the address is selected by applying a voltage to the 'ADD' input. When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period the device generates an internal STOP condition which inhibits further reading.

### 2.1 Write mode

With reference to Table 2, bytes 2 and 3 contain frequency information bits $2^{14}$-$2^0$ inclusive. Byte 4 controls the reference divider ratio bits R4-R0 (Table 1) and the charge pump setting bits C1-C0 (Table 6). Byte 5 controls the IF select (Table 8), the band select function bits BS1-BS0 (Table 7), the switching ports P3-P0 and the test modes (Table 5).

After reception and acknowledgement of a correct address (byte 1), the first bit of the following byte determines whether the byte is interpreted as a byte 2 or 4, a logic '0' indicating byte 2 and a logic '1' indicating byte 4. Having interpreted this byte as either byte 2 or 4 the following data byte will be interpreted as byte 3 or 5 respectively. Having received two complete data bytes, additional data bytes can be entered, where byte interpretation follows the same procedure, without re-addressing the device. This procedure continues until a STOP condition is received. The STOP condition can be generated after any data byte, if however it occurs during a byte transmission, the previous byte data is retained. To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 15 bits of frequency data have been received, or after the generation of a STOP condition.

### 2.2 Read mode

When the device is in read mode, the status byte read from the device takes the form shown Table 3.

Bit 1 (POR) is the power-on reset indicator, and this is set to a logic '1' if the Vcc supply to the device has dropped below 3V (at $25^oC$), e.g., when the device is initially turned ON. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high this indicates that the programmed information may have been corrupted and the device reset to power up condition.

Bit 2 (FL) indicates whether the device is phase locked, a logic '1' is present if the device is locked and a logic '0' if the device is unlocked.

### 2.3 Programmable features

| | |
|---|---|
| Synthesiser programmable divider | Function as described above. |
| Reference programmable divider | Function as described above. |
| Band selection | The required mixer oscillator band and RF input is selected by bits BS1-BS0, within data byte 5, as defined in Table 7. |
| IF selection | The centre of the image reject passband is selected by IF as defined in Table 8. |
| Charge pump current | The charge pump current can be programmed by bits C1-C0 within data byte 4, as defined in Table 6. |
| Ports P3-P0 | These are configured as NPN open collector buffers and programmed by bits P3-P0.<br>Logic ‘1’ = on.<br>Logic ‘0’ = off (high impedance); default on power up.<br>In test modes, when TE=1, ports P3-P0 respond according to T2-T0 respectively and previously transmitted data is lost. |
| Test mode | The test modes are invoked by setting bits T2–T0 as described in Table 5. |

| R4 | R3 | R2 | R1 | R0 | Ratio |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 2 |
| 0 | 0 | 0 | 0 | 1 | 4 |
| 0 | 0 | 0 | 1 | 0 | 8 |
| 0 | 0 | 0 | 1 | 1 | 16 |
| 0 | 0 | 1 | 0 | 0 | 32 |
| 0 | 0 | 1 | 0 | 1 | 64 |
| 0 | 0 | 1 | 1 | 0 | 128 |
| 0 | 0 | 1 | 1 | 1 | 256 |
| 0 | 1 | 0 | 0 | 0 | not allowed |
| 0 | 1 | 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 0 | 1 | 1 | 20 |
| 0 | 1 | 1 | 0 | 0 | 40 |
| 0 | 1 | 1 | 0 | 1 | 80 |
| 0 | 1 | 1 | 1 | 0 | 160 |
| 0 | 1 | 1 | 1 | 1 | 320 |
| 1 | 0 | 0 | 0 | 0 | not allowed |
| 1 | 0 | 0 | 0 | 1 | 6 |
| 1 | 0 | 0 | 1 | 0 | 12 |
| 1 | 0 | 0 | 1 | 1 | 24 |
| 1 | 0 | 1 | 0 | 0 | 48 |
| 1 | 0 | 1 | 0 | 1 | 96 |
| 1 | 0 | 1 | 1 | 0 | 192 |
| 1 | 0 | 1 | 1 | 1 | 384 |
| 1 | 1 | 0 | 0 | 0 | not allowed |
| 1 | 1 | 0 | 0 | 1 | 7 |
| 1 | 1 | 0 | 1 | 0 | 14 |
| 1 | 1 | 0 | 1 | 1 | 28 |
| 1 | 1 | 1 | 0 | 0 | 56 |
| 1 | 1 | 1 | 0 | 1 | 112 |
| 1 | 1 | 1 | 1 | 0 | 224 |
| 1 | 1 | 1 | 1 | 1 | 448 |

**Table 1 - Reference Division Ratio**

| | MSB | | | | | | | LSB | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Address** | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | 0 | A | **Byte 1** |
| **Programmable divider** | 0 | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | A | **Byte 2** |
| **Programmable divider** | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ | A | **Byte 3** |
| **Control data** | 1 | C1 | C0 | R4 | R3 | R2 | R1 | R0 | A | **Byte 4** |
| **Control data** | IF | BS1 | BS0 | TE | P3/T2 | P2/T1 | P1/T0 | P0 | A | **Byte 5** |

**Table 2 - Write Data Format (MSB is transmitted first)**

| | MSB | | | | | | | LSB | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Address** | 1 | 1 | 0 | 0 | 0 | MA1 | MA0 | 1 | A | **Byte 1** |
| **Status Byte** | POR | FL | 0 | 0 | 0 | 0 | 0 | 0 | A | **Byte 2** |

**Table 3 - Read Data Format (MSB is transmitted first)**

| | | |
|---|---|---|
| A | : | Acknowledge bit |
| MA1,MA0 | : | Variable address bits (see Table 4) |
| $2^{14}$-$2^{0}$ | : | Programmable division ratio control bits |
| R4-R0 | : | Reference division ratio select (see Table 1) |
| C1,C0 | : | Charge pump current select (see Table 6) |
| BS1-BS0 | : | Band select bits (see Table 7) |
| IF | : | IF passband select (see Table 8) |
| TE | : | Test mode enable |
| T2-T0 | : | Test mode control bits when TE=1 (see Table 5) |
| P3-P0 | : | P3-P0 port output states |
| POR | : | Power on reset indicator |
| FL | : | Phase lock flag |

| MA1 | MA0 | Address Input Voltage Level |
|---|---|---|
| 0 | 0 | 0-0.1Vcc |
| 0 | 1 | Open circuit |
| 1 | 0 | 0.4Vvcc – 0.6 Vcc # |
| 1 | 1 | 0.9 Vcc - Vcc |

# Programmed by connecting a 30 kΩ resistor between pin and Vcc

**Table 4 - Address Selection**

| TE | T2 | T1 | T0 | Test Mode Description |
|---|---|---|---|---|
| 0 | X | X | X | Normal operation |
| 1 | 0 | 0 | 0 | Normal operation |
| 1 | 0 | 0 | 1 | Charge pump sink *<br>Status byte FL set to logic ‘0’ |
| 1 | 0 | 1 | 0 | Charge pump source *<br>Status byte FL set to logic ‘0’ |
| 1 | 0 | 1 | 1 | Charge pump disabled *<br>Status byte FL set to logic ‘1’ |
| 1 | 1 | 0 | 0 | Normal operation and Port P0 = Fpd/2 |
| 1 | 1 | 0 | 1 | Charge pump sink *<br>Status byte FL set to logic ‘0’<br>Port P0 = Fcomp |
| 1 | 1 | 1 | 0 | Charge pump source *<br>Status byte FL set to logic ‘0’<br>Port P0 = Fcomp |
| 1 | 1 | 1 | 1 | Charge pump disabled *<br>Status byte FL set to logic ‘1’<br>Port P0 = Fcomp |

**Table 5 - Test Modes**

* crystal and selected local oscillator need signals to enable charge pump test modes and to toggle status byte bit FL

X -’don’t care’

| C1 | C0 | Current in µA | | |
|---|---|---|---|---|
| | | Min. | Typ. | Max. |
| 0 | 0 | ±85 | ±130 | ±175 |
| 0 | 1 | ±190 | ±280 | ±370 |
| 1 | 0 | ±420 | ±600 | ±780 |
| 1 | 1 | ±930 | ±1300 | ±1670 |

**Table 6 - Charge pump current**

| BS1 | BS0 | Band Selected |
|---|---|---|
| 0 | 0 | LO Band |
| 0 | 1 | MID Band |
| 1 | 0 | HI band |
| 1 | 1 | HI band |

**Table 7 - Band select**

| IF input | Centre of Image Reject Passband | Passband Bandwidth |
|---|---|---|
| 0 | 57 MHz | 6 MHz |
| 0 | 44 MHz | 6 MHz |
| 1 | 36 MHz | 8 MHz |

**Table 8 - IF SELECT function**

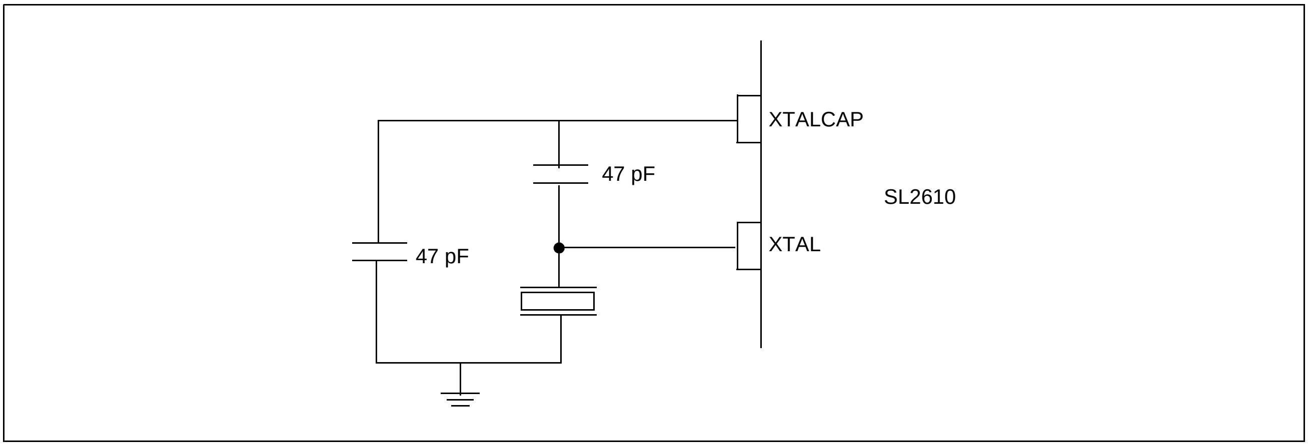



**Figure 6 - Crystal Oscillator Application**

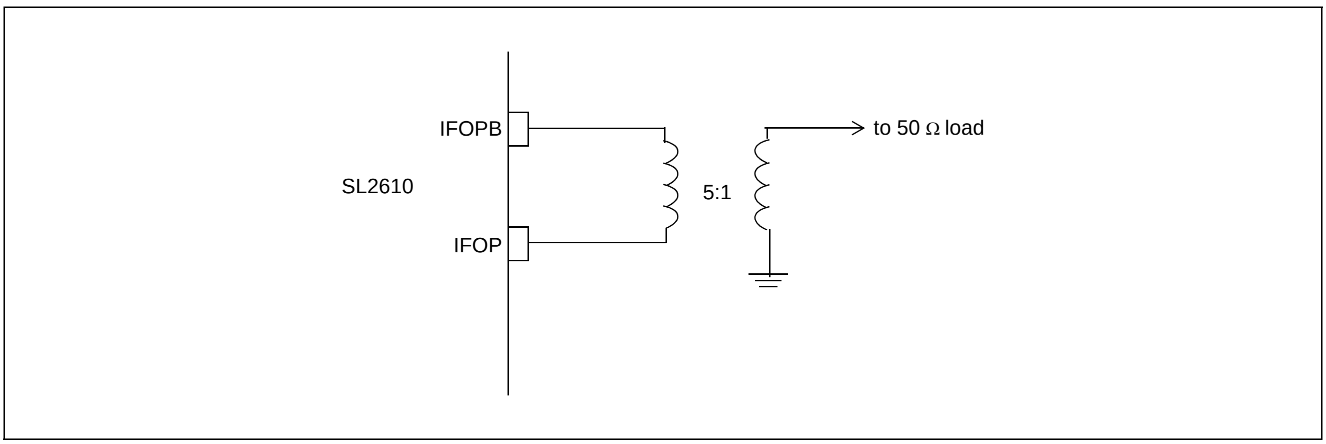



**Figure 7 - Ifamp Output Load Condition for Test Purposes**

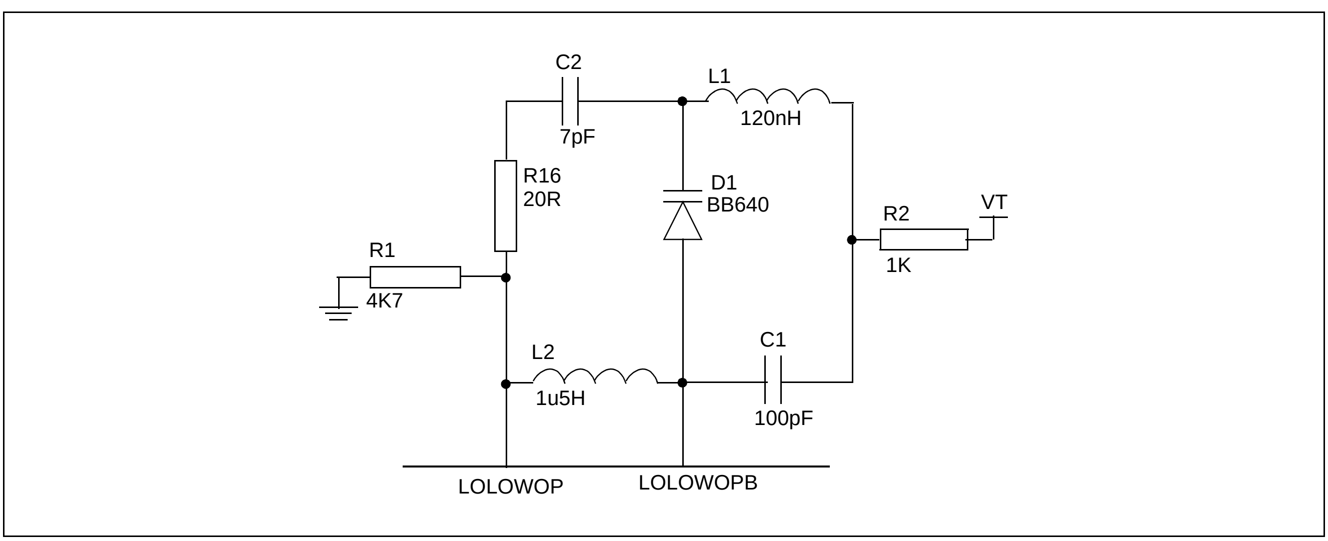



**Figure 8 - LO Band VCO Application**

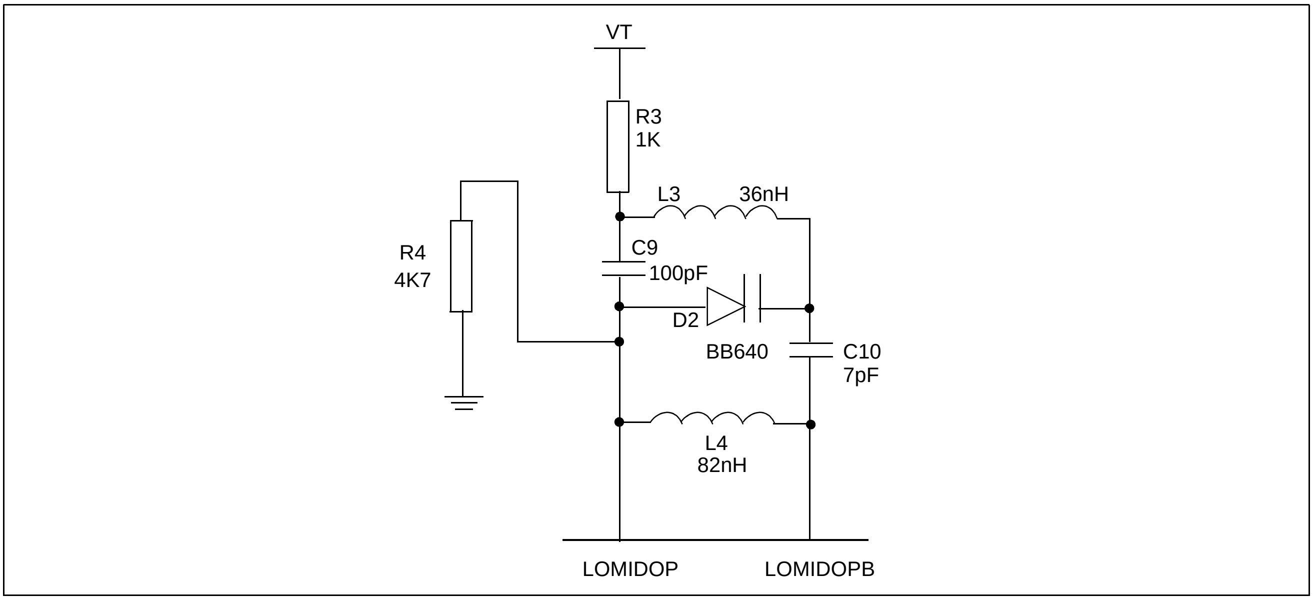



**Figure 9 - Mid Band VCO Application**

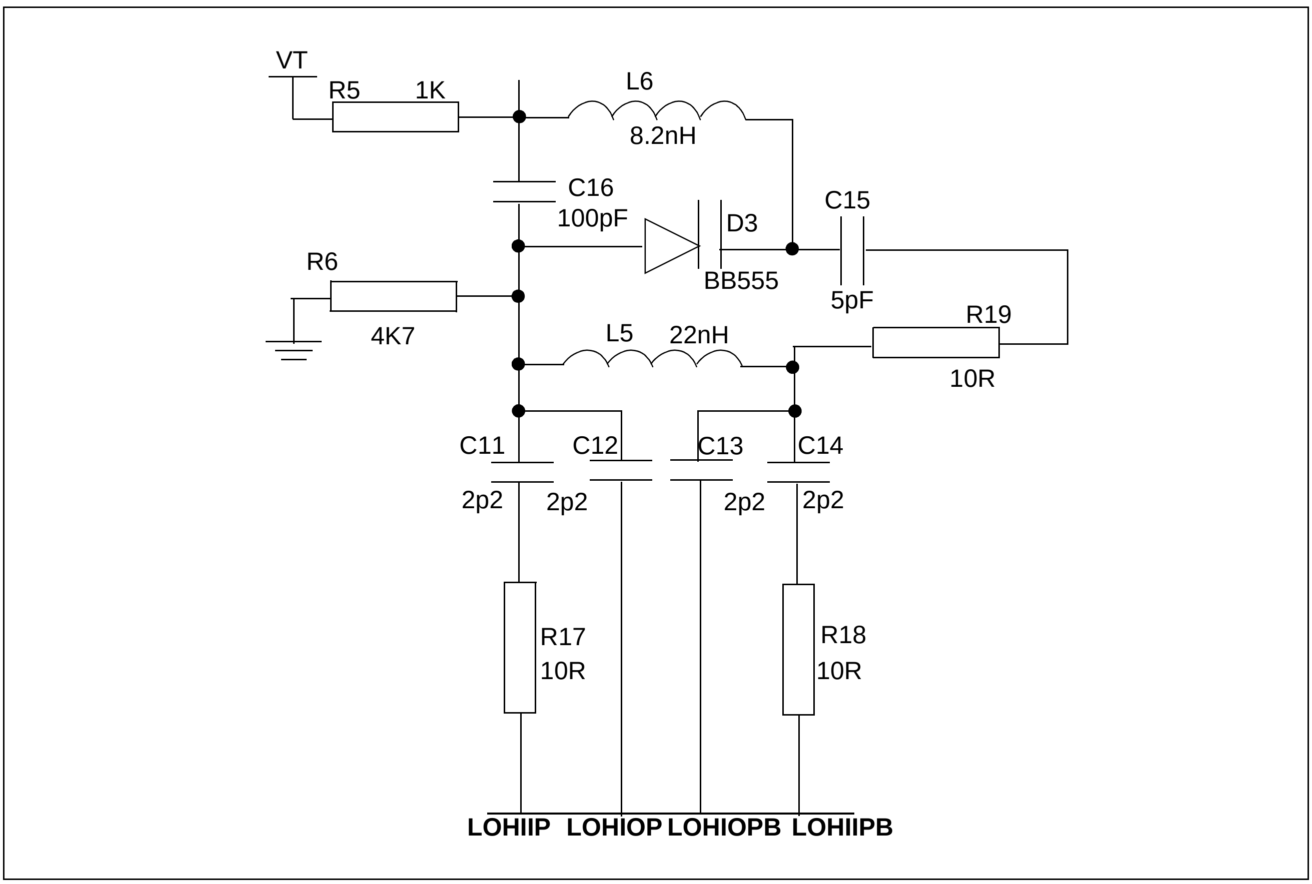



**Figure 10 - HI Band VCO Application**

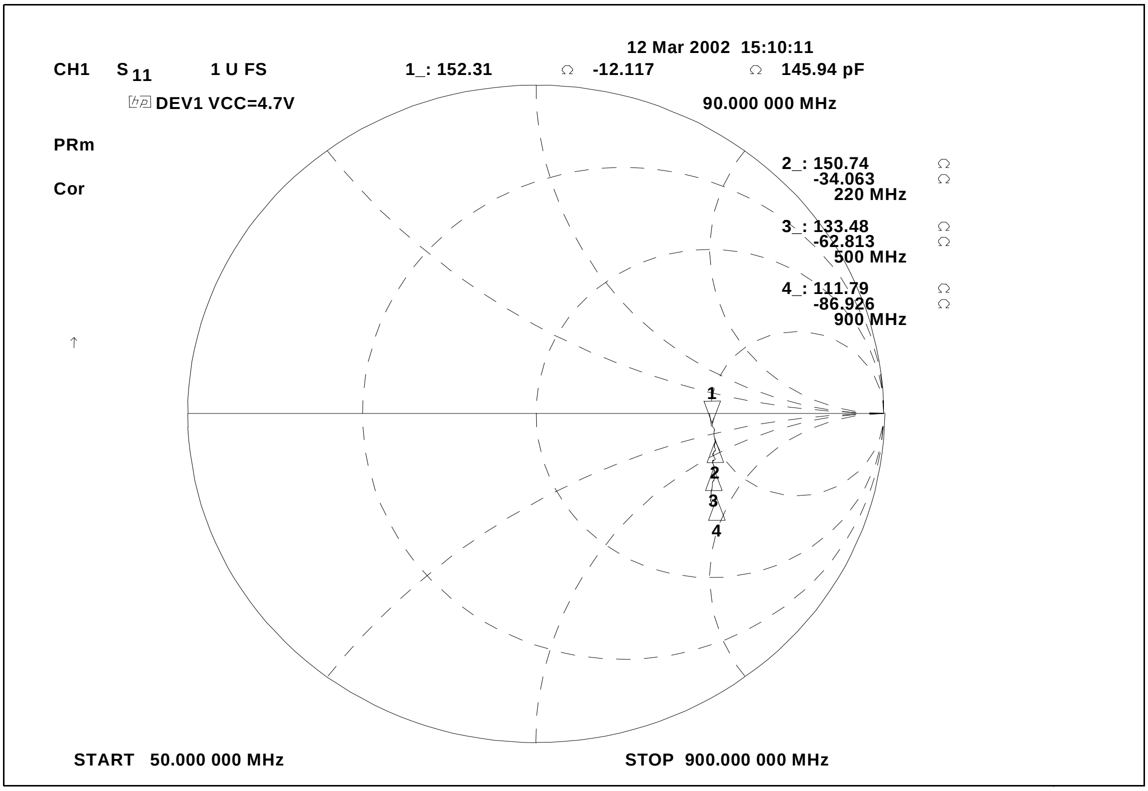



**Figure 11 - LO, MID and HI Band Input Impedance**

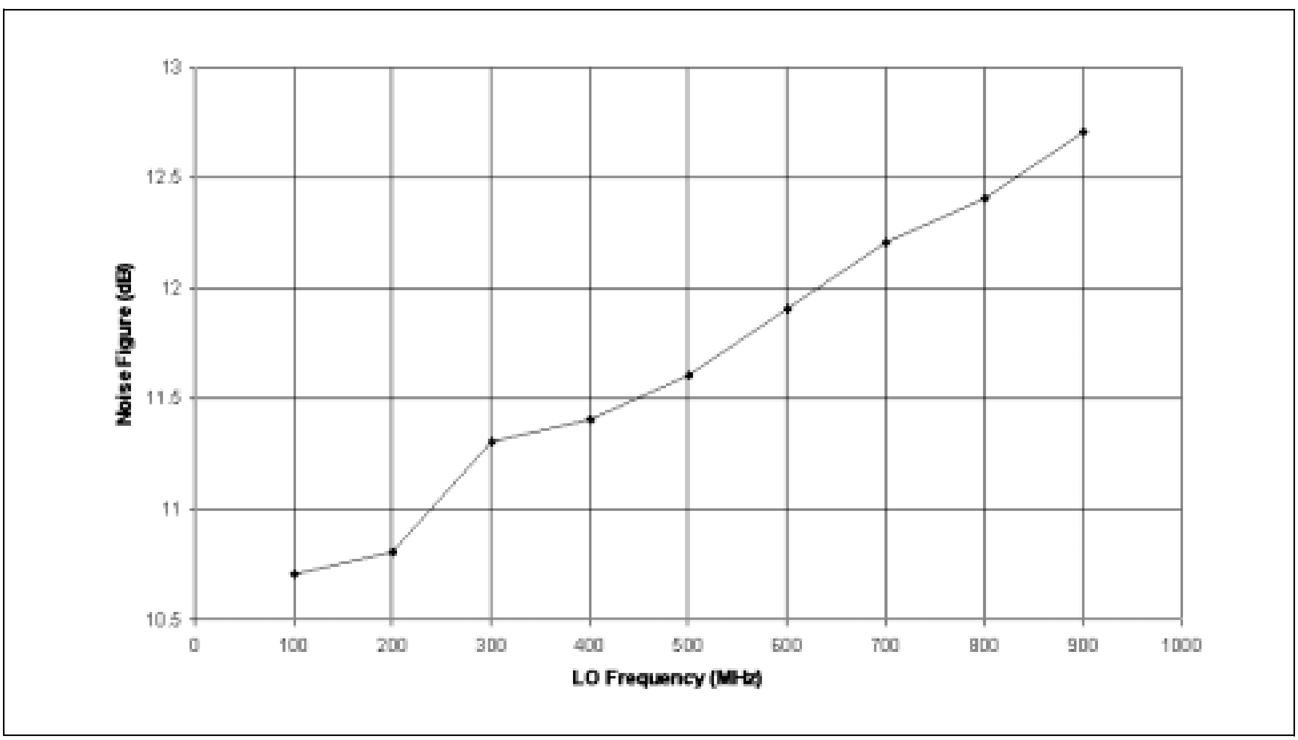



**Figure 12 - Low, Mid and Hi Band Noise Figure versus Frequency**

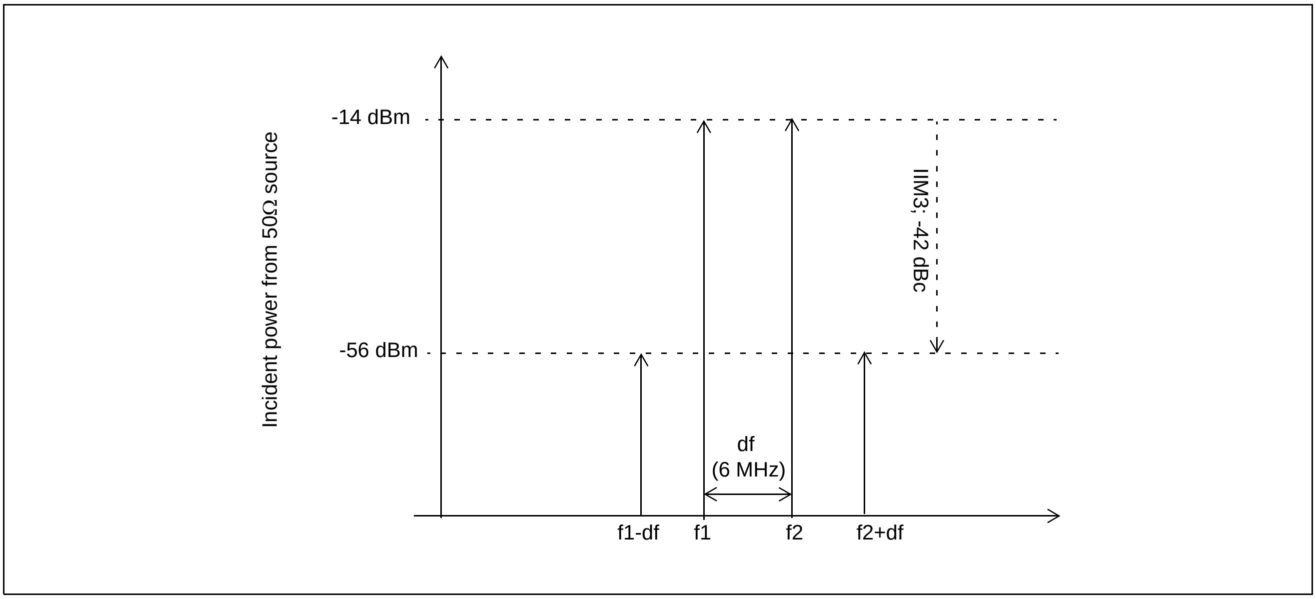



**Figure 13 - Converter Third Order Two Tone Intermodulation Test Condition Spectrum, Input Referred, All Bands**

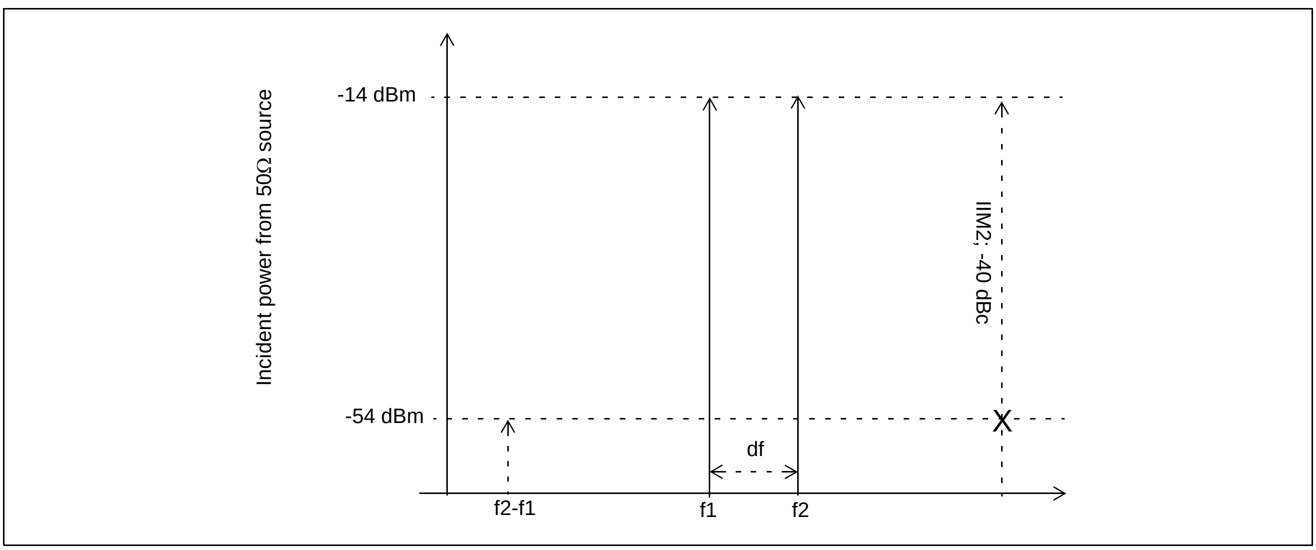



**Figure 14 - Second Order Two Tone Intermodulation Test Condition Spectrum, Input Referred**

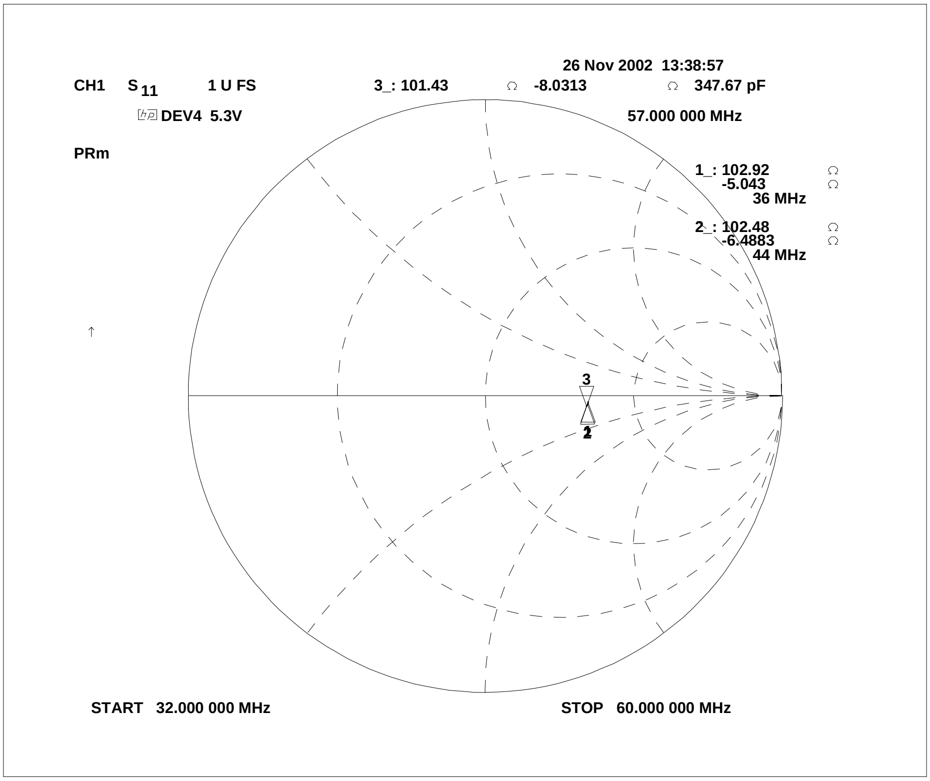



**Figure 15 - Converter Output Impedance (Single Ended)**

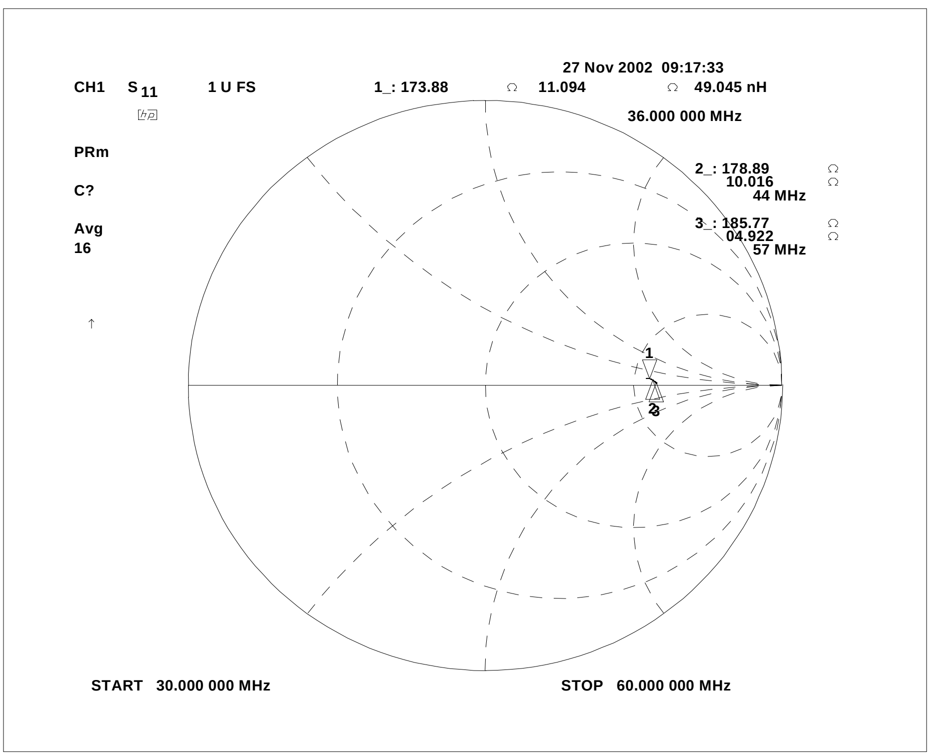



**Figure 16 - IFAMP Input Impedance**

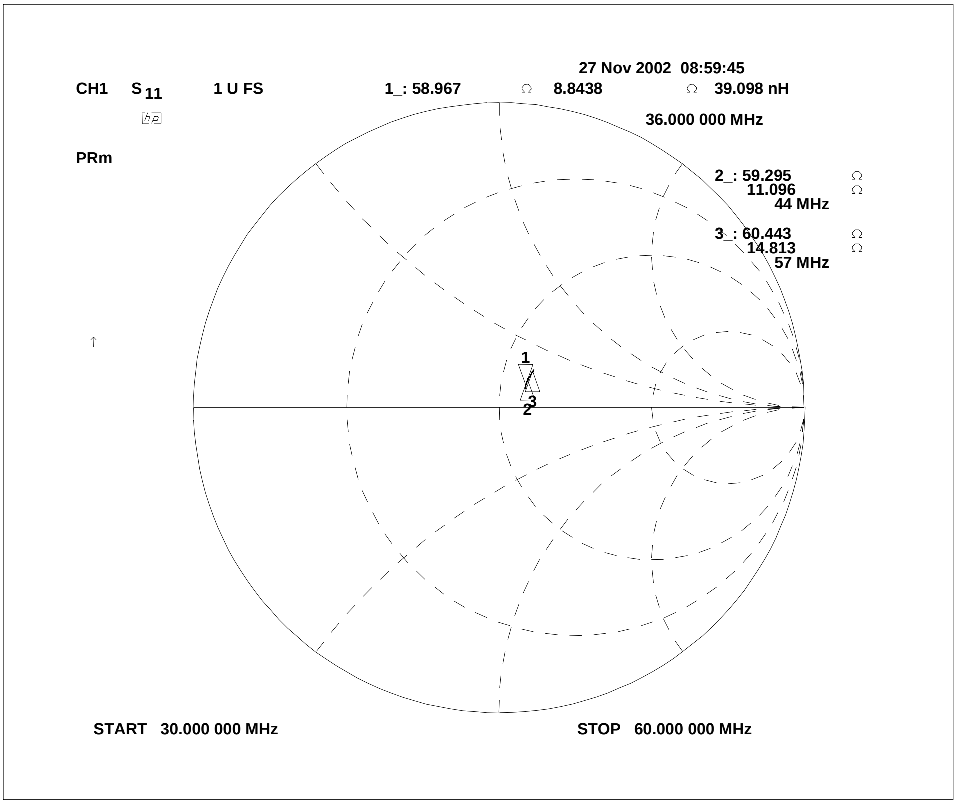



**Figure 17 - IFAMP Output Impedance (Single Ended)**

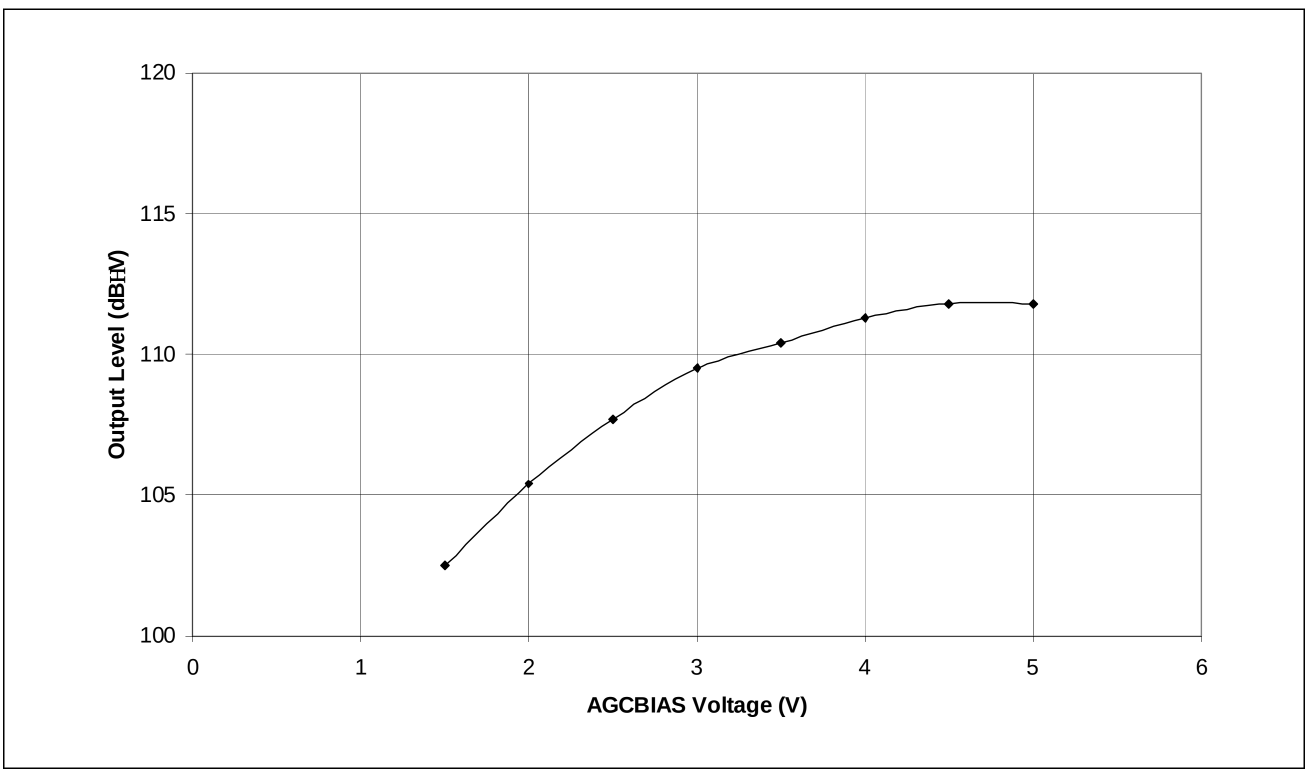



**Figure 18 - Typical AGC Output Level Set versus AGCBIAS Voltage**

## Electrical Characteristics

### Test conditions (unless otherwise stated)

$T_{amb}$ = -40$^{o}$C to 85$^{o}$C, Vee= 0 V, Vcc=Vcca=Vccd = 5 V $\pm$5%

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

| Characteristic | Pin | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Supply current | | | 163 | 196 | mA | All switching ports off. |
| **LO or MID BAND ENABLED** | | | | | | |
| Input frequency range | | 50 | | 500 | MHz | |
| Input impedance | | | | | | See Figure 11 and refer to Note 8. |
| Input Noise Figure | | | | 13 | dB | Tamb=27$^{o}$C, see Figure 12, refer to Note 2, no correction for external filtering. |
| Converter gain | | 10<br>8.5 | | 14<br>12.5 | dB<br>dB | At 36 MHz and 44 MHz IF frequency.<br>At 57 MHz IF frequency.<br>Conversion gain from 50 Ω single ended source to differential<br>200 Ω load, refer to Note 3. |
| Conversion gain to IFAMP output | | 28<br>25 | | 36<br>33 | dB<br>dB | At 36 MHz and 44 MHz IF frequency.<br>At 57 MHz IF frequency.<br>Conversion gain from 50 Ω single ended source to 50 Ω single-ended load with output transformer as in Figure 7, see Notes 2 and 3. |
| Gain variation within channel | | | 0.4 | 1 | dB | Channel bandwidth 8 MHz within operating frequency range, see note (2), excluding interstage shaping filter ripple. |
| Converter input referred IP2 | | 26 | | | dBm | See Figure 14 and refer to Notes 4 and 6. Assuming ideal power match. |
| Converter input referred IM2 | | | | -40 | dBc | See Figure 14 and refer to Notes 4 and 6. |
| Converter input referred IP3 | | 7 | | | dBm | See Figure 13 and refer to Notes 4 and 6. Assuming ideal power match. |
| Converter input referred IM3 | | | | -42 | dBc | See Figure 13 and refer to Notes 4 and 6. |
| Input referred P1dB | | 101 | | | dBμV | |
| Local oscillator operation range | | 50 | | 550 | MHz | Refer to Note 7. |
| Local oscillator tuning range | | 68<br>200 | | 225<br>465 | MHz<br>MHz | With application as in Figure 8.<br>With application as in Figure 9. |

| Characteristic | Pin | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| LO phase noise, SSB<br>@ 1 kHz offset<br>@ 10 kHz offset<br>@ 100 kHz offset | | | | <br>-55<br>-86<br>-109 | <br>dBc/Hz<br>dBc/Hz<br>dBc/Hz | With application as in Figure 8 and Figure 9 outside of PLL loop bandwidth. |
| LO temperature stability | | | | 80 | kHz/$^{o}$C | Application as in Figure 8 and Figure 9.<br>No temperature compensation. |
| LO turn on drift | | | | 100 | kHz | Application as in Figure 8 and Figure 9, frequency drift over 15 minute period from turn on at a fixed ambient temperature.<br>No temperature compensation. |
| LO to RF input leakage | | | | 60 | dBμV | Application as in Figures 8 and 9. |
| LO Vcc stability | | | | 0.5 | MHz/V | |
| LO spurs due to RF pulling | | | | -52 | dBc | See Note 5. |
| **HI BAND ENABLED** | | | | | | |
| Input frequency range | | 200 | | 870 | MHz | |
| Input impedance | | | | | | See Figure 11 and refer to Note 8. |
| Input Noise Figure | | | | 13.5 | dB | Tamb=27$^{o}$C, see Figure 12, refer to Note 2, no correction for external filtering. |
| Converter gain | | 10<br>8.5 | | 14<br>12.5 | dB<br>dB | At 36 MHz and 44 MHz IF frequency.<br>At 57 MHz IF frequency.<br>Conversion gain from 50 Ω single ended source to differential 200 Ω load, refer to Note 3. |
| Conversion gain to IFAMP output | | 28<br>25 | | 36<br>33 | dB<br>dB | At 36 MHz and 44 MHz IF frequency.<br>At 57 MHz IF frequency.<br>Conversion gain from 50 Ω single ended source to 50 Ω single-ended load with output transformer as in Figure 7, see Notes 2 and 3. |
| Gain variation within channel | | | 0.4 | 1 | dB | Channel bandwidth 8 MHz within operating frequency range, see Note 3, excluding interstage shaping filter ripple. |
| Converter input referred IP2 | | 26 | | | dBm | See Figure 14 and refer to Notes 4 and 6. Assuming ideal power match. |

| Characteristic | Pin | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Converter input referred IM2 | | | | -40 | dBc | See Figure 14 and refer to Notes 4 and 6. |
| Converter input referred IP3 | | 7 | | | dBm | See Figure 13 and refer to Notes 4 and 6. Assuming ideal power match. |
| Converter input referred IM3 | | | | -42 | dBc | See Figure 13 and refer to Notes 4 and 6. |
| Input referred P1dB | | 101 | | | dBμV | |
| Local oscillator operation range | | 200 | | 1000 | MHz | Refer to Note 7. |
| Local oscillator tuning range | | 440 | | 950 | MHz | With application as in Figure 10. |
| LO phase noise, SSB<br>@ 1 kHz offset<br>@ 10 kHz offset<br>@ 100 kHz offset | | | | <br>-55<br>-86<br>-109 | <br>dBc/Hz<br>dBc/Hz<br>dBc/Hz | With application as in Figure 10, outside of PLL loop bandwidth. |
| LO temperature stability | | | | 110 | kHz/$^{o}$C | Application as in Figure 10.<br>No temperature compensation. |
| LO turn on drift | | | | 100 | kHz | Application as in Figure 10, frequency drift over 15 minute period from turn on at a fixed ambient temperature.<br>No temperature compensation. |
| LO to RF input leakage | | | | 60 | dBμV | Application as in Figure 10. |
| LO Vcc stability | | | | 0.5 | MHz/V | |
| LO spurs due to RF pulling | | | | -52 | dBc | See Note 5. |
| **All Bands** | | | | | | |
| Converter output impedance | | | 200 | | Ω | Differential, see Figure 15. |
| Image rejection | | 25<br>29<br>25 | 30<br>35<br>30 | | dB<br>dB<br>dB | At 36 MHz IF frequency, IF bit = 1.<br>At 44 MHz IF frequency, IF bit = 0.<br>At 57 MHz IF frequency, IF bit = 0.<br>See Table 8.<br>Tamb = 0$^{o}$C to +85$^{o}$C.<br>Tank Schematics and layouts as in recommended application. See Figures 4 and 5. |
| Isolation between band inputs | | | | -60 | dBc | Level of desired signal converted to IF output through disabled band relative to signal converted through enabled band. |
| Composite output amplitude | | | | 3 | dBm | |

| Characteristic | Pin | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **IFAMP** | | | | | | |
| Input frequency range | | 32 | | 60 | MHz | |
| Input impedance | | | 200 | | Ω | Differential, see Figure 16. |
| Gain | | 20<br>18.5 | | 24<br>22.5 | dB<br>dB | At 36 MHz and 44 MHz IF frequency.<br>At 57 MHz IF frequency.<br>Voltage conversion gain from 200 Ω differential source to differential load as contained in Figure 7, see Note 3. |
| Output impedance | | | 100 | | Ω | Differential, see Figure 17. |
| Output limiting | | 3<br>2.7 | | | Vp-p<br>Vp-p | At 36 MHz and 44 MHz IF fequency.<br>At 57 MHz IF frequency.<br>Differential into load as in Figure 7. |
| IFAMP OPIP3 | | 135 | | | dBμV | Two output tones at 2 MHz separation at 104 dBuV into load as in Figure 7, see Note 2. |
| IFAMP OPIM3 | | | | -62 | dBc | Two output tones at 2 MHz separation at 104 dBuV into load as in Figure 7, see Note 2. |
| AGCBIAS Leakage current | 28 | -100<br>-50 | | 100<br>50 | μA<br>μA | Vee ≤ Vagc1 ≤ Vcc<br>1.5V ≤ Vagc1 ≤ 3.5V |
| AGCOUT voltage range | 13 | 0.5 | | 3 | V | Max load current 20 μA. |
| AGC output level set | | | | | | See Figure 18. |
| Supply rejection | | | | -52 | dBc | Spurs introduced on converted output relative to desired signal by a supply ripple voltage of 10 mV p-p in the range 1 kHz to 100 kHz (including external supply decoupling). |
| **Synthesiser** | | | | | | |
| SDA, SCL<br>Input high voltage<br>Input low voltage<br>Input current<br>Leakage current | 19, 20 | <br>3<br>0<br>-10 | | <br>5.5<br>1.5<br>10<br>10 | <br>V<br>V<br>μA<br>μA | <br><br><br>Input voltage =Vee to Vcc<br>Input voltage = Vee to 5.5 V, Vcc=Vee |
| Hysterysis | 19, 20 | | 0.4 | | V | |
| SDA output voltage | 19 | | | 0.4<br>0.6 | V<br>V | Isink = 3 mA<br>Isink = 6 mA |
| SCL clock rate | 20 | | | 400 | kHz | |

| Characteristic | Pin | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Charge pump output current | 16 | | | | | See Table 6.<br>Vpin16 = 2 V |
| Charge pump output leakage | 16 | | ±3 | ±10 | nA | Vpin16 = 2 V |
| Charge pump drive output current | 15 | 0.5 | | | mA | Vpin15 = 0.7 V |
| Crystal frequency | 17, 18 | 4 | | 16 | MHz | Application as in Figure 6. |
| Recommended crystal series resonance | | 10 | | 200 | Ω | 4 MHz parallel resonant crystal. |
| External reference input frequency | 17, 18 | 4 | | 20 | MHz | Sinewave coupled through 10 nF blocking capacitor. |
| External reference drive level | 18 | 0.2 | | 0.5 | Vpp | Sinewave coupled through 10 nF blocking capacitor. |
| Phase detector comparison frequency | | .03125 | | 0.25 | MHz | |
| Equivalent phase noise at phase detector | | | -158 | | | With 4 MHz crystal, SSB, within loop bandwidth.<br>With Fcomp = 125 kHz |
| RF division ratio | | 240 | | 32767 | | |
| Reference division ratio | | | | | | See Table 1. |
| Switching ports P0-P3<br>sink current<br>leakage current | 1, 5, 6, 14 | 10 | | <br><br>10 | <br>mA<br>μA | <br>Vport = 0.7 V<br>Vport = Vcc |
| Address select<br>Input high current<br>Input low current | 24 | | | <br>1<br>-0.5 | <br>mA<br>mA | See Table 4.<br>Vin=Vcc<br>Vin=Vee |

Notes

1 All power levels are referred to 50 Ω, and 0 dBm = 107 dBμV.

2 Total system with final load as in Figure 7, including an interstage IF shaping filter with IL of 2 dB and characteristic impedance of 200 Ω differential.

3 The specified gain is determined by the following formula;
Gs = Gm + Vtr where Gs = gain as specified
Gm = gain as measured with specified load conditions
Vtr = voltage transformation ratio of transformer as in Figure 7

4 Two input tones within RF operating range at -14 dBm from 50 Ω single ended source with 200 Ω differential output load. DC output current must be shunted to Vcc through suitable inductor, i.e. 10 μH.

5 Modulation spurs introduced on local oscillator through injection locking of the local oscillator by an undesired RF carrier.
Desired carrier at 80 dBμV, undesired carrier at 90 dBμV at an offset frequency of $f_d$ plus 42+$f_c$ MHz, where $f_d$ is desired carrier frequency, $f_c$ is US chrominance sub carrier and 42 equals 7 channel spacings.

6 All intermodulation specifications are measured with a single-ended input.

7 Operation range is defined as the region over which the oscillator presents a negative impedance.

8 Target to achieve 6 dB minimum S11.

## Absolute Maximum Ratings

All voltages are referred to Vee at 0 V.

| Characteristic | Min. | Max. | Units | Conditions |
|---|---|---|---|---|
| Supply voltage | -0.3 | 6 | V | |
| RF input voltage | | 117 | dBμV | Transient condition only. |
| All I/O port DC offsets | -0.3 | Vcc+0.3 | V | |
| Total port current | | 20 | mA | |
| Storage temperature | -55 | 150 | $^{o}$C | |
| Junction temperature | | 125 | $^{o}$C | Power applied. |
| Package thermal resistance, chip to ambient | | 27 | $^{o}$C/W | Package paddle soldered to ground. |
| Power consumption at 5.25V | | 1 | W | |
| ESD protection | 1 | | kV | Mil-std 883B method 3015 cat1 |

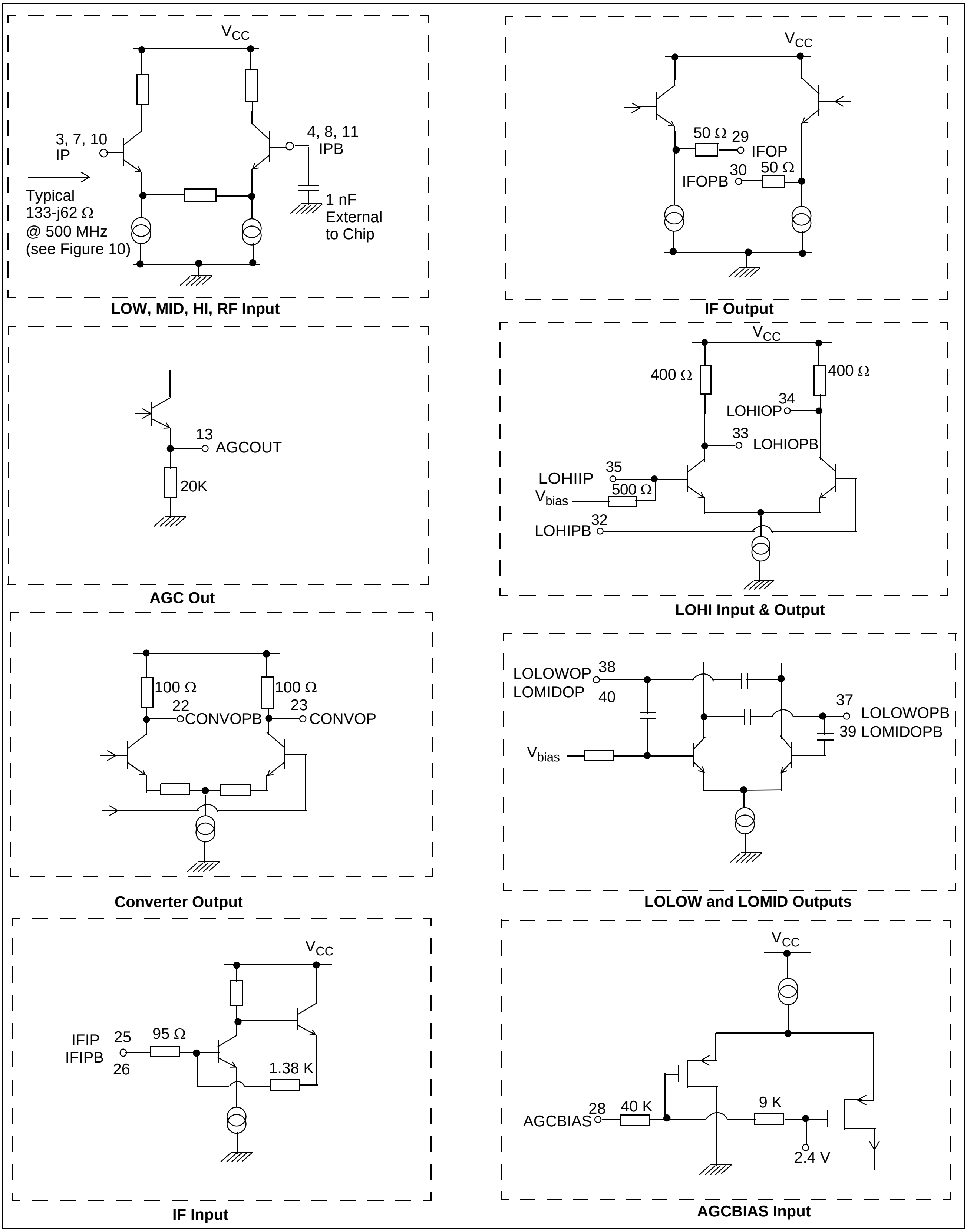



**Figure 19 - Input and Output Interface Circuits (RF Section)**

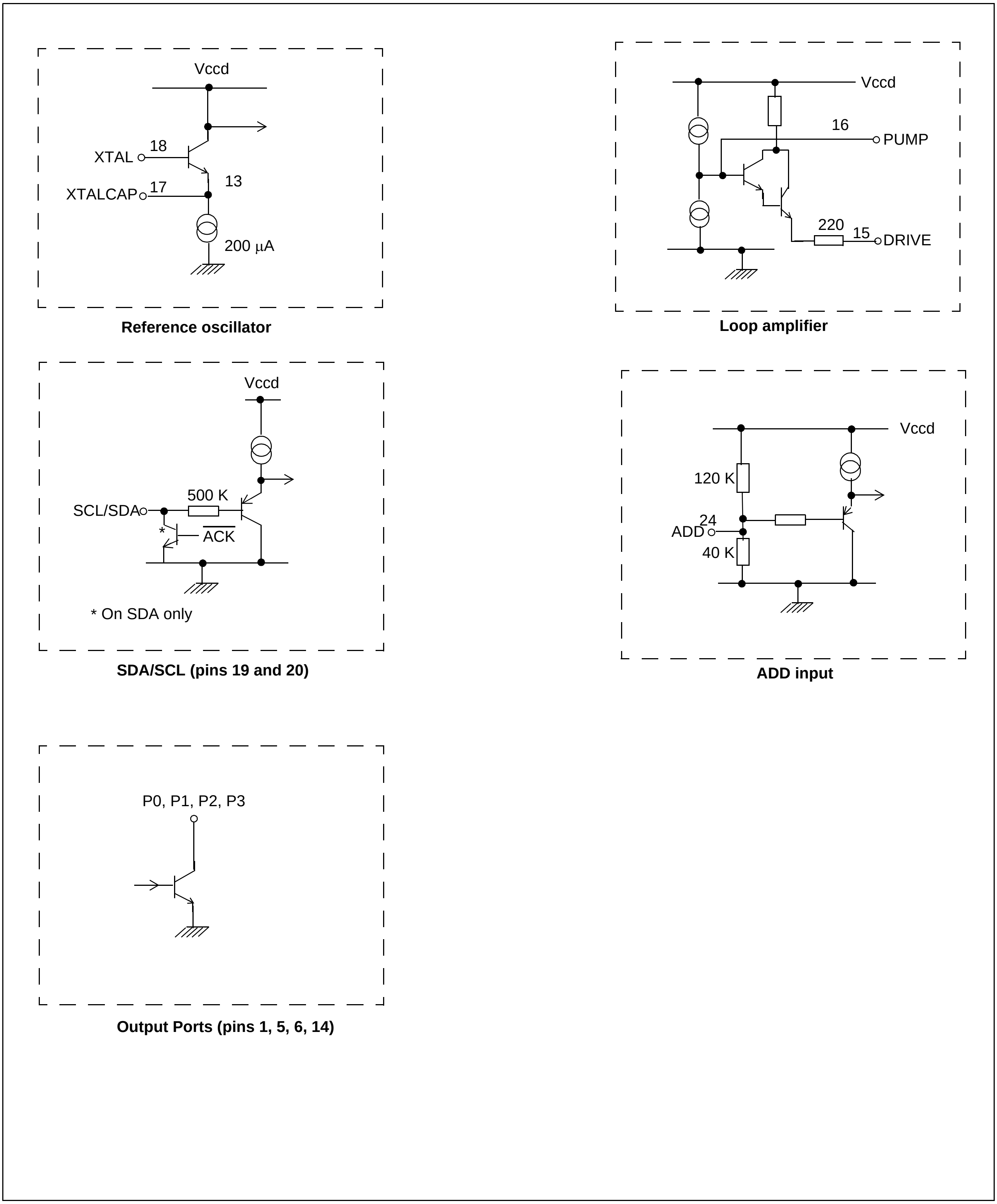
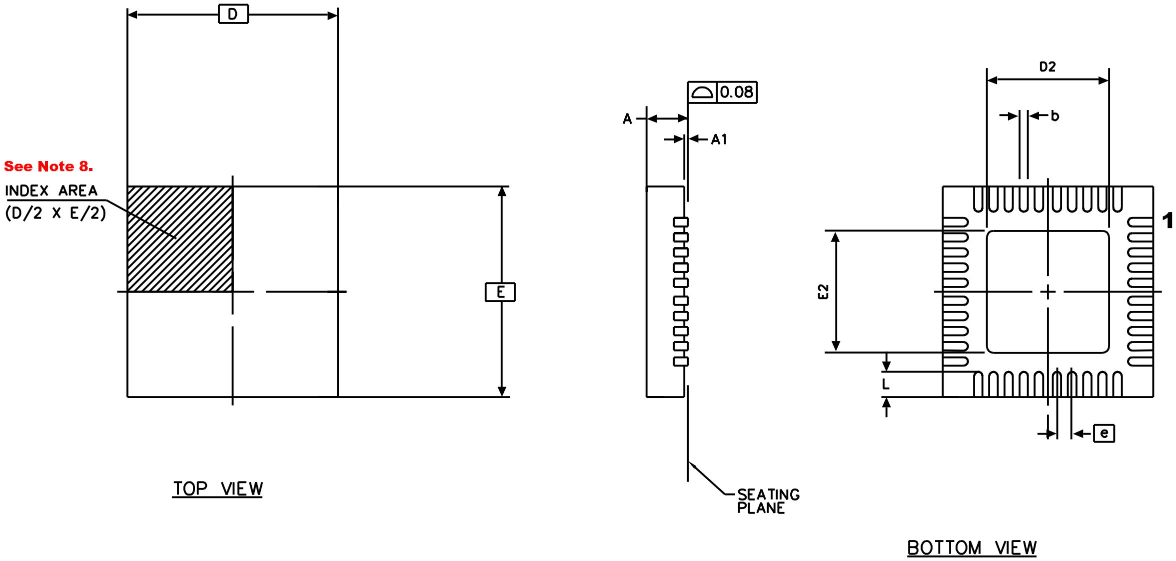



**Figure 20 - Input and Output Interface Circuits (PLL Section)**




| SYMBOL | COMMON DIMENSIONS MIN. | COMMON DIMENSIONS MAX. |
|---|---|---|
| A | – | 1.00 |
| A1 | 0.00 | 0.05 |
| b | 0.18 | 0.30 |
| D | 6.00 BSC | |
| D2 | 4.00 | 4.25 |
| E | 6.00 BSC | |
| E2 | 4.00 | 4.25 |
| N | 40 | |
| Nd | 10 | |
| Ne | 10 | |
| e | 0.50 BSC | |
| L | 0.30 | 0.50 |

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. LEAD COUNT IS 40.
6. PACKAGE WARPAGE MAX 0.08mm.
7. NOT TO SCALE.
8. TERMINAL #1 IDENTIFIER MUST BE LOCATED WITHIN THE ZONE INDICATED AND MAY BE EITHER A MOULD OR MARKED FEATURE.



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| ACN | 211246 | 212948 | | |
| DATE | 11Jul01 | 18Jun02 | | |
| APPRD. | | | | |

ZARLINK SEMICONDUCTOR

Package Code LC

Previous package codes LH

Package Outline for 40 lead MLP (6 x 6 x 0.9)mm

GPD00772

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