

TC74ACT374P, TC74ACT374F, TC74ACT374FW, TC74ACT374FT

OCTAL D - TYPE FLIP - FLOP WITH 3 - STATE OUTPUT

The TC74ACT374 is an advanced high speed CMOS OCTAL FLIP-FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input (\overline{OE}).




When the \overline{OE} input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

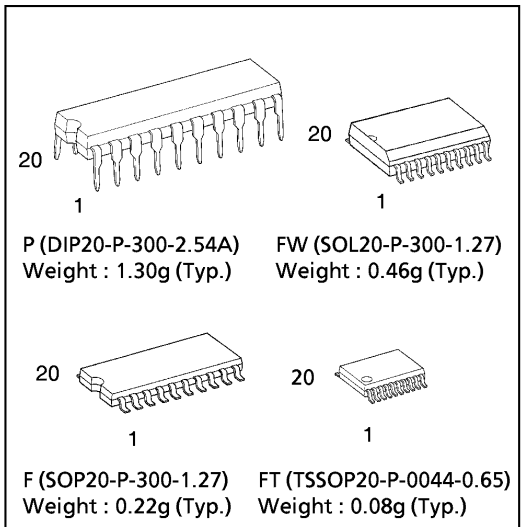
- High Speed..... $f_{MAX} = 180\text{MHz}$ (typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 8\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs..... $V_{IL} = 0.8\text{V}$ (Max.)
 $V_{IH} = 2.0\text{V}$ (Min.)
- Symmetrical Output Impedance..... $|I_{OH}| = I_{OL} = 24\text{mA}$ (Min.)
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74F374

TRUTH TABLE

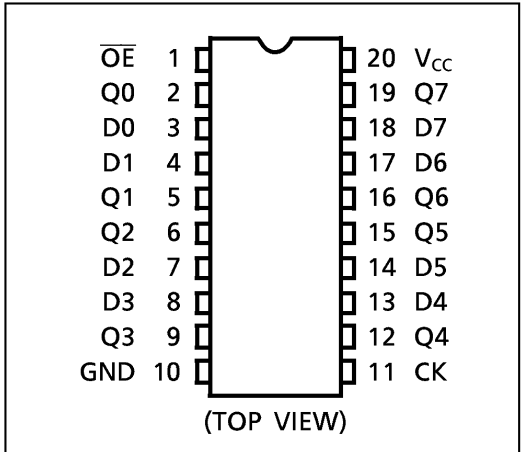
INPUTS			OUTPUTS
\overline{OE}	CK	D	Q
H	X	X	Z
L		X	Q_n
L		L	L
L		H	H

X : Don't Care
Z : High Impedance
 Q_n : No Change

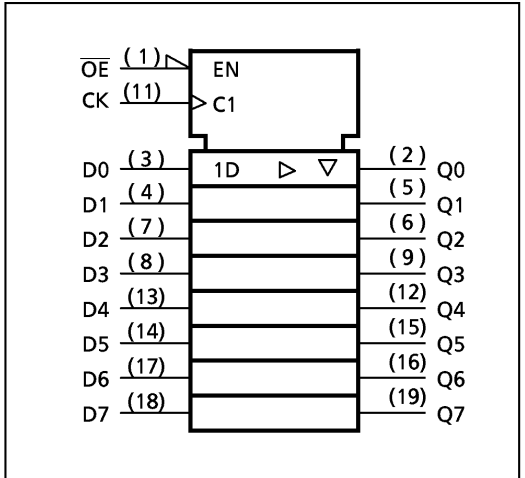
(Note) The JEDEC SOP (FW) is not available in Japan.



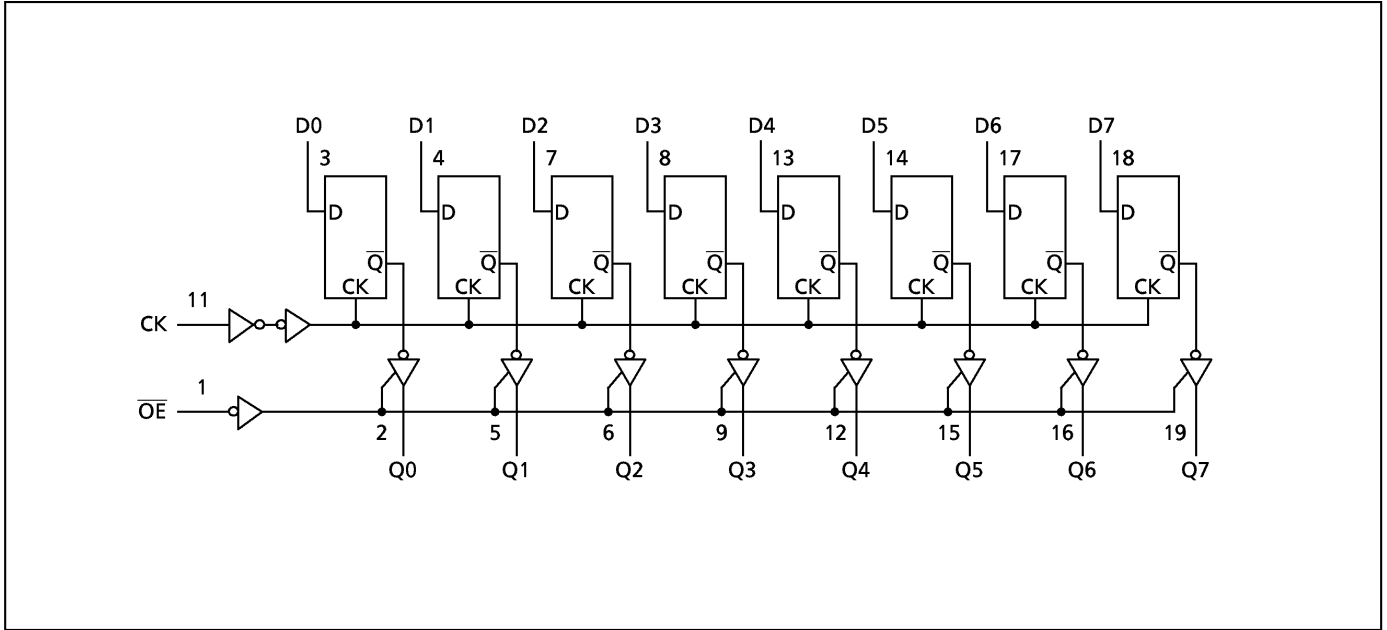
PIN ASSIGNMENT



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC} /Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt / dV	0~10	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		4.5 } 5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	V_{IL}		4.5 } 5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -24\text{mA}$	4.5	3.94	—	—	3.80	—	
			$I_{OH} = -75\text{mA}^*$	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\mu\text{A}$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 24\text{mA}$	4.5	—	—	0.36	—	0.44	
			$I_{OL} = 75\text{mA}^*$	5.5	—	—	—	—	1.65	
3 - State Output Off - State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	±0.5	—	±5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	±0.1	—	±1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	8.0	—	80.0		
	I_C	PER INPUT : $V_{IN} = 3.4\text{V}$ OTHER INPUT : V_{CC} or GND	5.5	—	—	1.35	—	1.5	mA	

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _{W(H)} t _{W(L)}		5.0 ± 0.5	5.0	5.0	5.0	ns
Minimum Set-up Time	t _s		5.0 ± 0.5	3.0	3.0	3.0	
Minimum Hold Time	t _h		5.0 ± 0.5	2.0	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT	
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.		MAX.
Propagation Delay Time (CK-Q)	t _{pLH} t _{pHL}		5.0 ± 0.5	—	6.1	9.6	1.0	11.0	ns
Output Enable Time	t _{pZL} t _{pZH}		5.0 ± 0.5	—	6.2	10.1	1.0	11.5	
Output Disable Time	t _{pLZ} t _{pHZ}		5.0 ± 0.5	—	5.6	7.9	1.0	9.0	
Maximum Clock Frequency	f _{MAX}		5.0 ± 0.5	95	160	—	95	—	MHz
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Output Capacitance	C _{OUT}			—	10	—	—	—	
Power Dissipation Capacitance	C _{PD} (1)			—	34	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 22 + 12 \cdot n$$

DIP 20PIN PACKAGE DIMENSIONS (DIP20-P-300-2.54A)

Unit in mm



SOP 20PIN (200mil BODY) PACKAGE DIMENSIONS (SOP20-P-300-1.27)

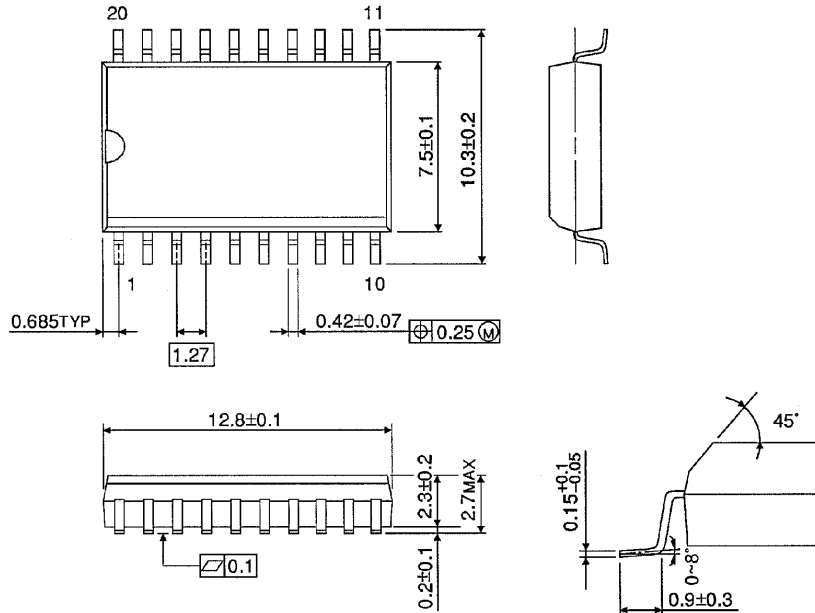
Unit in mm



SOP 20PIN (300mil BODY) PACKAGE DIMENSIONS (SOL20-P-300-1.27)

Unit in mm

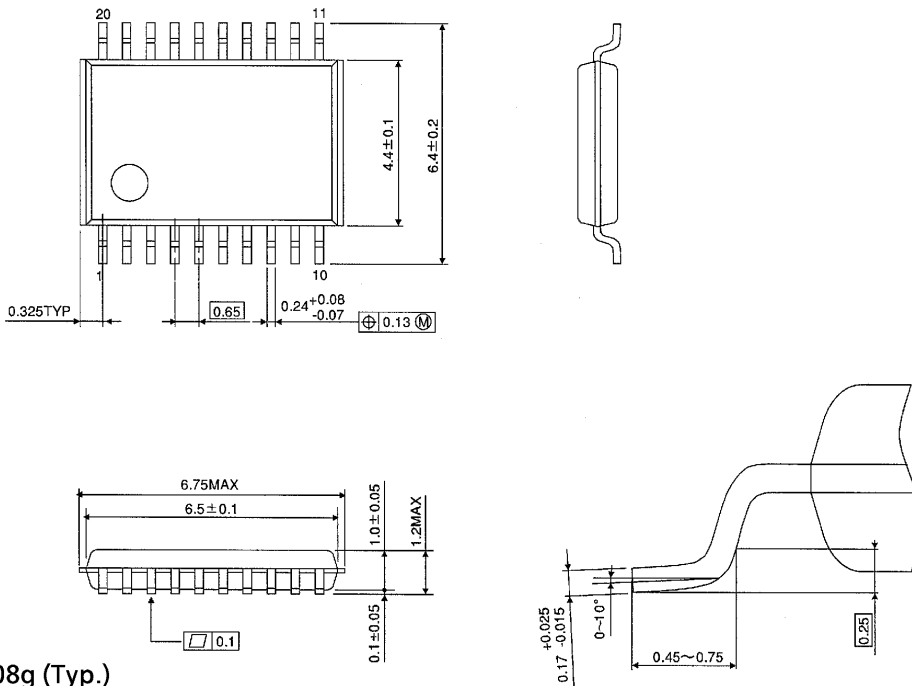
(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)

TSSOP 20PIN PACKAGE DIMENSIONS (TSSOP20-P-0044-0.65)

Unit in mm



Weight : 0.08g (Typ.)

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