**Integrated Circuit Systems, Inc.**

# ICS843071I
## FEMTOCLOCKS™ CRYSTAL-TO- LVPECL CLOCK GENERATOR

## GENERAL DESCRIPTION

The ICS843071I is a Serial ATA (SATA)/Serial Attached SCSI (SAS) Clock Generator and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS843071I uses an 18pF parallel resonant crystal over the range of 20.833MHz - 28.3MHz. For SATA/SAS applications, a 25MHz crystal is used and either 75MHz or 150MHz may be selected with the FREQ_SEL pin. The ICS843071I has excellent <1ps phase jitter performance, over the 12KHz - 20MHz integration range. The ICS843071I is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

## FEATURES

- (1) Differential LVPECL output

- Crystal oscillator interface, 18pF parallel resonant crystal (20.833MHz - 28.3MHz)

- Output frequency range: 62.5MHz - 170MHz

- VCO range: 500MHz - 680MHz

- RMS phase jitter @ 150MHz, using a 25MHz crystal (12KHz - 20MHz): 0.67ps (typical)

- 3.3V or 2.5V operating supply

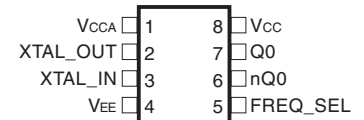- -40°C to 85°C ambient operating temperature

## COMMON CONFIGURATION TABLE - SERIAL ATA/SERIAL ATTACHED SCSI

| Inputs | | | | | Output Frequency (MHz) |
|---|---|---|---|---|---|
| Crystal Frequency (MHz) | FREQ_SEL | M | N | Multiplication Value M/N | |
| 25 | 0 | 24 | 4 | 6 | 150 |
| 25 | 1 | 24 | 8 | 3 | 75 |

## BLOCK DIAGRAM
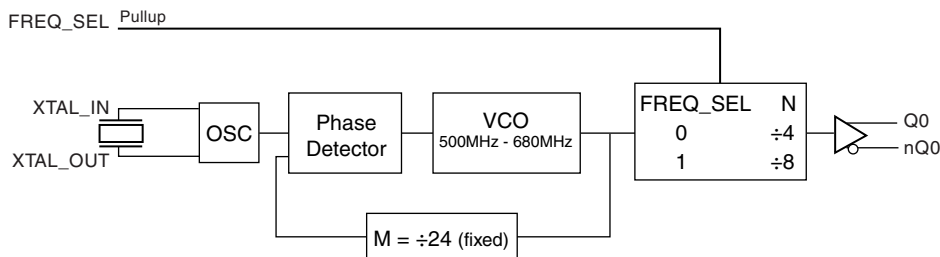


## PIN ASSIGNMENT



**ICS843071I**
**8-Lead TSSOP**
4.40mm x 3.0mm x 0.925mm package body
**G Package**
Top View

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**TABLE 1. PIN DESCRIPTIONS**

| Number | Name | Type | | Description |
|--------|------|------|------|-------------|
| 1 | $V_{CCA}$ | Power | | Analog supply pin. |
| 2, 3 | XTAL_OUT, XTAL_IN | Input | | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output. |
| 4 | $V_{EE}$ | Power | | Negative supply pin. |
| 5 | FREQ_SEL | Input | Pullup | Frequency select pin. LVCMOS/LVTTL interface levels. |
| 6, 7 | nQ0, Q0 | Output | | Differential clock outputs. LVPECL interface levels. |
| 8 | $V_{CC}$ | Power | | Core supply pin. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |

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### CLOCK GENERATOR

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5 V |
| Outputs, $I_O$ (LVDS) | |
|   Continuous Current | 10mA |
|   Surge Current | 15mA |
| Package Thermal Impedance, $\theta_{JA}$ | 101.7°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC}$ = $V_{CCA}$ = 3.3V±5%, T$_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | 58 | | mA |
| $I_{CCA}$ | Analog Supply Current | | | 7 | | mA |

**TABLE 3B. POWER SUPPLY DC CHARACTERISTICS,** $V_{CC}$ = $V_{CCA}$ = 2.5V±5%, T$_A$ = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $V_{CCA}$ | Analog Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| $I_{EE}$ | Power Supply Current | | | 55 | | mA |
| $I_{CCA}$ | Analog Supply Current | | | 7 | | mA |

**TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS,** $V_{CC}$ = $V_{CCA}$ = 3.3V±5% OR 2.5V±5%, T$_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 3.3V | 2 | | $V_{CC}$ + 0.3 | V |
| | | | 2.5V | 1.7 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | 3.3V | -0.3 | | 0.8 | V |
| | | | 2.5V | -0.3 | | 0.7 | V |
| $I_{IH}$ | Input High Current | FREQ_SEL | $V_{CC}$ = $V_{IN}$ = 3.465V or 2.625V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | FREQ_SEL | $V_{CC}$ = 3.465V or 2.625V, $V_{IN}$ = 0V | -150 | | | µA |

NOTE 1: Outputs terminated with 50Ω to $V_{CC}$/2. See Parameter Measurement Information Section, "Output Load Test Circuit" diagrams.

TABLE 3D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CC} = 3.3V\pm5\%$ OR $2.5V\pm5\%$, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CC}$ - 1.4 | | $V_{CC}$ - 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CC}$ - 2.0 | | $V_{CC}$ - 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC}$ - 2V.

TABLE 4. CRYSTAL CHARACTERISTICS

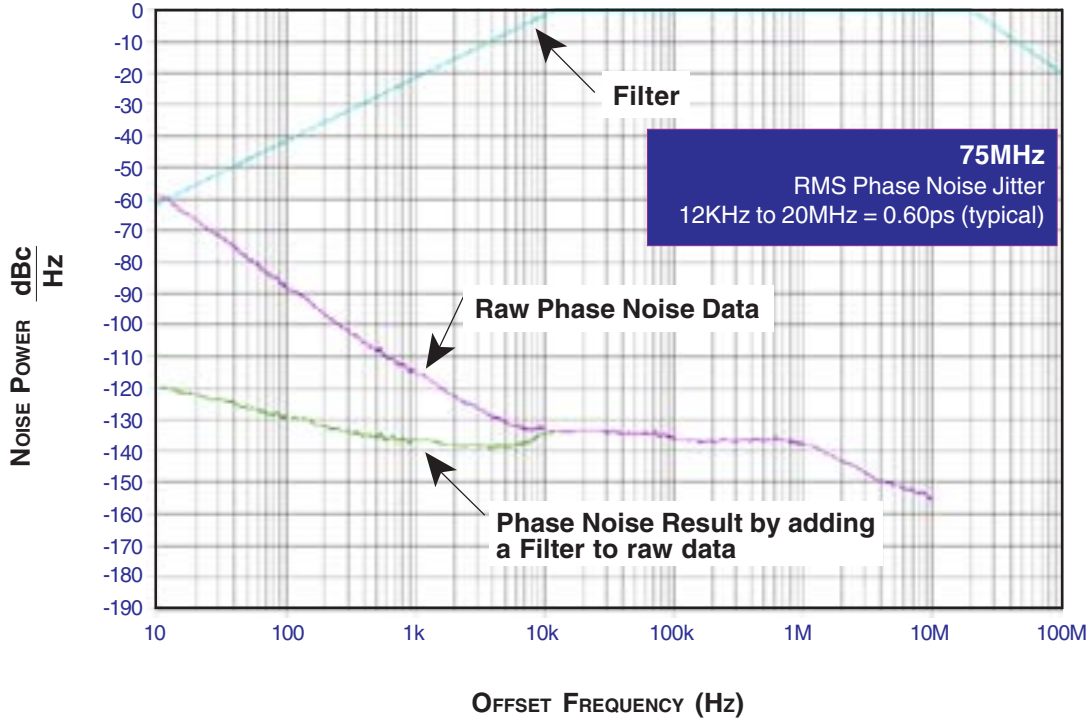| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-----------------|---------|---------|---------|-------|
| Mode of Oscillation | | | Fundamental | | |
| Frequency | | 20.833 | | 28.3 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V\pm5\%$, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $f_{OUT}$ | Output Frequency | | 62.5 | | 170 | MHz |
| $t$jit(Ø) | RMS Phase Jitter ( Random); NOTE 1 | 150MHz @ Integration Range: 12KHz - 20MHz | | 0.67 | | ps |
| | | 75MHz @ Integration Range: 12KHz - 20MHz | | 0.60 | | ps |
| $t_R / t_F$ | Output Rise/Fall Time | 20% to 80% | | 350 | | ps |
| odc | Output Duty Cycle | | | 50 | | % |

NOTE 1: Please refer to the Phase Noise Plots following this section.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 2.5V\pm5\%$, TA = -40°C TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------|-----------|-----------------|---------|---------|---------|-------|
| $f_{OUT}$ | Output Frequency | | 62.5 | | 170 | MHz |
| $t$jit(Ø) | RMS Phase Jitter ( Random); NOTE 1 | 150MHz @ Integration Range: 12KHz - 20MHz | | 0.78 | | ps |
| | | 75MHz @ Integration Range: 12KHz - 20MHz | | 0.75 | | ps |
| $t_R / t_F$ | Output Rise/Fall Time | 20% to 80% | | 350 | | ps |
| odc | Output Duty Cycle | | | 50 | | % |

NOTE 1: Please refer to the Phase Noise Plots following this section.

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## TYPICAL PHASE NOISE AT 75MHz



**75MHz**
RMS Phase Noise Jitter
12KHz to 20MHz = 0.60ps (typical)

Filter

Raw Phase Noise Data

Phase Noise Result by adding
a Filter to raw data

NOISE POWER $\frac{dBc}{Hz}$

OFFSET FREQUENCY (Hz)

## TYPICAL PHASE NOISE AT 150MHz



**150MHz**
RMS Phase Noise Jitter
12KHz to 20MHz = 0.67ps (typical)

Filter

Raw Phase Noise Data

Phase Noise Result by adding
a Filter to raw data

NOISE POWER $\frac{dBc}{Hz}$

OFFSET FREQUENCY (Hz)

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## PARAMETER MEASUREMENT INFORMATION



2V

$V_{CC}$

$Z = 50\Omega$

Qx

SCOPE

LVPECL

$50\Omega$

$V_{EE}$

$Z = 50\Omega$

nQx

$50\Omega$

-1.3V ± 0.165V
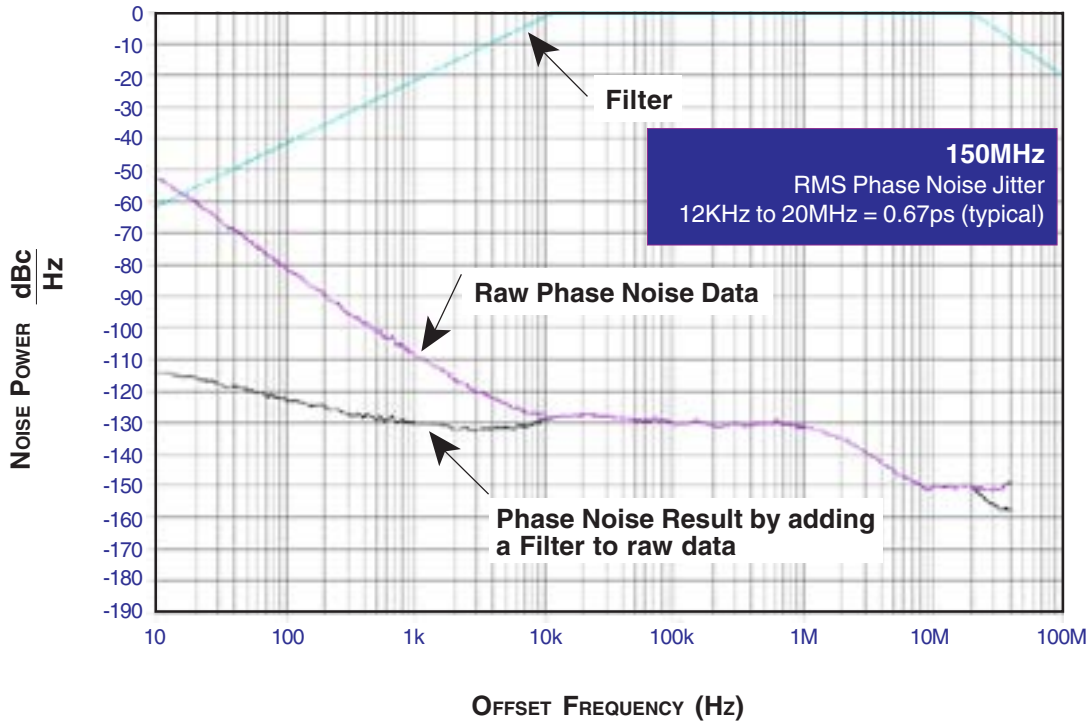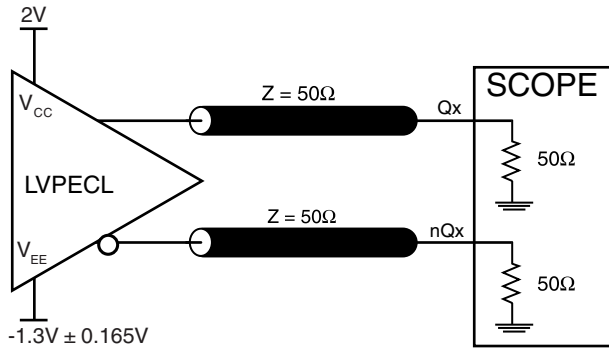
**LVPECL 3.3V OUTPUT LOAD AC TEST CIRCUIT**



2V

$V_{CC}$

$Z = 50\Omega$

Qx

SCOPE

LVPECL

$50\Omega$

$V_{EE}$

$Z = 50\Omega$

nQx

$50\Omega$

-0.5V ± 0.125V
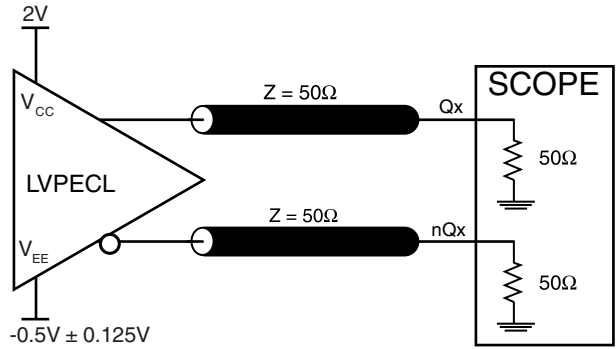
**LVPECL 2.5V OUTPUT LOAD AC TEST CIRCUIT**



80%          80%

$V_{SWING}$

Clock
Outputs     20%              20%

$t_R$          $t_F$

**OUTPUT RISE/FALL TIME**



nQ0

Q0
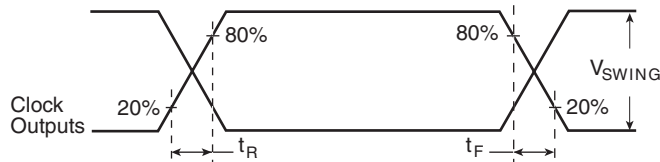
Pulse Width
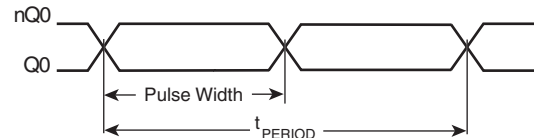
$t_{PERIOD}$

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



Phase Noise Plot

Noise Power

Phase Noise Mask

$f_1$     Offset Frequency     $f_2$
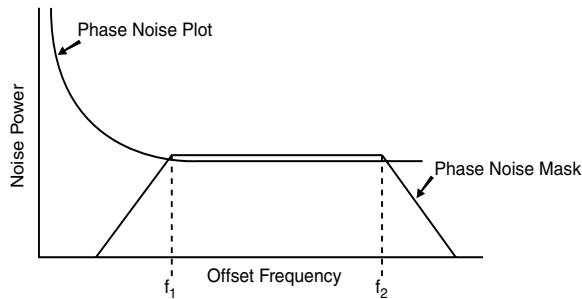
RMS Jitter = $\sqrt{\text{Area Under the Masked Phase Noise Plot}}$

**RMS PHASE JITTER**

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## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS843071I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{CC}$ and $V_{CCA}$ should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each $V_{CCA}$ pin.
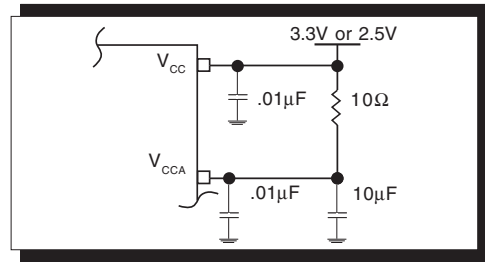


**FIGURE 1. POWER SUPPLY FILTERING**

### TERMINATION FOR 2.5V LVPECL OUTPUT

*Figure 2A* and *Figure 2B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC}$ - 2V. For $V_{CC}$ = 2.5V, the $V_{CC}$ - 2V is very close to ground level. The R3 in Figure 2B can be eliminated and the termination is shown in *Figure 2C*.
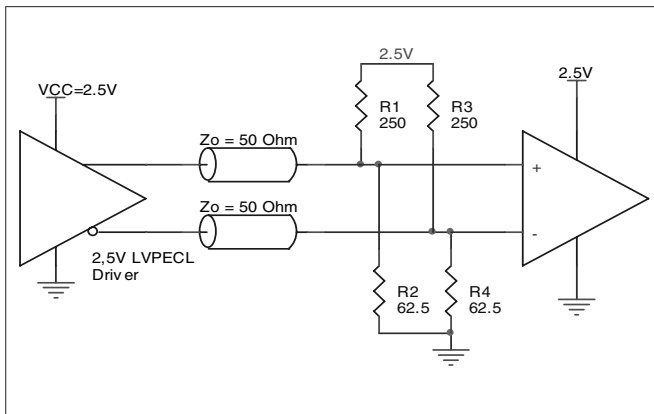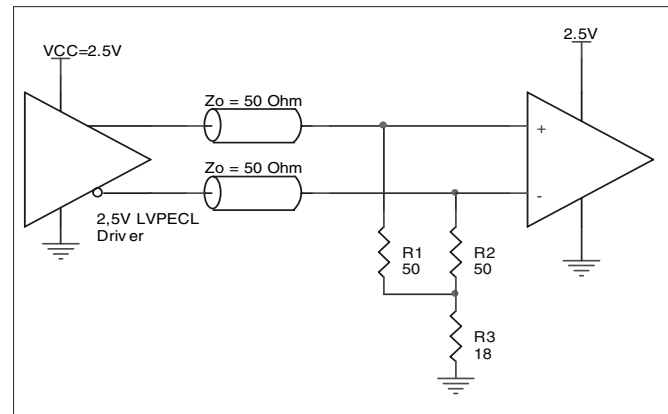


**FIGURE 2A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**
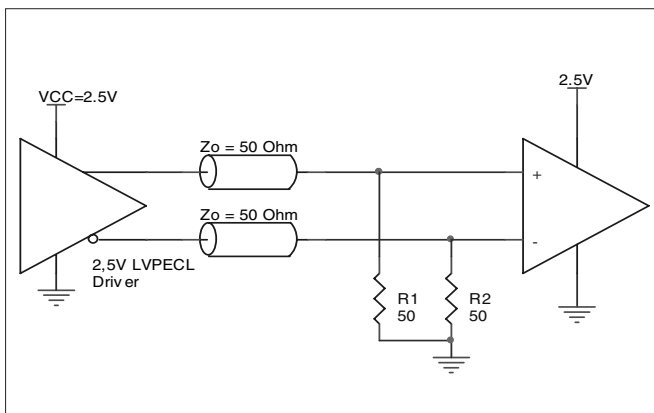


**FIGURE 2B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**



**FIGURE 2C. 2.5V LVPECL TERMINATION EXAMPLE**

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## TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.
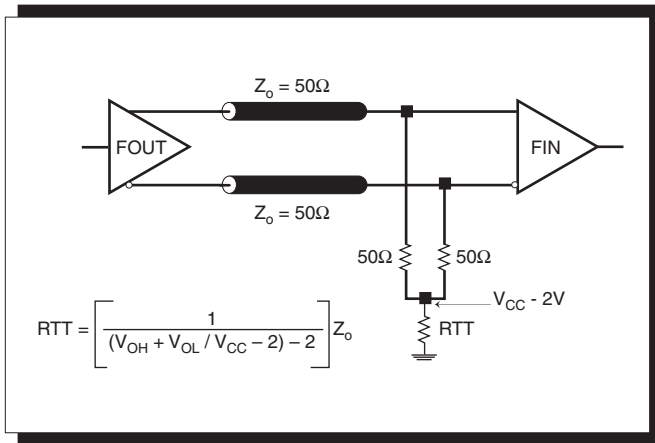


$$RTT = \left[ \frac{1}{(V_{OH} + V_{OL} / V_{CC} - 2) - 2} \right] Z_o$$

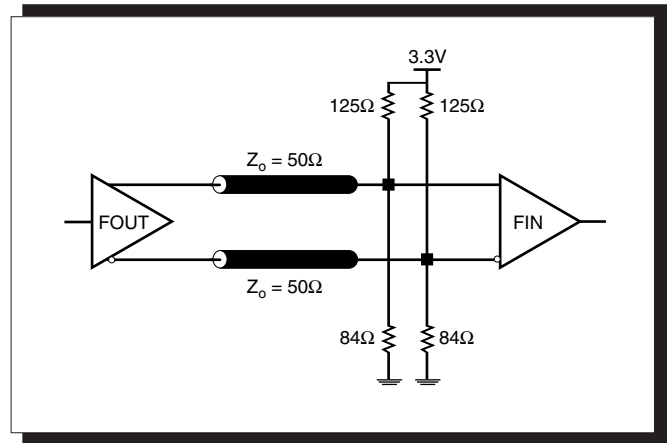**FIGURE 3A. LVPECL OUTPUT TERMINATION**



**FIGURE 3B. LVPECL OUTPUT TERMINATION**

## CRYSTAL INPUT INTERFACE

The ICS843071I has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 4* below were determined using a 25MHz, 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
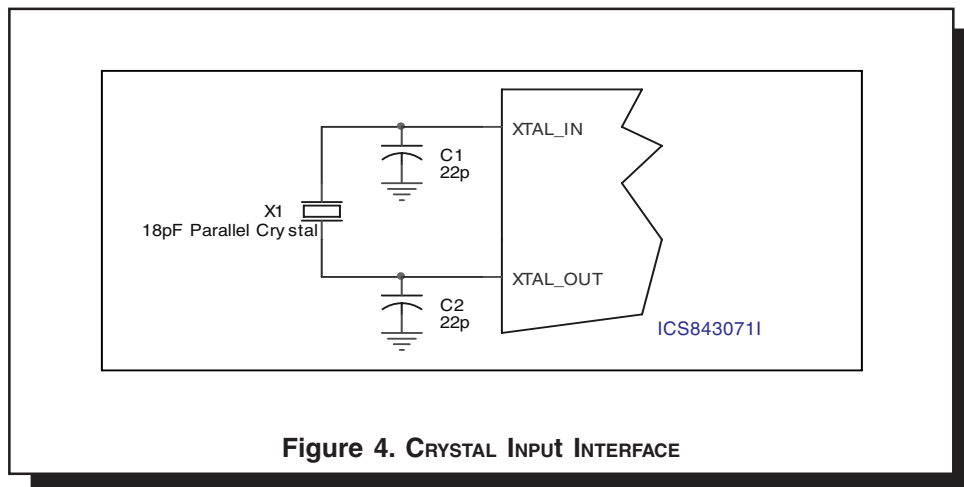


**Figure 4. CRYSTAL INPUT INTERFACE**

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# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS843071I. Equations and example calculations are also provided.

*1. Power Dissipation.*
The total power dissipation for the ICS843071I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.
**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_TYP}$ = 3.465V * 58mA = **200.97mW**

- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**

    **Total Power$_{\_MAX}$** (3.465V, with all outputs switching) = 200.97mW + 30mW = **230.97mW**

*2. Junction Temperature.*
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

   The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

   Tj = Junction Temperature

   $\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

   Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
   $T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
   85°C + 0.231W * 90.5°C/W = 106°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE $\theta_{JA}$ FOR 8-PIN TSSOP, FORCED CONVECTION**

| $\theta_{JA}$ by Velocity (Meters per Second) | | |
|---|---|---|
| **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards      101.7°C/W | 90.5°C/W | 89.8°C/W |

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*3. Calculations and Equations.*
The purpose of this section is to derive the power dissipated into the load.
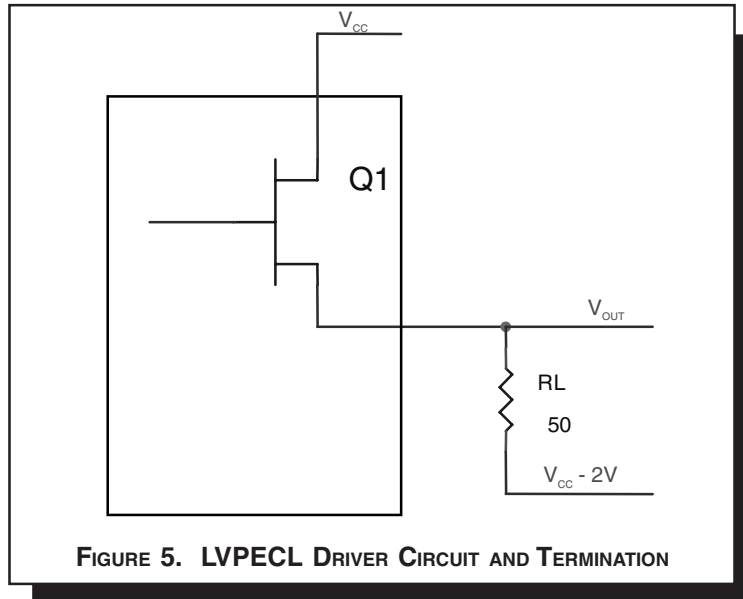LVPECL output driver circuit and termination are shown in *Figure 5.*



**FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50Ω] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50Ω] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

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# RELIABILITY INFORMATION

**TABLE 7.** $\theta_{JA}$ **VS. AIR FLOW TABLE FOR 8 LEAD TSSOP**

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

**TRANSISTOR COUNT**

The transistor count for ICS843071I is: 1732

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**PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP**
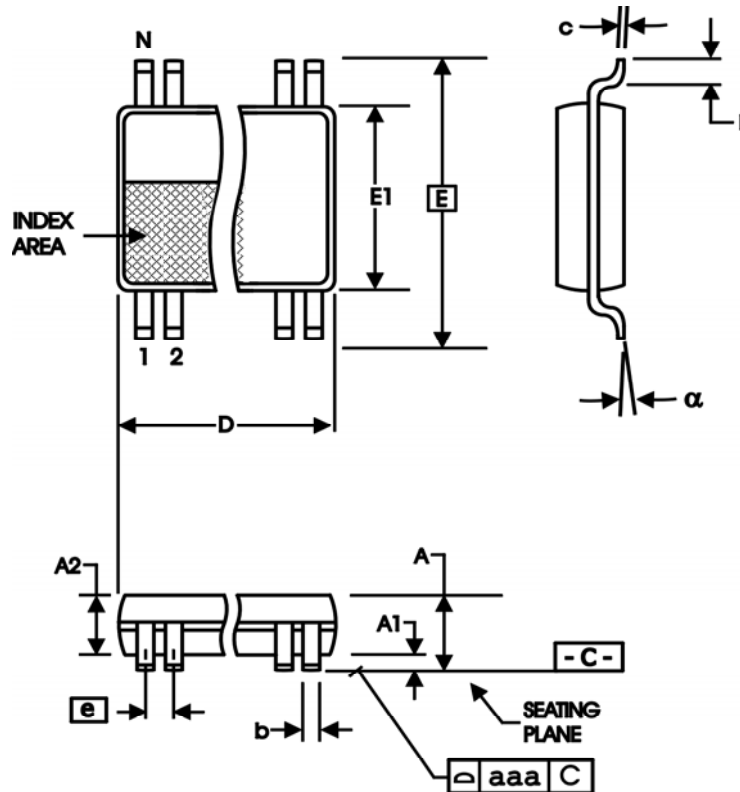
**TABLE 8. PACKAGE DIMENSIONS**

| SYMBOL | Millimeters | |
|---|---|---|
| | Minimum | Maximum |
| N | 8 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

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**TABLE 9. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| ICS843071AGI | 3071A | 8 Lead TSSOP | tube | -40°C to 85°C |
| ICS843071AGIT | 3071A | 8 Lead TSSOP | 2500 tape & reel | -40°C to 85°C |