



# FAST CMOS 16-BIT BIDIRECTIONAL TRANSCEIVER

**IDT74FCT166245T/AT**

## FEATURES:

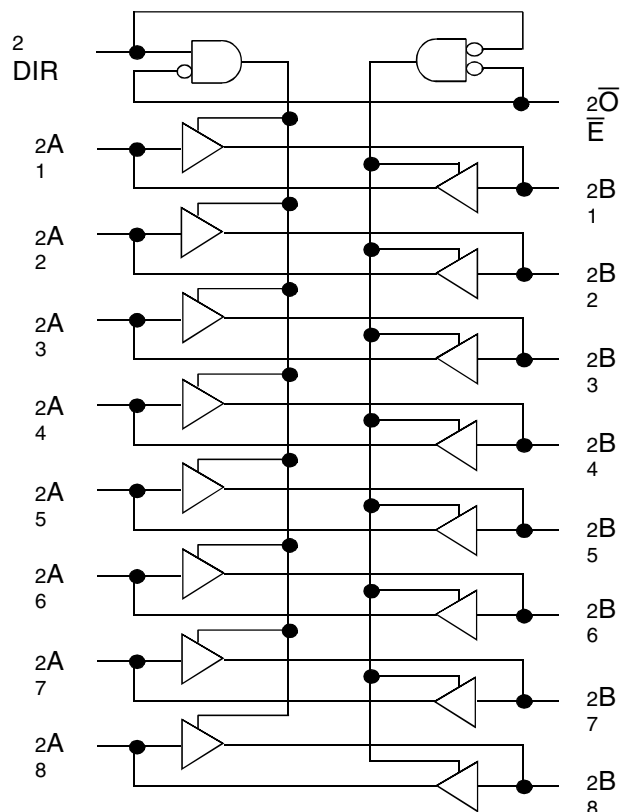
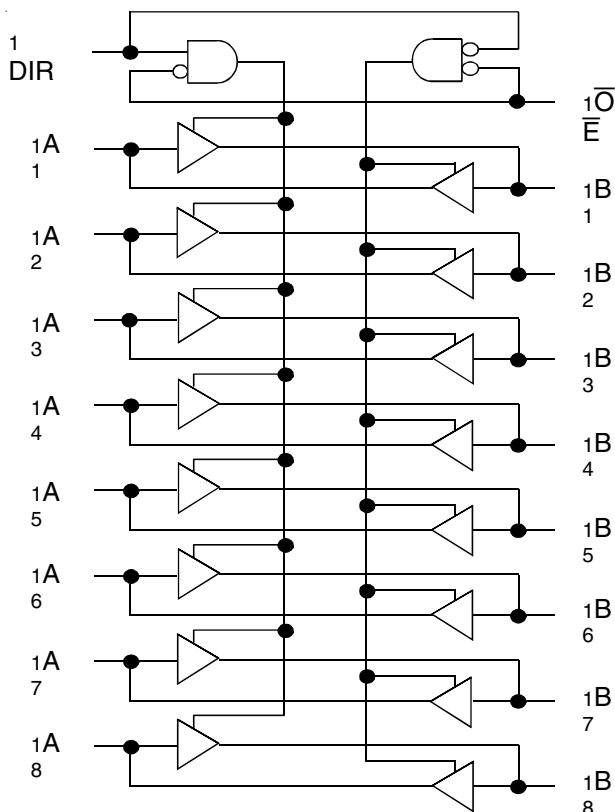
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Light drive A port:  $\pm 8mA$
- High drive B port: +64mA, -32mA
- Minimal system switching noise
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.25V at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$  (A port switching)
- Power off disable outputs permit "live insertion"
- Available in SSOP and TSSOP packages

## DESCRIPTION:

The FCT166245T 16-bit transceiver is built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two buses (A and B). The Direction and Output Enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin ( $\overline{xOE}$ ) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

The FCT166245T is suited for very low noise, point-to-point driving where there is a single receiver, or a light lumped load (<100pF). The buffers are designed to limit the output current to levels which will avoid noise and ringing on the signal lines without using external series terminating resistors. These parts have a  $\pm 8mA$  driver on the "A" Port and a +64/-32mA driver on the "B" Port, making them ideal for interfacing noisy system busses to noise sensitive interfaces.

## FUNCTIONAL BLOCK DIAGRAM

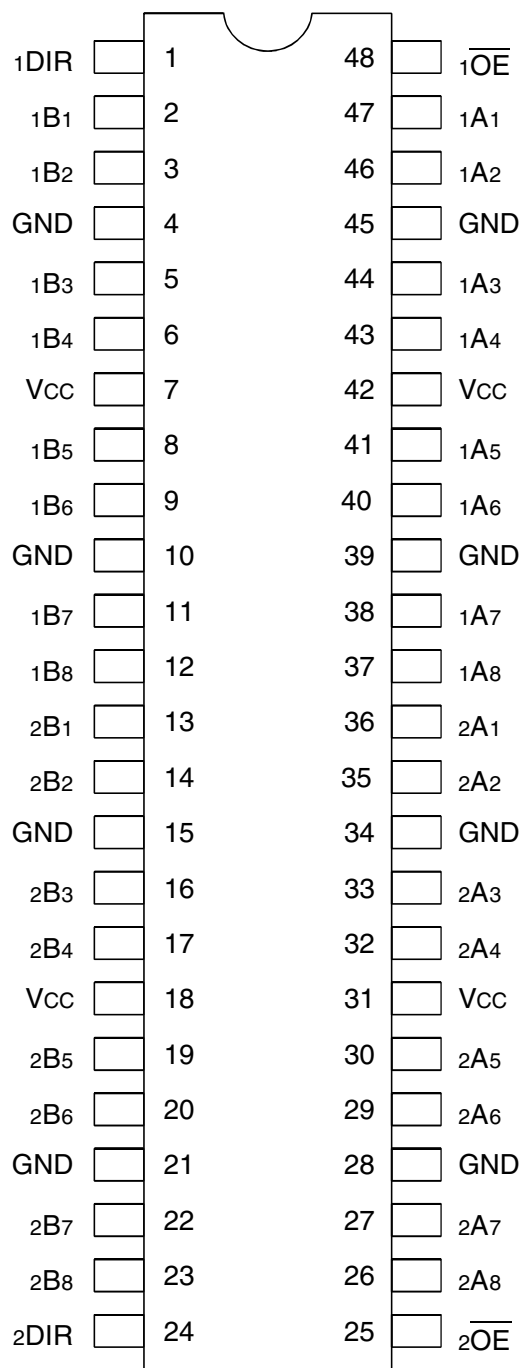


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

INDUSTRIAL TEMPERATURE RANGE

MAY 2001

PIN CONFIGURATION



SSOP/ TSSOP  
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX and FCT166XXX(A port) Output and I/O terminals.
- Output and I/O terminals for FCT162XXX and FCT166XXX(A port).

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6	pF
COUT	Output Capacitance	VOUT = 0V	3.5	8	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
xOE	3-State Output Enable Inputs (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs <sup>(1)</sup>
xBx	Side A Inputs or 3-State Outputs <sup>(2)</sup>

NOTES:

- This is the ±8mA port.
- This is the +64/-32mA port.

FUNCTION TABLE(1)

Inputs		Outputs
xOE	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Z

NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care  
Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins) <sup>(5)</sup>		$V_i = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_o = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_o = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$		-80	-140	-250	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} = \text{GND or } V_{CC}$		—	5	500	$\mu\text{A}$

## OUTPUT DRIVE CHARACTERISTICS (A-PORT)

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_{ODL}$	Output LOW Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_o = 1.5\text{V}^{(3)}$		16	48	96	mA
$I_{ODL}$	Output HIGH Current	$V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_o = 1.5\text{V}^{(3)}$		-16	-48	-96	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
$V_{OH}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 8\text{mA}$	—	0.3	0.55	V

## OUTPUT DRIVE CHARACTERISTICS (B-PORT)

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_o$	Output Drive Current	$V_{CC} = \text{Max.}, V_o = 2.5\text{V}^{(3)}$		-50	—	-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -15\text{mA}$	2.4	3.5	—	
			$I_{OH} = -32\text{mA}^{(4)}$	2	3	—	
$V_{OH}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.2	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_o \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $\overline{xOE} = xDIR = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu\text{A}/\text{MHz}$
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ , Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xOE} = xDIR = \text{GND}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

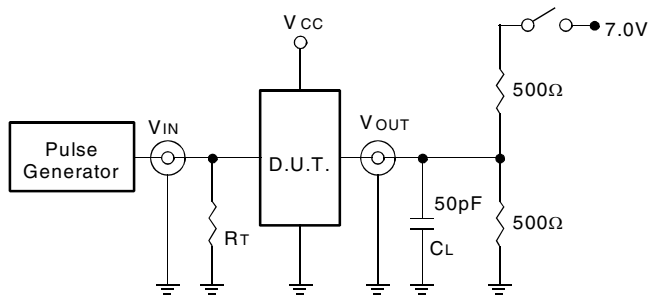
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	FCT166245T		FCT166245AT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay A to B	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	4.6	1.5	4.1	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay B to A		1.5	7	1.5	4.6	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time x $\overline{O\!E}$ to B		1.5	6.2	1.5	5.8	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time x $\overline{O\!E}$ to A		1.5	9.5	1.5	6.2	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time x $\overline{O\!E}$ to B		1.5	5	1.5	4.8	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time x $\overline{O\!E}$ to A		1.5	7.5	1.5	5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time DIR to B <sup>(3)</sup>		1.5	6.2	1.5	5.8	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time DIR to A <sup>(3)</sup>		1.5	9.5	1.5	6.2	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time DIR to B <sup>(3)</sup>		1.5	5	1.5	4.8	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time DIR to A <sup>(3)</sup>		1.5	7.5	1.5	5	ns
t <sub>SK(o)</sub>	Output Skew <sup>(4)</sup>		—	0.5	—	0.5	ns

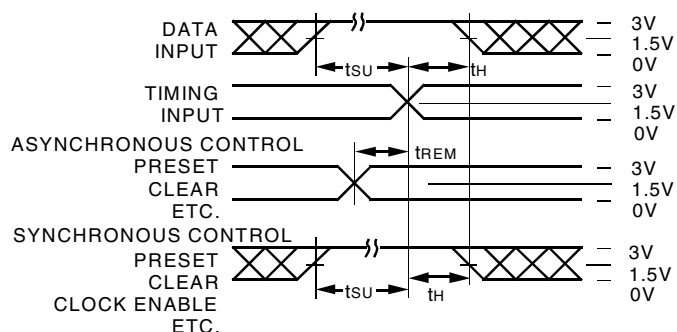
**NOTES:**

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

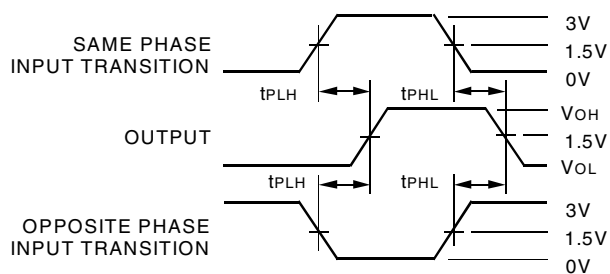
## TEST CIRCUITS AND WAVEFORMS



*Test Circuits for All Outputs*



*Set-up, Hold, and Release Times*



*Propagation Delay*

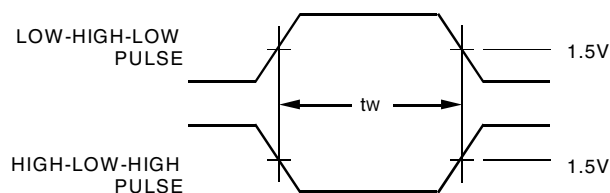
## SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

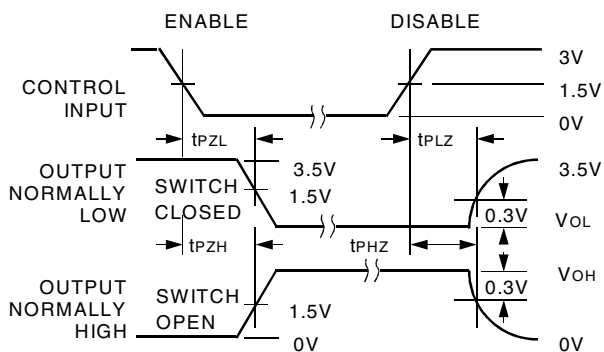
### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to Zout of the Pulse Generator.



*Pulse Width*

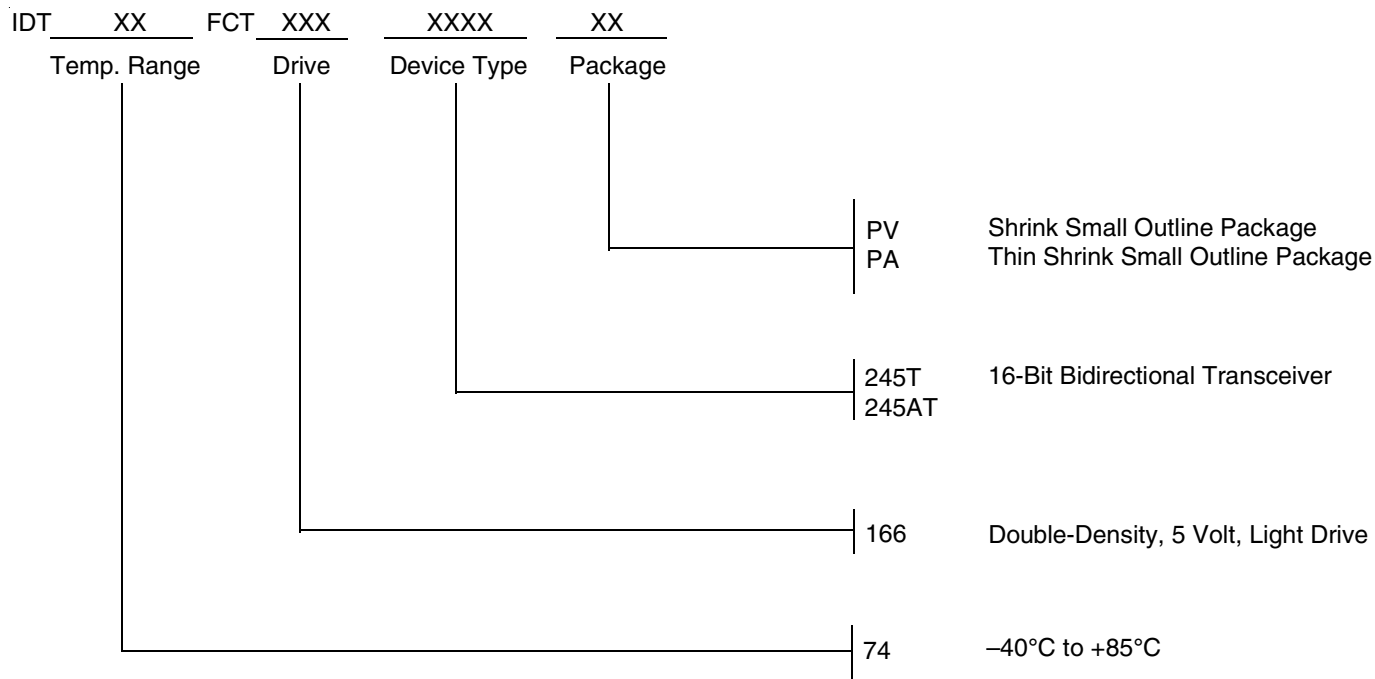


*Enable and Disable Times*

### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_f \leq 2.5\text{ns}$ .

ORDERING INFORMATION



**CORPORATE HEADQUARTERS**  
 2975 Stender Way  
 Santa Clara, CA 95054

**for SALES:**  
 800-345-7015 or 408-727-6116  
 fax: 408-492-8674  
 www.idt.com

**for Tech Support:**  
 logichelp@idt.com  
 (408) 654-6459