Ordering number : EN3201

CMOS LSI

SANYO No.3201A

# LC7991M

## Constant-Speed DC Motor Controller



### Overview

The Sanyo LC7991M is a PLL-type speed controller for constant-speed DC motors. It incorporates a crystal oscillator to provide highly-accurate speed control. Internal frequency dividers support a wide range of motor speeds from low-speed gear motors to high-speed polygon mirror motors. Integrated DACs and a phase comparator allow implementation of a DC motor control system with a minimum of external components.

Applications for the LC7991M include drum, paper feed and scanner motors for plain paper copiers, laser facsimile equipment, laser printers, as well as motors for floppy, hard and optical disk drives.

The LC7991M operates from a single 5V supply, and is available in 16-pin plastic DIPs.

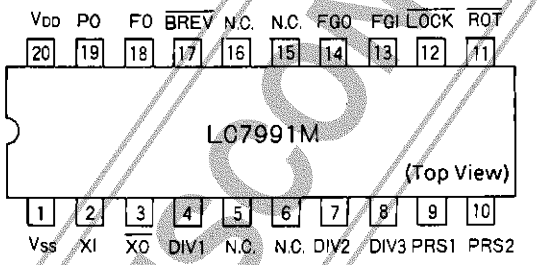
### Features

- Wide 200 to 2500Hz operating frequency range (FGI input)
- Low-impedance phase and frequency control outputs
- Speed lock indicator output directly drives an external LED.
- TTL-compatible motor frequency sensor and run/stop control inputs
- CMOS process
- Single 5V supply

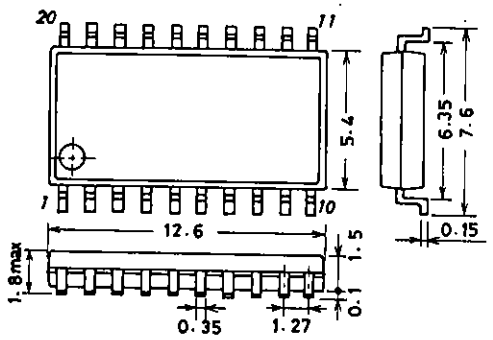
### Absolute Maximum Ratings at Ta = 25°C, $V_{CC}$ = 0V

| | | | | unit |
|---|---|---|---|---|
| Maximum Supply Voltage | $V_{DD}$ max | | −0.3 to +7.0 | V |
| Input Voltage | $V_{IN}$ | | −0.3 to $V_{DD}$+0.3 | V |
| Output Voltage | $V_{OUT}$ | | −0.3 to $V_{DD}$+0.3 | V |
| Output Current | $I_{OUT}$ | | ±20 | mA |
| Allowable Power Dissipation | Pd max | Ta = −30 to +75°C | 300 | mW |
| Operating Temperature | Topr | | −30 to +75 | °C |
| Storage Temperature | Tstg | | −55 to +125 | °C |

### Pin Assignment




**Package Dimensions** 3036B-IC
**( unit: mm )**




SANYO: MFP20

**Allowable Operating Conditions** at Ta = −30 to +75°C, $V_{SS}$ = 0V

| | | min | typ | max | unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 4.5 | 5 | 5.5 | V |
| Input Voltage | $V_{IN}$ | 0 | | $V_{DD}$ | V |
| Output Voltage | $V_{OUT}$ | 0 | | $V_{DD}$ | V |

**Electrical Characteristics** at Ta = 25°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V

| | | | min | typ | max | unit |
|---|---|---|---|---|---|---|
| Input 'H'-Level Voltage | $V_{IH}$ | [DIV1 to 3, PRS1, PRS2, $\overline{ROT}$, FGI inputs] | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| Input 'L'-Level Voltage | $V_{IL}$ | | 0 | | 0.3$V_{DD}$ | V |
| Input 'H'-Level Current | $I_{IH}$ | [DIV1 to 3, PRS1, PRS2 inputs] | | | 1 | μA |
| Input 'L'-Level Current | $I_{IL}$ | | −1 | | | μA |
| Input 'H'-Level Current | $I_{IH}$ | [$\overline{ROT}$, FGI inputs (pull-up 10kΩ)] | | | 1 | μA |
| Input 'L'-Level Current | $I_{IL}$ | | −500 | | | μA |
| Output 'H'-Level Current | $I_{OH}$ | [$\overline{LOCK}$, $\overline{BREV}$, FGO outputs] $V_{OH}$ = $V_{DD}$ − 0.4V | | | −2 | mA |
| Output 'L'-Level Current | $I_{OL}$ | $V_{OL}$ = 0.4V | 2 | | | mA |
| Maximum Non-Linearity (DA Converter) | − | [FO, PO outputs, output open] | | +1 | +3 | LSB |
| | | | | −2 | −6 | LSB |
| Output Resistance | $R_O$ | FO, PO outputs, $R_L$ = 10kΩ | | | 1000 | Ω |
| Current Dissipation | $I_{DD}$ | | | | 20 | mA |

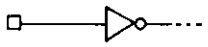
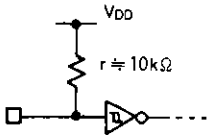
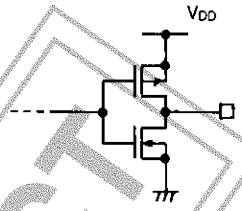
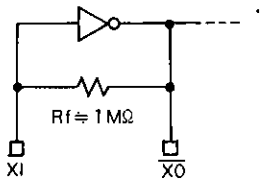
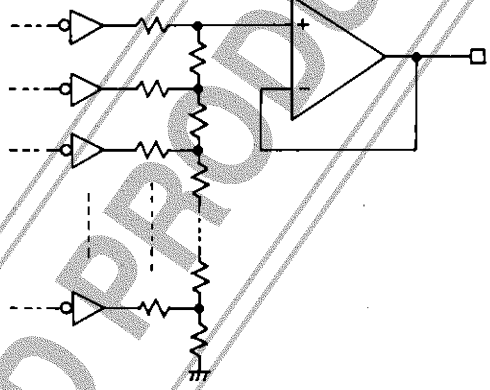
**AC Characteristics** at Ta = 25°C, $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V

| | | | min | typ | max | unit |
|---|---|---|---|---|---|---|
| Input Frequency | $f_{XI}$ | XI input | 0.1 | | 10.5 | MHz |
| | $f_{FG}$ | FGI input | | | 50 | kHz |
| FG Lock Frequency | $f_{FG\,LOOK}$ | FGI input, FG divider off | 200 | | 2500 | Hz |
| | $f_{FG\,LOOK}$ | FGI input, FG divider on | 400 | | 5000 | Hz |

**Pin Descriptions**

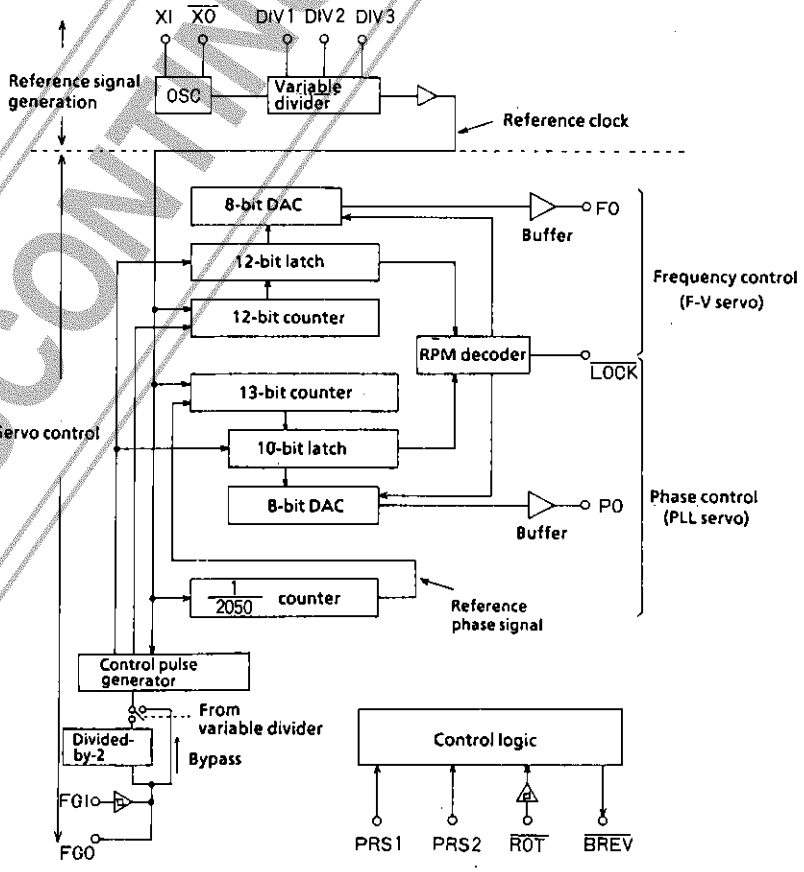
| Pin No. | Pin Name | Description | Input/Output |
|---|---|---|---|
| 1 | $V_{SS}$ | Ground (0V) | – |
| 2 | XI | Crystal oscillator | OSC circuit |
| 3 | $\overline{XO}$ | | |
| 4 | DIV1 | Variable frequency divider ratio select (FG divider on /off) | Input |
| 5 | N.C. | No connection | – |
| 6 | N.C. | | |
| 7 | DIV2 | Variable frequency divider ratio select (FG divider on /off) | Input |
| 8 | DIV3 | | |
| 9 | PRS1 | Phase comparison range select | Input |
| 10 | PRS2 | | |
| 11 | $\overline{ROT}$ | Rotate/halt control H : halt L : rotate | Pull-up · Schmitt input |
| 12 | $\overline{LOCK}$ | Lock output. LOW during lock. Can directly drive an external LED. | Output |
| 13 | FGI | Motor sensor FG input | Pull-up · Schmitt input |
| 14 | FGO | FG shaped output | Output |
| 15 | N.C. | No connection | – |
| 16 | N.C. | | |
| 17 | $\overline{BREV}$ | Brake timing output, LOW during braking. | Output |
| 18 | FO | Frequency control output, buffered by internal op-amp | DAC output |
| 19 | PO | Phase control output, buffered by internal op-amp | |
| 20 | $V_{DD}$ | Positive power supply (5V) | – |

## Pin Internal Circuits

| Input | Pull-up Schmitt-trigger input | Output (complementary) |
|---|---|---|
|  |   |   |
| **Crystal oscillator** | **DAC output** | |
|   |  | |



## Block Diagram



## Functional Descriptions

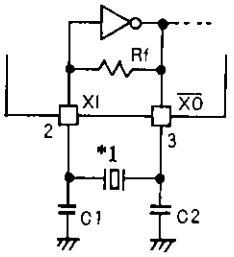
### 1. Reference Signal Generation

(1) Reference oscillator

The internal oscillator is used by connecting a crystal or a ceramic resonator between the XI and $\overline{XO}$ pins, and load capacitors to both XI and $\overline{XO}$, as shown in Fig. 1.

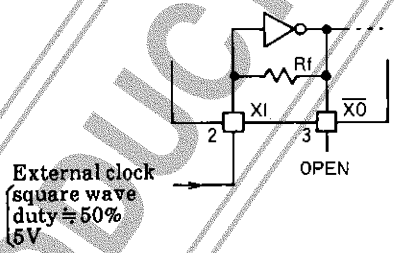
Alternatively, an externally generated clock may be used by leaving $\overline{XO}$ open, and applying the clock to the XI pin, as shown in Fig.2. The clock signal should be 5V in amplitude, with a duty cycle of approximately 50%.

Fig. 1 Internal Oscillator




*1 Crystal or ceramic resonator

Fig. 2 External Generated Clock




(2) Variable divider and FG divider

The LC7991M incorporates both a five-range selectable divider and a by-passable divide-by-2 circuit for FGI input. These dividers both increase motor speed lock range and simplify selection of a motor speed sensor encoder and oscillator crystal. The division ratio is selected by the DIV1 to DIV3 inputs, as shown in Table 1 below.

Table 1. Divider Control

| Control Input | | | Division Ratio (DIV) | FG Divider |
|---|---|---|---|---|
| DIV3 | DIV2 | DIV1 | | |
| H | H | H | 20 | OFF |
| H | H | L | 10 | OFF |
| H | L | H | 6 | OFF |
| H | L | L | 3 | OFF |
| L | H | H | 2 | OFF |
| L | H | L | Test mode | |
| L | L | H | 2 | ON |
| L | L | L | Test mode | |

H : High level
L : Low level
OFF : Bypass
ON : Divided-by-2

(3) Crystal/clock frequency selection

The required reference clock frequency is determined from the lock frequency $f_{FG\,Lock}$ and the division ratio DIV.

If the FG divider is bypassed,

$fxtal = f_{FG\,Lock} \times DIV \times 2050$ (Hz)

If the FG divider is selected,

$fxtal = f_{FG\,Lock} \times DIV \times 1025$ (Hz)

The available lock frequencies for different clock frequencies are shown below in Table 2. Readily available ceramic resonator include the MURATA CSA6.14MT for 500, 1000 and 1500Hz operation, and the MURATA CSA8.20MT for 2000Hz operation.

Table 2. Clock Frequency and Lock Frequency

| Division Ratio | FG Divider | Clock Frequency (MHz) | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | 2.05 | 4.1 | 6.15 | 8.2 | 10.25 | |
| 20 | OFF | 50 | 100 | 150 | 200 | 250 | Hz |
| 10 | | 100 | 200 | 300 | 400 | 500 | |
| 6 | | 167 | 333 | 500 | 667 | 833 | |
| 3 | | 333 | 667 | 1000 | 1333 | 1667 | |
| 2 | | 500 | 1000 | 1500 | 2000 | 2500 | |
| | ON | 1000 | 2000 | 3000 | 4000 | 5000 | |

## 2. Servo Controller

The servo controller compares the reference clock and the motor input frequency signal on pin FGI with control motor speed. FGI is a Schmitt-trigger input. The frequency control output FO and the phase control output PO are output via the 8-bit DA converters. The $\overline{\text{LOCK}}$ output indicates that the motor is within the lock range.

(1) Servo action

Servo action is divided into drive, tracking and braking operation. Tracking operation takes place when motor speed is within 6% of the desired speed. FO and PO act to bring the motor into sync. If the motor is underspeed, both FO and PO go HIGH to accelerate the motor. If the motor is overspeed, FO and PO both go LOW to break the motor.

Servo action and the operation of the $\overline{\text{LOCK}}$, FO and PO outputs for the three modes of operation is summarized in Table 3. The lock frequency $f_{FG\ Lock}$ is defined as

$$f_{FG\ Lock} = \frac{f_{Xtal}}{DIV \times 2050} \quad ; \text{FG divider off}$$

$$f_{FG\ Lock} = \frac{f_{Xtal}}{DIV \times 1025} \quad ; \text{FG divider on}$$

where DIV is the variable divider ratio, and $f_{Xtal}$ is the crystal oscillator or external input clock frequency.

Table 3. Servo Action

| FG Input Frequency | Mode | $\overline{\text{LOCK}}$ Output | FO Output | PO Output |
|---|---|---|---|---|
| Overspeed : $> f_{FG\ Lock} + 6\%$ | Braking | HIGH | LOW | LOW |
| Tracking range : $f_{FG\ Lock} \pm 6\%$ | Tracking | LOW | Analog frequency output | Analog phase output |
| Underspeed $< f_{FG\ Lock} - 6\%$ | Drive | HIGH | HIGH | HIGH |

(2) Phase and frequency control

When the motor frequency comes within 6% of the target frequency, FO and PO are switched to the outputs of the internal 8-bit DACs. Each DAC has 256 steps between logic-LOW and logic-HIGH. FO is controlled by the motor speed, and PO by the difference in phase between the internal reference clock and FGI input signal (the motor signal input phase). The output characteristics are shown in Figs. 3 and 4.

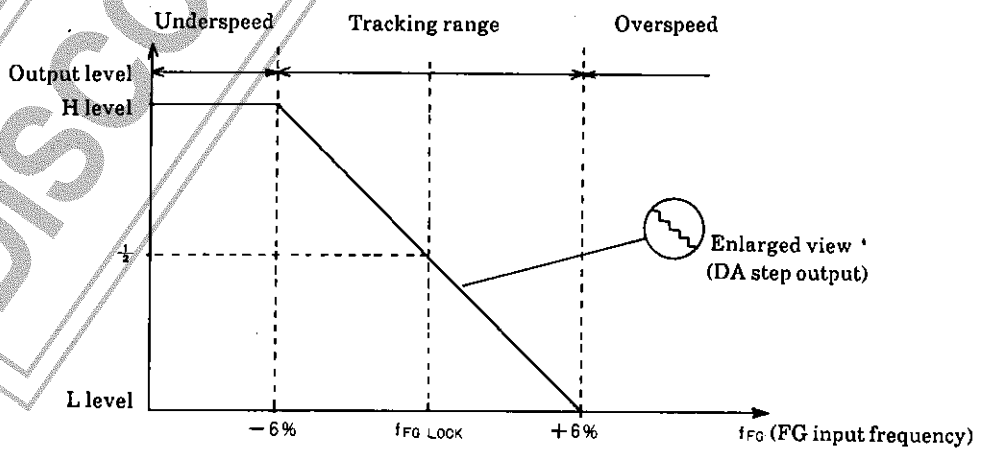



Fig.3 FO Output Characteristic

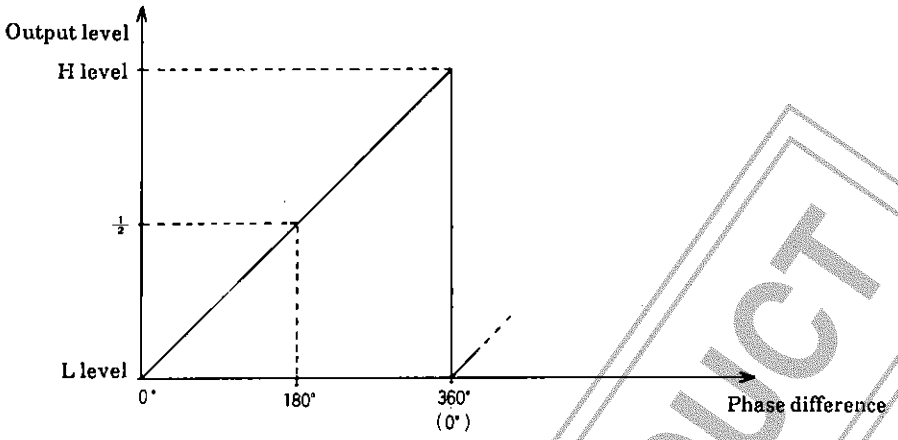



Fig.4 PO Output Characteristic, ×2 Range

### 3. Rotate Control & Brake Timing Output

The $\overline{ROT}$ active-LOW input may be used to control the motor. When $\overline{ROT}$ is HIGH, both FO and PO are forced LOW.

The motor will take some time to stop following removal of motor drive. The $\overline{BREV}$ output provides the timing required to brake the motor by shorting the windings or applying a reverse voltage. $\overline{BREV}$ goes LOW on the rising edge of $\overline{ROT}$, and goes HIGH again when the motor frequency drops to 1/8 of lock frequency.

$\overline{ROT}$ and $\overline{BREV}$ timing is shown below in Fig.5.

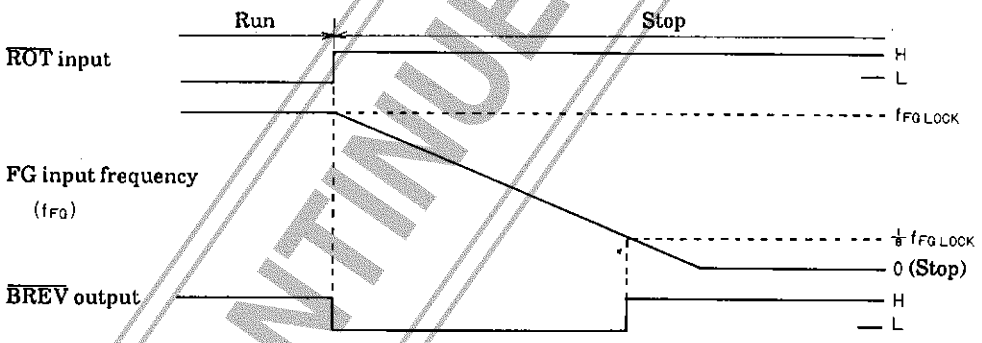



Fig.5 Motor Brake Timing

H : High level
L : Low level

### 4. Phase Range Select

The PRS1 and PRS2 inputs select the phase comparator range, as shown in Table 4. The $6\pi$ and $14\pi$ ranges have a hysteresis region beyond the normal $2\pi$ phase comparison region, as shown in Fig.6.

Table 4. Phase Range Selection

| PRS2 | PRS1 | Range |
|---|---|---|
| L | L | $2\pi$ |
| L | H | Test mode |
| H | L | $6\pi$ |
| H | H | $14\pi$ |

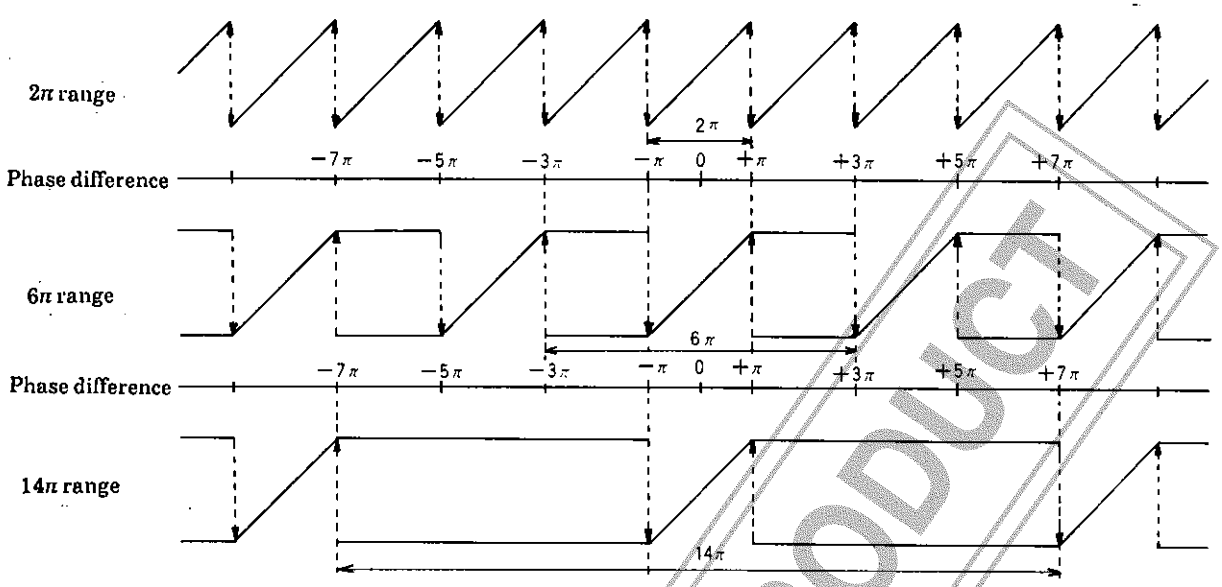



Fig.6 Phase Comparison Ranges

## Sample Application Circuit