RFP30N06LE, RF1S30N06LESM

Data Sheet April 1999 File Number 3629.2

30A, 60V, ESD Rated, 0.047 Ohm, Logic Level N-Channel Power MOSFETs

These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

These transistors incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

Formerly developmental type TA49027.

Ordering Information

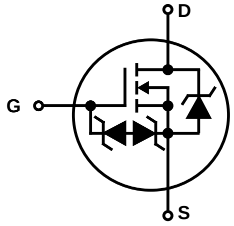
PART NUMBER	PACKAGE	BRAND
RFP30N06LE	TO-220AB	F30N06LE
RF1S30N06LESM	TO-263AB	1S30N06L

NOTE: When ordering use the entire part number. Add suffix, 9A, to obtain the TO-263 variant in tape and reel i.e. RF1S30N06LESM9A.

Features

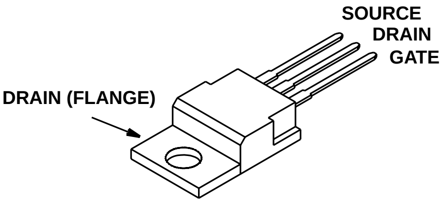
- 30A, 60V
- $r_{DS(ON)} = 0.047\Omega$
- 2kV ESD Protected
- Temperature Compensating PSPICE™ Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

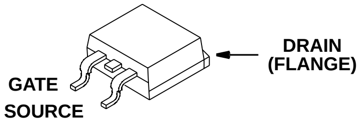


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_A = 25^oC$, Unless Otherwise Specified

		RFP30N06LE, RF1S30N06LESM	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	+10, -8	V
Continuous Drain Current	I_D	30	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	96	W
Derate Above 25^oC		0.645	$W/^oC$
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2	kV
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$, Figure 11		60	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$, Figure 10		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated B_{VDSS}, $V_{GS} = 0$		-	-	25	µA
		V_{DS} = 0.8 x Rated B_{VDSS}, $V_{GS} = 0$, $T_C = 150^oC$		-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = +10, -8V$		-	-	±10	µA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 30A$, $V_{GS} = 5V$, Figure 9		-	-	0.047	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 30A$, $R_L = 1\Omega$, $V_{GS} = 5V$, $R_{GS} = 2.5\Omega$, Figures 13, 16, 17		-	-	140	ns
Turn-On Delay Time	$t_{d(ON)}$			-	11	-	ns
Rise Time	t_r			-	88	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	30	-	ns
Fall Time	t_f			-	40	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 48V$, $I_D = 30A$, $R_L = 1.6\Omega$ Figures 18, 19	-	51	62	nC
Gate Charge at 5V	$Q_{g(5)}$	$V_{GS} = 0V$ to $5V$		-	28	34	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to $1V$		-	1.8	2.6	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz Figure 12		-	1350	-	pF
Output Capacitance	C_{OSS}			-	290	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	85	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.55	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	$I_{SD} = 30A$	-	-	1.5	V
Diode Reverse Recovery Time	t_{rr}	$I_{SD} = 30A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

NOTES:

2. Pulse Test: Pulse Width ≤ 300ms, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse Width limited by max junction temperature. See Transient Thermal Impedance Curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves Unless Otherwise Specified

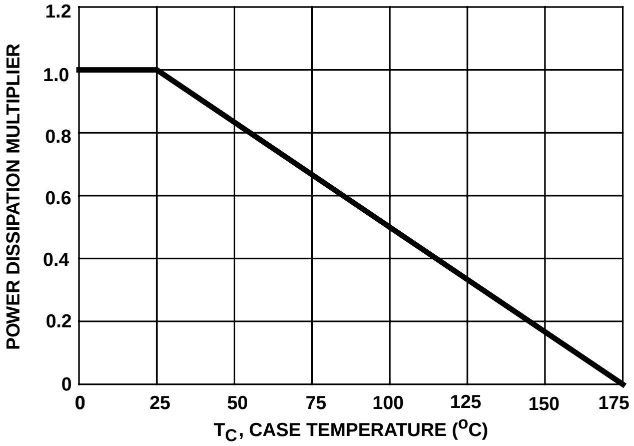


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

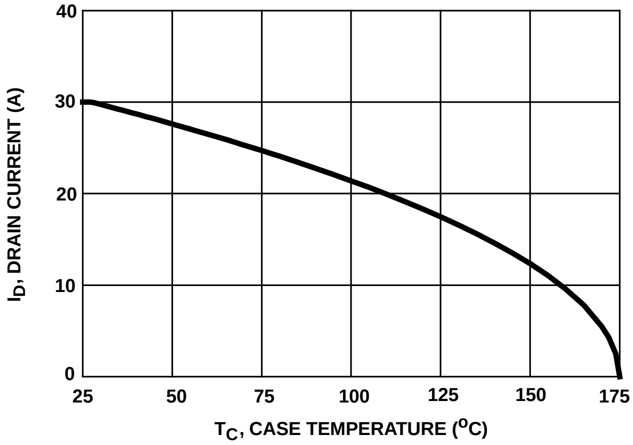


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

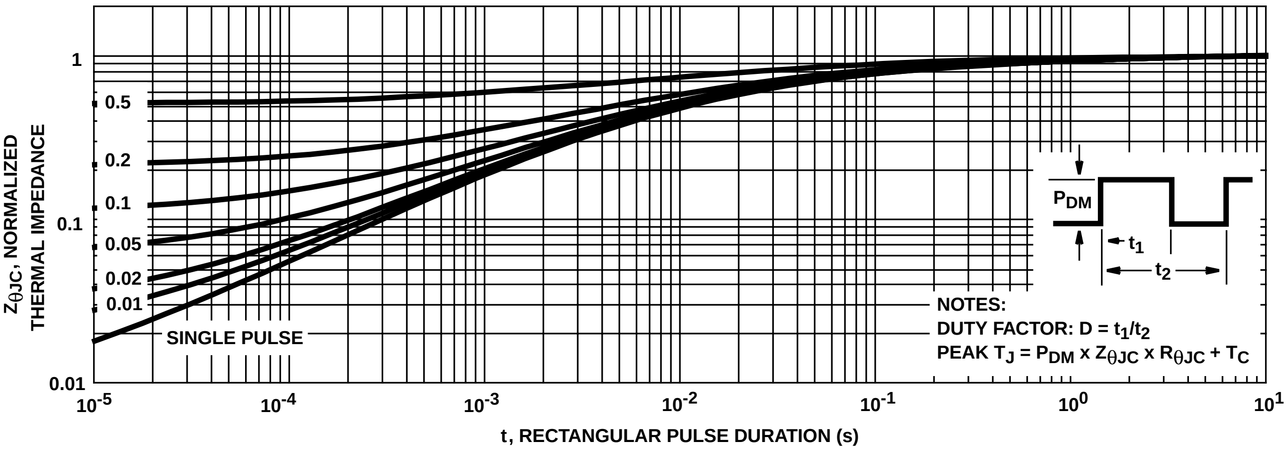


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

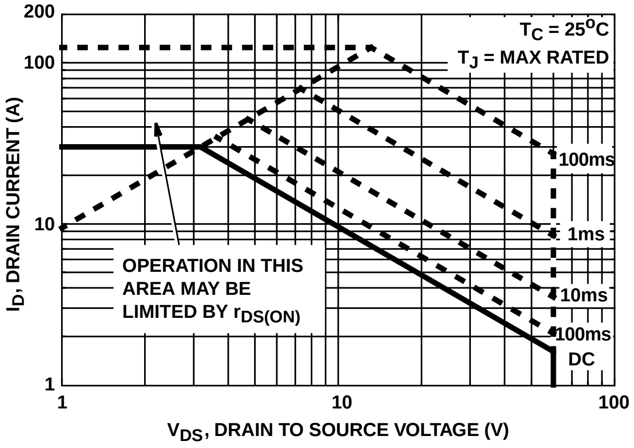


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

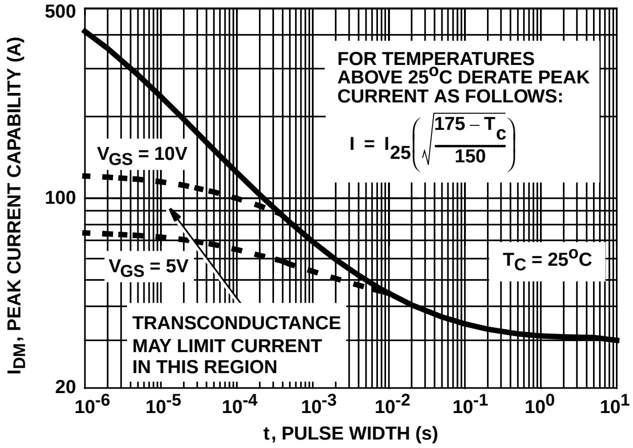
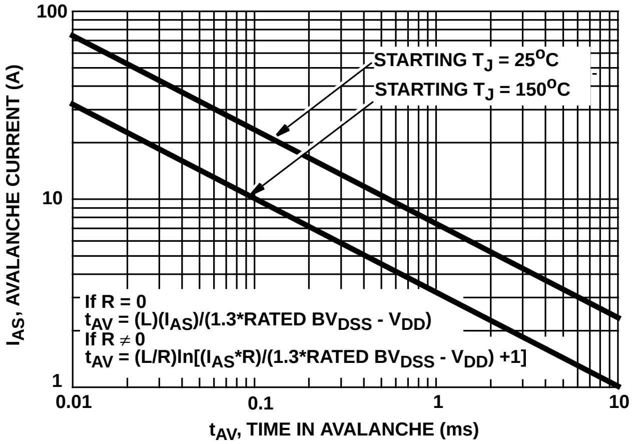


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified **(Continued)**



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

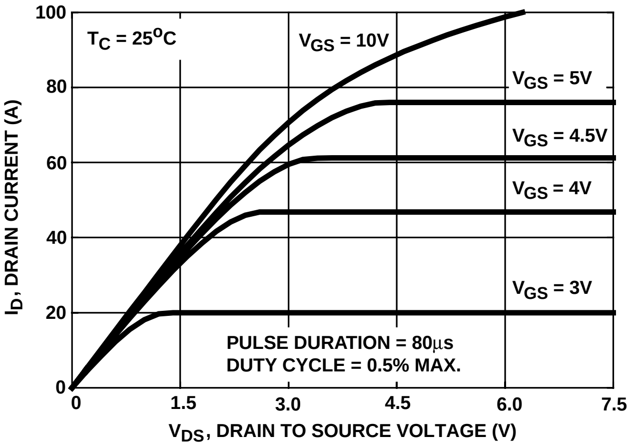


FIGURE 7. SATURATION CHARACTERISTICS

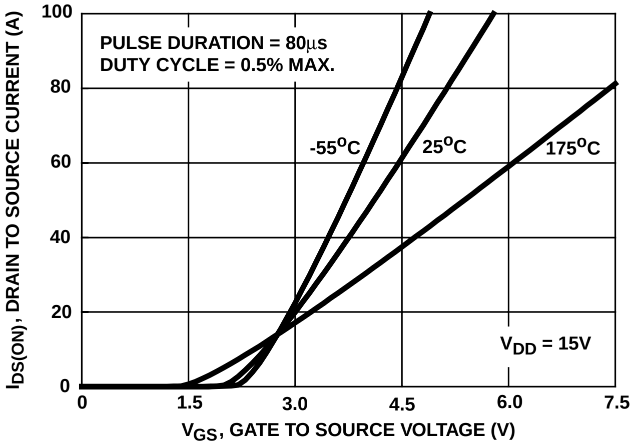


FIGURE 8. TRANSFER CHARACTERISTICS

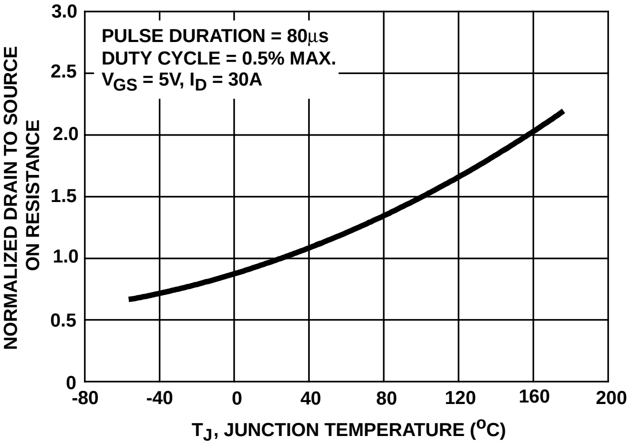


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

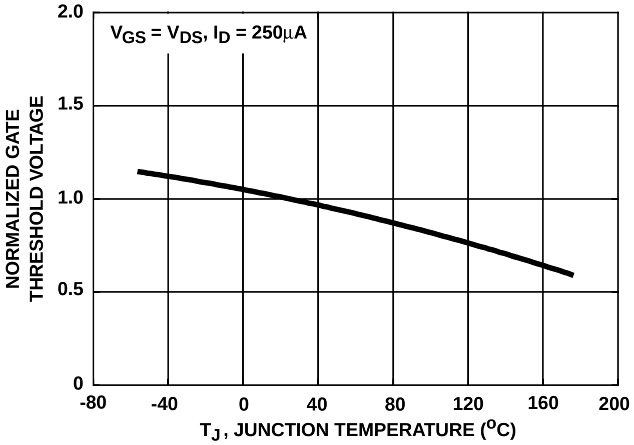


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

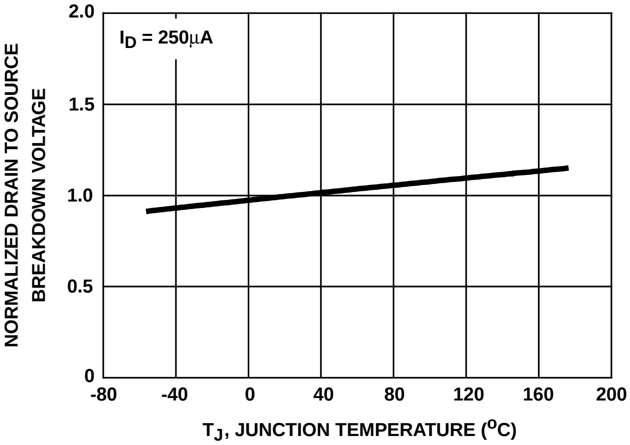


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

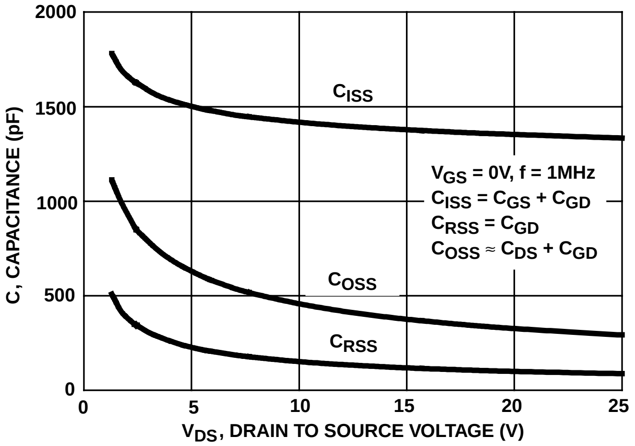
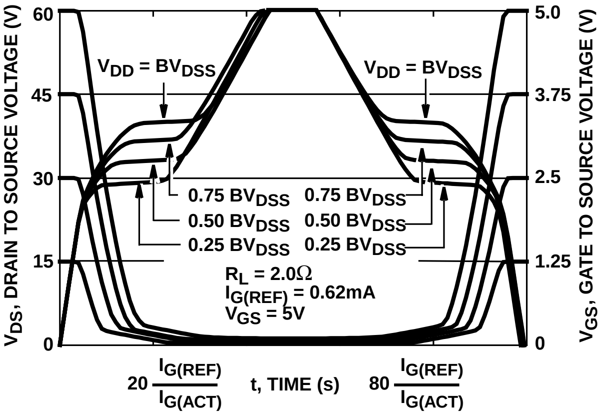


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

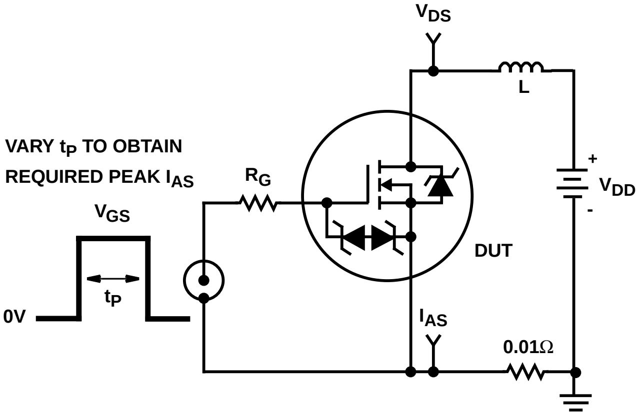


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

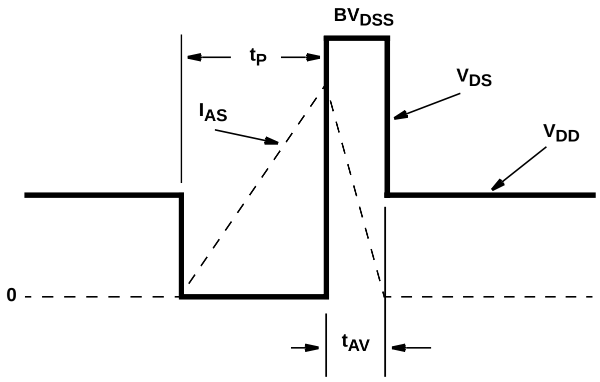


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

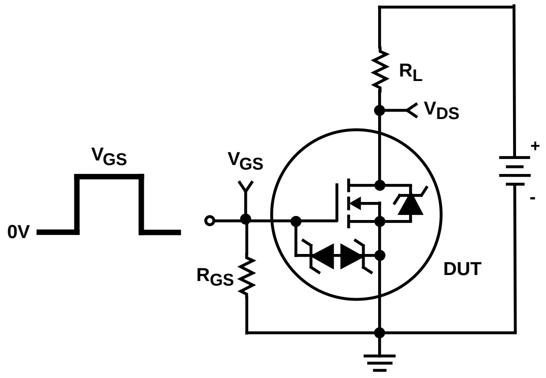


FIGURE 16. SWITCHING TIME TEST CIRCUIT

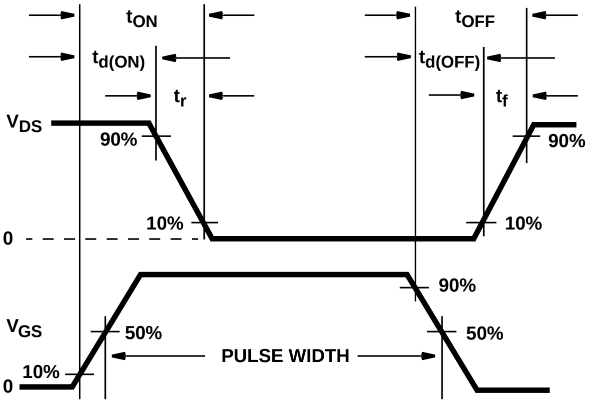


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

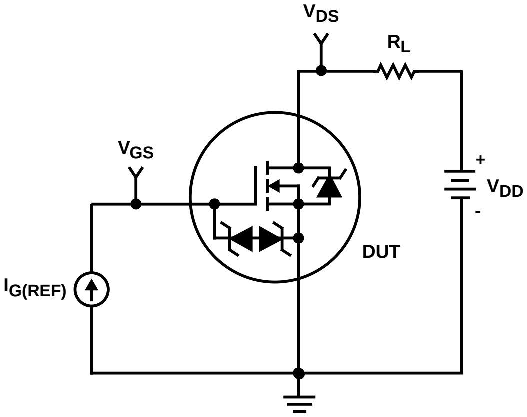


FIGURE 18. GATE CHARGE TEST CIRCUIT

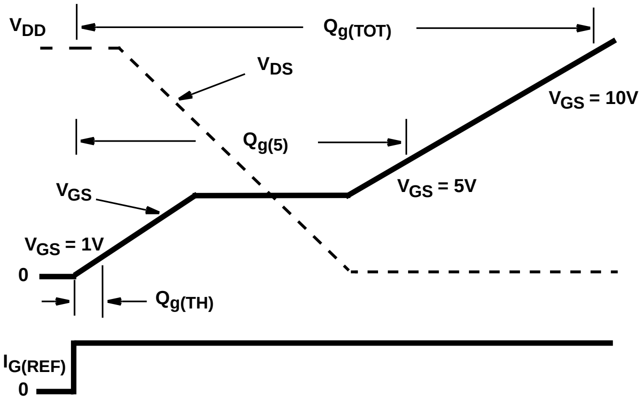
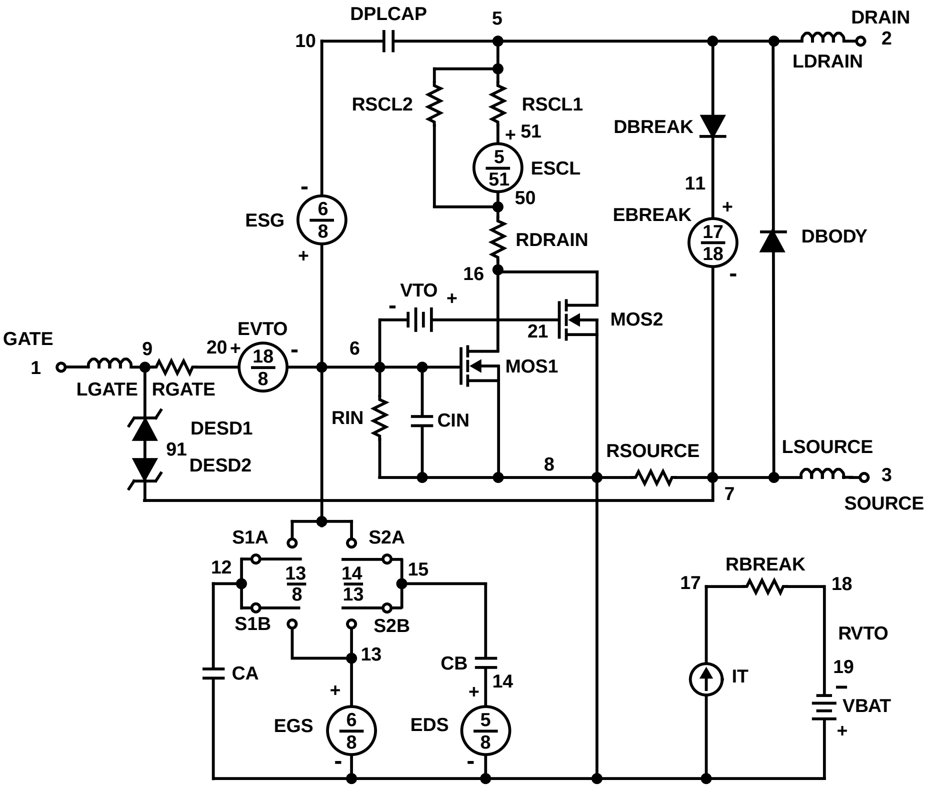


FIGURE 19. GATE CHARGE WAVEFORMS

PSPICE Electrical Model



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SUBCKT RFP30N06LE  2 1 3;        rev 6/2/93
CA 12 8 1 3.34e-9
CB 15 14 3.44e-9
CIN 6 8 0 1.343e-9

DBODY 7  5  DBDMOD
DBREAK 5 11  DBKMOD
DESD1 91 9  DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10  5  DPLCAPMOD

EBREAK 11 7  17 18  75.39
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN  2  5  1e-9
LGATE 1  9  7.22e-9
LSOURCE 3 7  6.31e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 11.86e-3
RGATE 9 20 2.52
RIN 6 8 1e9
RSCL1  5  51  RSLVCMOD 1e-6
RSCL2  5  50  1e3
RSOURCE 8 7 RDSMOD 26.6e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6  0.5

ESCL  51 50  VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/89,7))

.MODEL DBDMOD D (IS = 3.80e-13  RS = 1.12e-2  TRS1 = 1.61e-3  TRS2 = 6.08e-6  CJO = 1.05e-9  TT = 3.84e-8)
.MODEL DBKMOD D (RS = 1.82e-1  TRS1 = 7.50e-3  TRS2 = -4.0e-5)
.MODEL DESD1MOD D (BV = 13.54  TBV1 = 0  TBV2 = 0  RS = 45.5  TRS1 = 0  TRS2 = 0)
.MODEL DESD2MOD D (BV = 11.46  TBV1 = -7.576e-4  TBV2 = -3.0e-6  RS = 0  TRS1 = 0  TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 0.591e-9  IS = 1e-30  N = 10)
.MODEL MOSMOD NMOS (VTO = 1.94  KP = 139.2  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 1.07e-3  TC2 = -3.03e-7)
.MODEL RDSMOD RES (TC1 = 5.38e-3  TC2 = 1.64e-5)
.MODEL RSLVCMOD RES (TC1 = 1.75e-3  TC2 = 3.90e-6)
.MODEL RVTOMOD RES (TC1 = -2.15e-3  TC2 = -5.43e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.05  VOFF = -1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.5  VOFF = -4.05)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -2.2  VOFF = 2.8)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 2.8  VOFF = -2.2)

.ENDS
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NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records 1991.

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