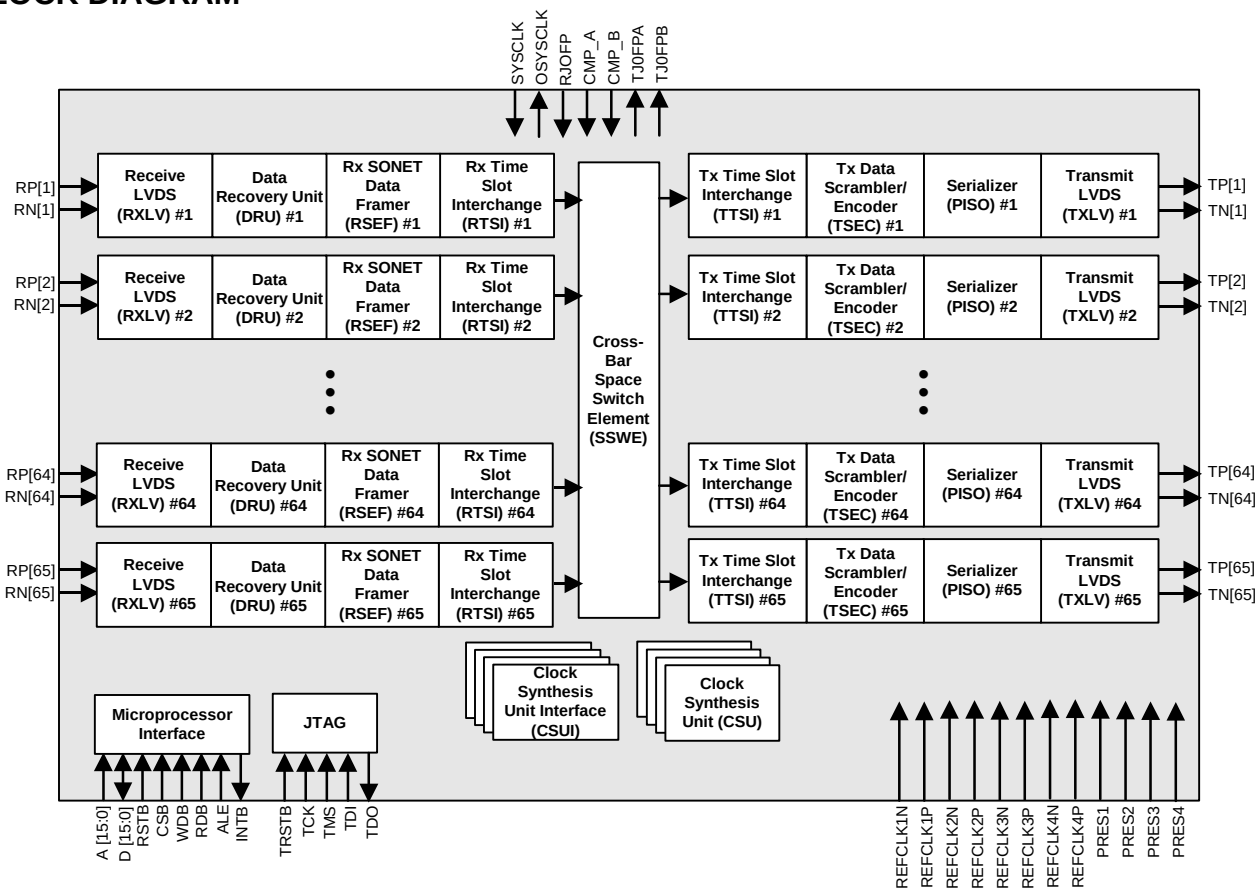
160 Gbit/s Transport Switching Element

FEATURES

- Supports multiple fabric architectures that range from 160 Gbit/s (one PM5374 TSE-160) to 640 Gbit/s (four TSE-160 devices) in a single stage, and beyond 10 Tbit/s using multi-stage fabrics.
- Implements a Time-Space-Time fabric with STS-1/AU-3 granularity.
- Provides Test Port functionality with 65th port. Transmit test port can snoop on any data arriving at a single receive link, or any data departing a single transmit link. Receive Test Port can be used to inject arbitrary data into the device.
- Provides two independent time domains for frame alignment purposes. These time domains can be arranged in sets (faces) of 16 links. The selection of the time domains for each link interface is selectable through the software interface.
- Supports STS-48 equivalent flows using SONET scrambling over LVDS links operating at 2.488.
- Supports STS-12 equivalent flows using an extended 8B/10B protocol over LVDS links operating at 777.6 Mhz to support first generation CHESS™ interfaces.
- Provides 65 ingress and egress STS-48 equivalent ports for a total of 65*48 = 3120 STS-1 flows.
- Optionally supports 65 ingress and egress STS-12 equivalent ports for a total of 65*12 = 780 STS-1 flows.
- Provides SONET scrambled 622 Mbit/s link operation, selectable per link face.
- Supports non-blocking permutation switching at STS-1 granularity for the above supported flows.
- Ports are grouped in sets (faces) of 16 links, and each face is configurable for STS-12 or STS-48 data rates.
- Supports multi-plane (inverse multiplexed) switch architectures in conjunction with other CHESS™ components.
- Interfaces to STS-192 devices by aggregating 16 STS-12, 8 STS-24, or 4 STS-48 equivalent flows.
- Supports multicast and broadcast of STS-1 streams.
- Detects and reports inactive or errored LVDS links via the microprocessor interface.
- Supports two sets of switch settings (active and standby) and a controlled method of changing settings on STS-1 frame boundaries.
- Supported by an efficient algorithm to compute control settings for all permutation loads for all supported fabric architectures. Algorithms are also available for multicast/broadcast allocation.

BLOCK DIAGRAM



160 Gbit/s Transport Switching Element

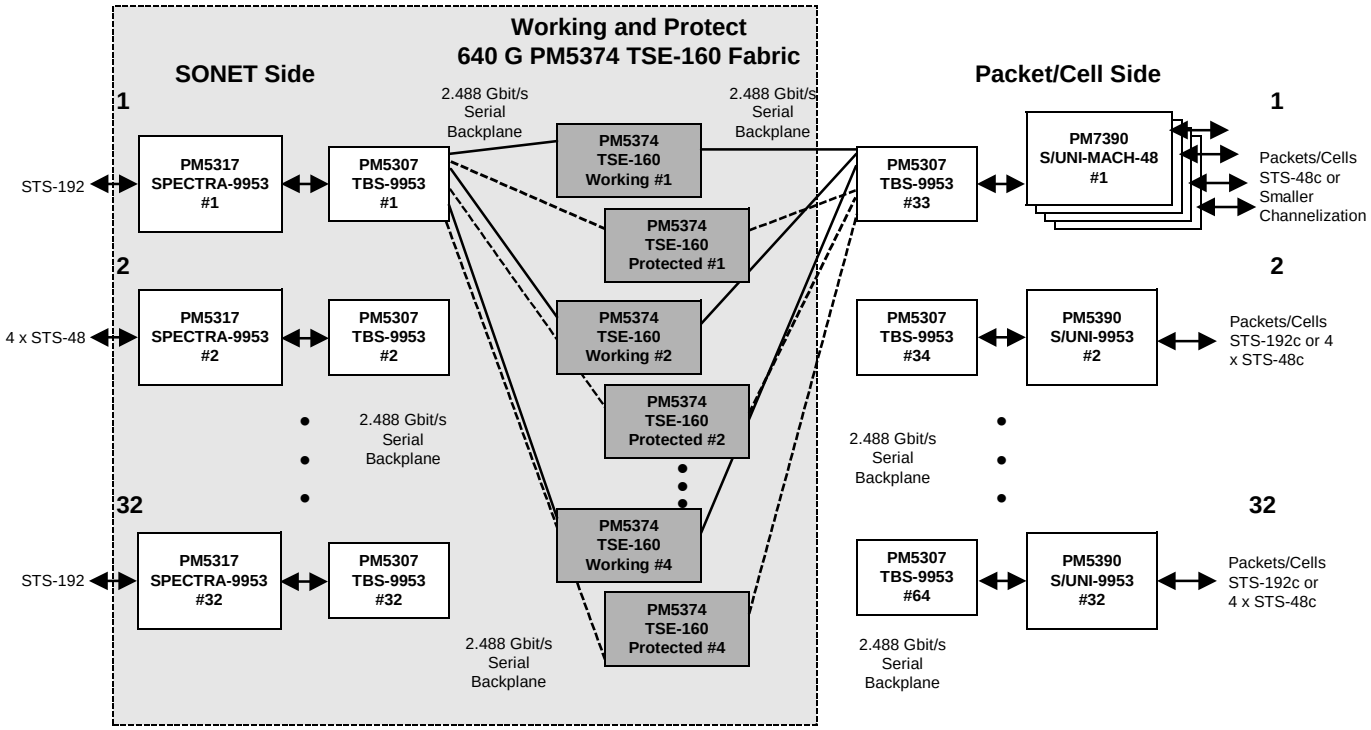
- Driven by a 155.52 MHz reference clock.
- Implemented in 1.8 V core and 3.3 V I/O, 0.18 µm CMOS and packaged in a 1152 ball FCBGA.
- Requires no external RAMs or logic parts.
- Provides a standard IEEE 1149.1 JTAG port.
- Supports a 16-bit microprocessor interface which is used to initialize the device, to write switch settings into on-chip control tables, and to monitor device performance.

APPLICATIONS

- Optical cross connects.
- Multi-service provisioning platforms.
- SONET/SDH Add/Drop Multiplexers.
- SONET/SDH Digital Cross connects.

TYPICAL APPLICATIONS

MULTI-SERVICE SWITCH



ADM Function

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