MN662785TBUC

1. TYPE

Signal processing integrated circuit for CDs (Compact Discs)

2. OVERVIEW

MN662785TBUC is a signal processing IC for CDs. It incorporates optical servo (focus, tracking, and traverse servos) processing function, digital signal processing function (EFM demodulation and error correction), digital servo processing function for spindle motor, anti-shock memory control function for 16M, 4M, or 1M DRAM in compression or decompression mode available to disc rotation synchronous playback (jitter-free), a digital filter, and D/A converter. All the processing functions after the head amplifier (RF amplifier) are incorporated into a single chip.

3. FUNCTIONS AND FEATURES

(Optical servo)
- Focus (Fo), tracking (Tr), and traverse (TRV) servos
- Automatic adjustment functions (Fo/Tr gain, Fo/Tr offset, Fo/Tr balance)
- On-chip PWM for drive output
- Provided with a countermeasure for dropout
- Provided with anti-shock function
- Provided with track cross detection function

(Digital signal processing)
- Containing DSL and PLL
- Provided with a frame synchronous detection/protection/interpolation
- Subcode data processing
  - Q-data CRC check
  - On-chip Q-data register
  - On-chip CD-TEXT-data register
- CIRC error correction
  - C1 decoder : double error correction
  - C2 decoder : triple error correction
  - On-chip de-interleaving 16K RAM
- Audio data interpolation processing
  - 4-sampling linear interpolation and previous value hold
- Soft muting
- Digital attenuation (256 levels) (-∞, -48 dB to 0 dB, 256 levels)
- Soft attenuation (256 levels) (-∞, -48 dB to 0 dB, 256 levels)
- Digital audio interface (EIAJ format), IEC format
- Compatible with digital audio interface when anti-shock memory control is turned on.
- Compatible with bilingual operation when anti-shock memory control is turned on.

(Spindle motor servo)
- CLV digital servo
- Provided with servo gain selection function
- Provided with shaft loss compensation setting function
- Provided with forced acceleration/deceleration output level setting function

(Audio circuit)

- 8x-oversampling digital filter
- On-chip low-voltage op amp
- Bass boost filter, high-band notch filter, and surround function

(Anti-shock memory controller)

- ADPCM 4-bit compression or expansion mode/decompression full 16-bit mode
- External DRAM selectable

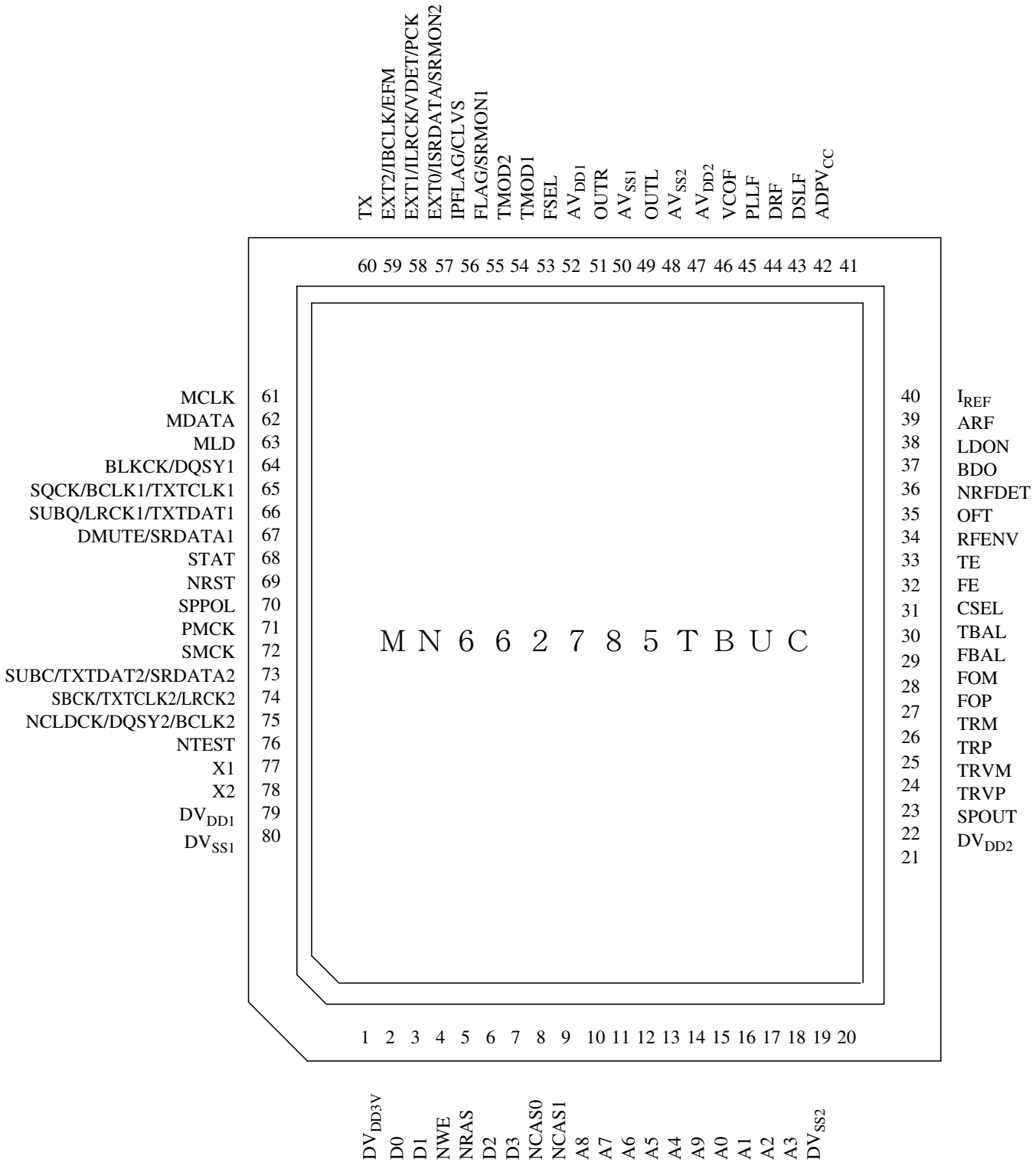
16M DRAM (4M × 4 bits)	× 1
4M DRAM (1M × 4 bits)	× 2
4M DRAM (1M × 4 bits)	× 1
1M DRAM (256K × 4 bits)	× 2
1M DRAM (256K × 4 bits)	× 1

(Others)

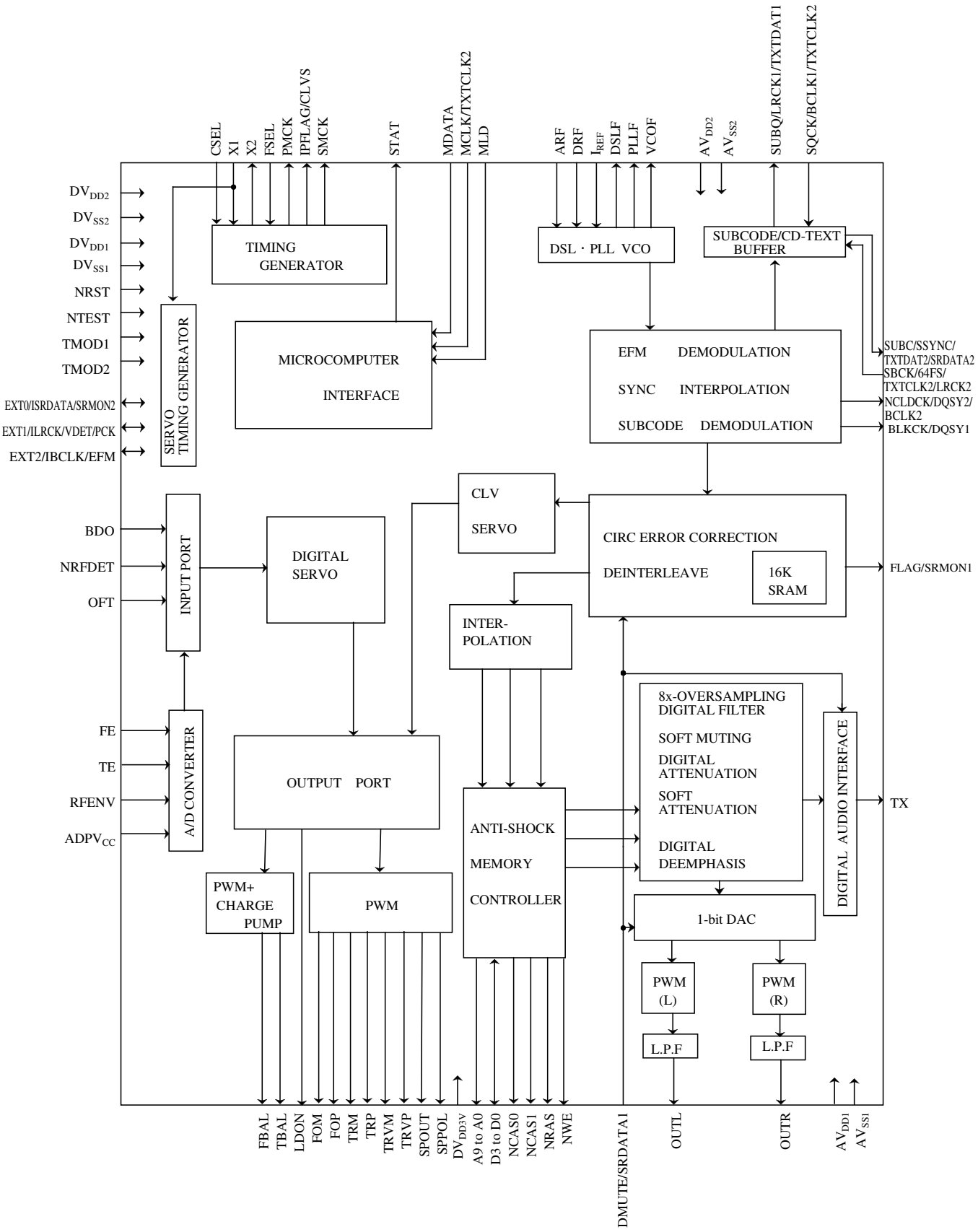
- Disc rotation synchronous playback (jitter-free) mode

4. PIN ASSIGNMENT

・80-pin quad flat package (LQFP080-P-1414A)



5. BLOCK DIAGRAM



6. PIN DESCRIPTIONS

No.	Symbol	I/O	Function
1	DV_{DD3V}	I	Power supply for DRAM interface (Pins 2 to 19)
2	D0	I/O	DRAM data I/O 0
3	D1	I/O	DRAM data I/O 1
4	NWE	O	DRAM write enable signal output
5	NRAS	O	DRAM RAS control signal output
6	D2	I/O	DRAM data I/O 2
7	D3	I/O	DRAM data I/O 3
8	NCAS0	O	DRAM CAS control signal output 0
9	NCAS1	O	DRAM CAS control signal output 1 (When two 1M or 4M DRAMs are in use) DRAM address signal output 10 (When 16M DRAM is in use)
10	A8	O	DRAM address signal output 8
11	A7	O	DRAM address signal output 7
12	A6	O	DRAM address signal output 6
13	A5	O	DRAM address signal output 5
14	A4	O	DRAM address signal output 4
15	A9	O	DRAM address signal output 9
16	A0	O	DRAM address signal output 0
17	A1	O	DRAM address signal output 1
18	A2	O	DRAM address signal output 2
19	A3	O	DRAM address signal output 3
20	DV_{SS2}	I	Ground for digital circuits
21	DV_{DD2}	I	Power supply for digital circuits
22	SPOUT	O	Spindle motor drive signal output

No.	Symbol	I/O	Function
23	TRVP	O	Traverse drive signal output (+ side output)
24	TRVM	O	Traverse drive signal output (- side output)
25	TRP	O	Tracking drive signal output (+ side output)
26	TRM	O	Tracking drive signal output (- side output)
27	FOP	O	Focus drive signal output (+ side output)
28	FOM	O	Focus drive signal output (- side output)
29	FBAL	O	Focus balance adjustment signal output
30	TBAL	O	Tracking balance adjustment signal output
31	CSEL	I	Test pin Normal: H
32	FE	I	Focus error signal input
33	TE	I	Tracking error signal input
34	RFENV	I	RF envelope signal input
35	OFT	I	Off-track signal input H : Off track
36	NRFDET	I	RF detection signal input L : Detect
37	BDO	I	Dropout signal input H : Dropout
38	LDON	O	Laser ON signal output H : ON
39	ARF	I	RF signal input
40	I_{REF}	I	Reference current input
41	$ADPV_{CC}$	I	A/D converter reference voltage input
42	DSLF	O	DSL loop filter
43	DRF	I	DSL bias
44	PLLF	O	PLL loop filter
45	VCOF	O	Jitter-free VCO loop filter
46	AV_{DD2}	I	Power supply for analog circuits (For DSL, PLL, VCOF, DRF, and A/D converter)
47	AV_{SS2}	I	Ground for analog circuits (For DSL, PLL, VCOF, DRF, and A/D converter)

No.	Symbol	I/O	Function
48	OUTL	O	L-ch audio output (Refer to Note in page 3)
49	AV_{SS1}	I	Ground for analog circuits (For audio output stage)
50	OUTR	O	R-ch audio output (Refer to Note in page 3)
51	AV_{DD1}	I	Power supply for analog circuits (For audio output stage)
52	FSEL	I	Test pin Normal: H (Noise filter is selected by using a command.)
53	TMOD1	I	Pin mode selection input 1 Normal: L
54	TMOD2	I	Pin mode selection input 2 Normal: L
55	FLAG/SRMON1	O	Flag signal output / Serial monitor signal output 1 (Evaluation dedicated monitor)
56	IPFLAG/CLVS	O	Command selection ・Interpolation flag signal output H: Interpolation ・Spindle servo phase sync signal output H: CLV L: Rough servo
57	EXT0/ ISRDATA/ SRMON2	I/O	Command selection ・ Expansion port 0 I/O ・ Serial audio data input (External I/O mode) $64f_S$ ・ Serial monitor signal output 2 (Evaluation dedicated monitor)
58	EXT1/ ILRCK/ VDET/PCK	I/O	Command selection ・ Expansion port 1 I/O ・ L or R discrimination signal input (External I/O mode) H: L-ch audio data L: R-ch audio data ・ Vibration detection flag signal output ・ PLL extraction clock output f_{PCK} =4.321 MHz (Normal-speed playback)
59	EXT2/ IBCLK/EFM	I/O	Command selection ・ Expansion port 2 I/O ・ Bit clock input (External I/O mode) $64f_S$ ・ EFM monitor signal
60	TX	O	Digital audio interface signal output
61	MCLK	I	Microcomputer command clock signal input
62	MDATA	I	Microcomputer command data signal input
63	MLD	I	Microcomputer command load signal input L : Load
64	BLKCK/ DQSY1	O	・Block clock signal output f_{BLKCK}=75 Hz (Normal-speed playback) ・CD-TEXT sync signal output f_{DQSY}=300 Hz (Normal-speed playback)
65	SQCK/ BCLK1/ TXTCLK1	I/O	・External clock input for subcode Q register ・Bit clock output ・CD-TEXT data read clock input 1
66	SUBQ/ LRCK1/ TXTDAT1	O	・Subcode Q-data output ・L or R discrimination signal output H: L-ch audio data L: R-ch audio data ・CD-TEXT data output 1

No.	Symbol	I/O	Function
67	DMUTE/ SRDATA1	I/O	・Muting input H：Mute (Muting of OUTL, OUTR, and TX outputs) ・Serial audio data output
68	STAT	O	Status signal output (CRC, RESY, CLVS, NTTSTOP, SQOK, FLAG6, SENSE, NFLOCK, NTLOCK, BSSEL, ZDET, SUBQ data output, CD-TEXT data output, Anti-shock memory controller reading data, Disc rotation speed data)
69	NRST	I	Reset input L：Reset
70	SPPOL	O	Spindle motor power control signal output (PC)
71	PMCK	O	88.2-kHz clock signal output
72	SMCK	O	・4.2336-MHz clock signal output ・8.4672-MHz clock signal output
73	SUBC/ SSYNC/ TXTDAT2/ SRDATA2	O	・Subcode output ・CD-TEXT data output ・Serial audio data output
74	SBCK/ TXTCLK2/ LRCK2	I	・Subcode output clock input ・CD-TEXT data read clock input 3 ・L or R discrimination signal output (External output mode) H: L-ch audio data L: R-ch audio data
75	NCLDCK/ DQSY2/ BCLK2	O	・Frame sync signal output f_{CLDCK}=7.35 kHz (Normal-speed playback) ・CD-TEXT output f_{DQSY} =300 Hz (Normal-speed playback) ・Bit clock output
76	NTEST	I	Test pin Normal: H
77	X1	I	Crystal oscillator input pin f=33.8688 MHz
78	X2	O	Crystal oscillator output pin f=33.8688 MHz
79	DV_{DD1}	I	Power supply for digital circuits
80	DV_{SS1}	I	Ground for digital circuits

7. FUNCTION DESCRIPTION (Table of contents)

7-0 Contents of functions amended from MN662780

(1) Digital servo section

- Focus and tracking servos' sampling frequency : 88.2 kHz
- Timings of initial settings
- Spindle forced acceleration/deceleration output level setting
- KICK pulse level setting (KICK2) for servo pull-in operation abolished
- Zero-cross reference brake mode abolished
- Fixed noise rejection mode during braking operation of tracking
- Software reset function added
- Change of servo parameter exponent part format (FEXP, TEXP)

(2) Digital filter (DF) and D/A converter (DAC) sections

- DF and DAC sections operating clock selectable between normal-speed and 2x-speed modes
- DF section 8x-oversampling operation
- Low-voltage op amp
- Change of low-band boost filter characteristics
  (Low band: +3 dB → +4.5 dB)

(3) Signal processing section

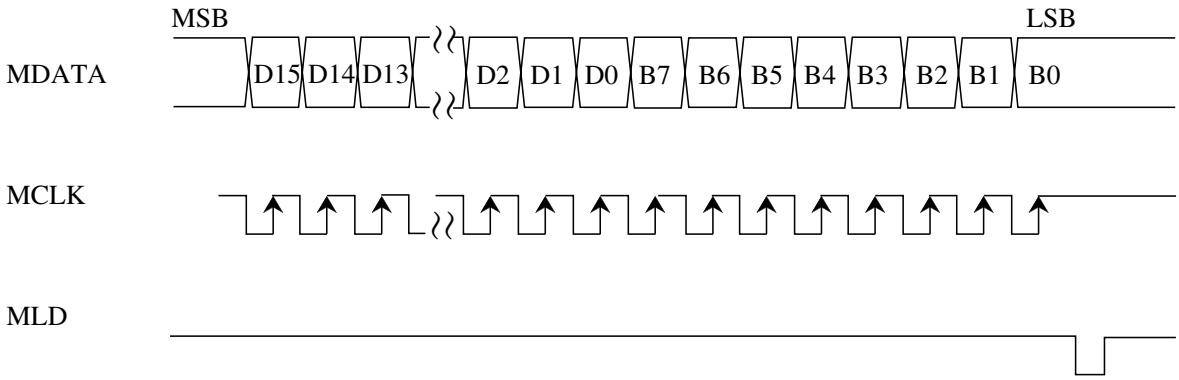
- 33.8688-MHz system clock
- Function to select a microcomputer interface input noise filter with a command
- Clock selection function for microcomputer (4 MHz, 8 MHz)
- Function to select current rate of PLL frequency comparison and phase comparison
- Function to select output width when detecting 12T or 5T
- Subcode Q data adding function in control of digital audio interface output when the anti-shock memory function is in use
- Compatible with bilingual operation when anti-shock memory function is in use
- Compatible with 2x-speed digital audio interface output
- Muting of data output from anti-shock memory controller
- Audio data 0 detection flag function (ZDET signal)

(4) Anti-shock memory controller

(5) The whole system
- Digital servo's D/A converter output abolished by PWM charge pump current output of FBAL, TBAL, and DSLF2
- No V_{REF} pin
- No DSLF2 pin
- Serial input/output interfaces added
- No PWMCK and TRVSTP pins
- No peak detection circuit
- No variable pitch function
- CD-TEXT mode interface added
- IPFLAG pin (pin 56) added
- EFM signal output added
- PCK signal output added
- VDET signal output added
- Added function to stop A/D converter operation with reference current shut-off command
- Oscillation stop mode added
- A/D converter reference voltage input pin ($ADPV_{CC}$: pin 41) added
- No CD-TEXT modes 1 and 3

7-1. Microcomputer interface

Each mode can be set by inputting the 16-bit data (D15 to D0) and 8-bit command (B7 to B0) starting from the MSB in 3 inputs of MDATA, MCLK, and MLD at the timing as shown in Figure 7-1-1.



Note) ・ Data is determined at the "L" level of MLD.
・ MDATA, MCLK, and MLD are invalid while NRST is "L."
・ All commands are initialized by setting NRST to "L."
・ While MLD is set to "L," MCLK will be canceled if it rises.
・ Set 0 to any bit which is input through the MDATA input with no functional specification assigned to the bit.

(Timing)

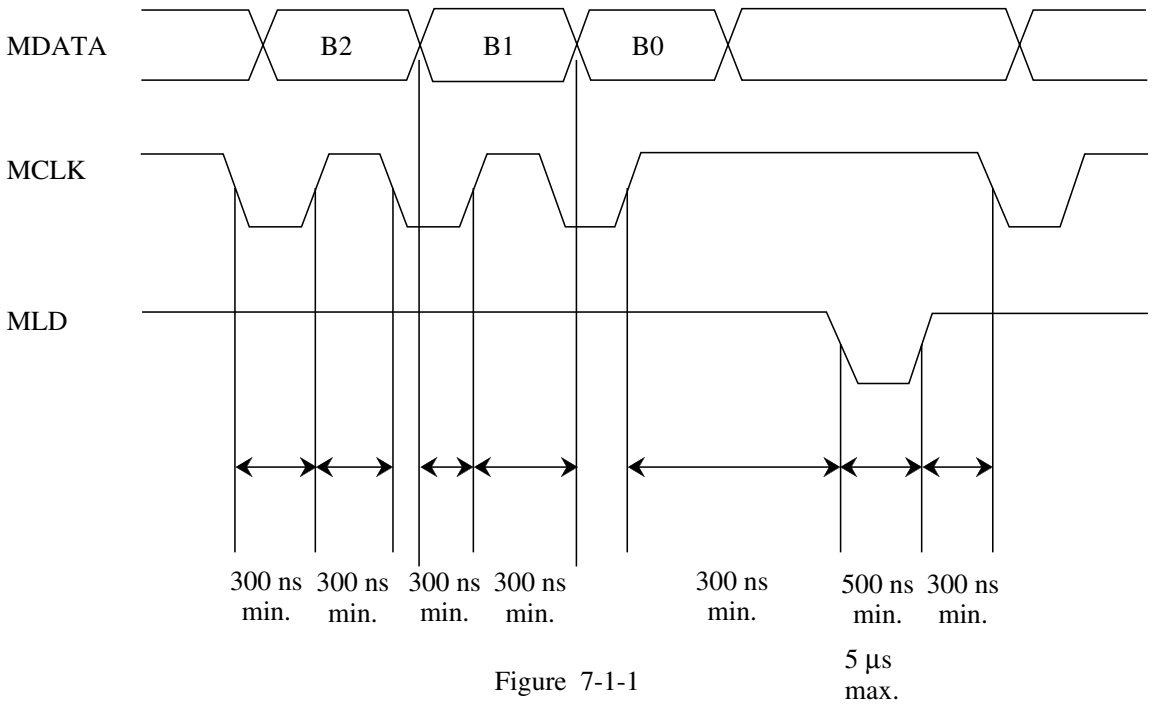


Figure 7-1-1

7-1 (1) List of commands vs. control items

Table 7-1-1

Command (HEX) (B7 to B0)	Control Target	Block
1 × 4 × 7 ×	Spindle servo Various signal processing STAT output	Signal processing section
8 × 9 ×	Anti-shock memory write command Anti-shock memory read command	Anti-shock memory controller
E × F ×	Focus, tracking, and traverse servos Initial setting, automatic adjustment, and access	Optical servo section

7-1 (2) List of microcomputer commands

Set 0 to any bit which is indicated by X in the following list of commands with no functional specification assigned to the bit.

(1) Commands for signal processing section

No data length setting is required wherever — appears in the following table. Table 7-1-2 (1)

Control target	Data length	Command (B7 to B0)	Symbol	Function (＊：Setting at reset)	Reference page
Spindle Control 1	———	0 0 0 1 X 0 X X	TTOFF	＊ Turntable OFF	
	———	0 0 0 1 X 1 X X	TTON	Turntable ON	
	———	0 0 0 1 X X 0 0	STOP	＊ Free-running	
	———	0 0 0 1 X X 0 1	ACC	Acceleration	
	———	0 0 0 1 X X 1 0	BRAKE	Deceleration	
	———	0 0 0 1 X X 1 1	PLAY	Normal play	
Various signal processing control	16 bits	0 1 0 0 0 0 0 1		Audio control	46
	16 bits	0 1 0 0 0 0 1 0		Digital audio interface control	47
	16 bits	0 1 0 0 0 1 0 0		Attenuation control	48
	16 bits	0 1 0 0 0 1 0 1		Spindle control	48
	16 bits	0 1 0 0 0 1 1 0		PWM output control (Optical servo system)	49
	16 bits	0 1 0 0 1 0 0 1		Playback speed control	50
	16 bits	0 1 0 0 1 0 1 0		Dropout control	50
	16 bits	0 1 0 0 1 0 1 1		PLL control	51
	16 bits	0 1 0 0 1 1 0 0		I/O control 1	52
	16 bits	0 1 0 0 1 1 0 1		DSL unbalance compensation control	52
	16 bits	0 1 0 0 1 1 1 0		I/O control 2	53

Table 7-1-2 (2)

Control target	Data length	Command (B7 to B0)	Symbol	Function (＊ : Setting at reset)	Reference page
STAT pin output	———	0 1 1 1 0 0 0 0		＊ STAT output CRC	54
	———	0 1 1 1 0 0 0 1		STAT output RESY	54
	———	0 1 1 1 0 0 1 0		STAT output CLVS	54
	———	0 1 1 1 0 0 1 1		STAT output NTTSTOP	54
	———	0 1 1 1 0 1 0 0		STAT output SQOK	54
	3 bits	0 1 1 1 0 1 0 1		STAT output switching	54
	———	0 1 1 1 0 1 1 0		STAT output BSSEL	54
	———	0 1 1 1 0 1 1 1		STAT output FCLV	54
	———	0 1 1 1 1 0 0 0		STAT output SSTAT	54
	———	0 1 1 1 1 0 0 1		STAT output SUBQ (SQCK sync)	54
	———	0 1 1 1 1 0 1 0		STAT output SUBQ (MCLK sync)	54
	———	0 1 1 1 1 0 1 1		STAT output ZDET (Zero data detection)	54
	———	0 1 1 1 1 1 1 0		STAT output SPEED (Disc rotation speed)	54

(2) Commands for anti-shock memory controller

No data length setting is required wherever — appears in the following table.

Table 7-1-2 (3)

Control target	Data length	Command (B7 to B0)	Symbol	Function (＊ : Setting at reset)	Reference page
Write command	8 bits	1 0 0 0 0 0 0 0		Memory system command	55
	4 bits	1 0 0 0 0 0 0 1		Expansion I/O port I/O setting	55
	4 bits	1 0 0 0 0 0 1 0		Expansion I/O port output data setting	56
	8 bits	1 0 0 0 0 1 0 1		Option setting	56
	8 bits	1 0 0 0 0 1 1 0		Option setting	56
	———	1 0 0 0 0 1 1 1		TX Q-data input	57
Read command	———	1 0 0 1 0 0 0 0		Status 1 reading (Read data length: 8 bits)	58
	———	1 0 0 1 0 0 0 1		Status 2 reading (Read data length: 8 bits)	58
	———	1 0 0 1 0 0 1 0		Remaining enabled data check (Read data length: 16 bits)	59
	———	1 0 0 1 0 0 1 1		Expansion I/O port input data setting (Read data length: 8 bits)	59

(3) Commands for optical servo section

No data length setting is required wherever — appears in the following table.

Table 7-1-2 (4)

Control target	Data length	Command (B7 to B0)	Symbol	Function (* : Setting at reset)	SENSE signal	Reference page
Optical servo	———	1 1 1 0 0 0 0 0	STB	* Standby	OFT	
	———	1 1 1 0 0 0 0 1		Reserved		
	———	1 1 1 0 0 0 1 0	DDT	Disc detection	FESL	
	———	1 1 1 0 0 0 1 1	TOF	Fo ON, Tr OFF	FESL	
	———	1 1 1 0 0 1 0 X	PLY	Fo ON, Tr ON	OFT	
	———	1 1 1 0 0 1 1 0		Reserved		
	———	1 1 1 0 0 1 1 1		Reserved		
Traverse servo	———	1 1 1 0 1 0 0 0	TVS	* Traverse stop	Unchanged	
	———	1 1 1 0 1 0 0 1		Reserved		
	———	1 1 1 0 1 0 1 0	TVF	Traverse forward feed	Unchanged	
	———	1 1 1 0 1 0 1 1	TVR	Traverse reverse feed	Unchanged	
	———	1 1 1 0 1 1 X X	TVP	Traverse play	Unchanged	
Access	———	1 1 1 1 0 0 0 0	ACA	Stopping access operation	NACEND	
	16 bits	1 1 1 1 0 0 0 1	KICK	Kick	NACEND	44
	16 bits	1 1 1 1 0 0 1 1	TCNT	Track count move	NACEND	44
Data setting	16 bits	1 1 1 1 0 0 1 0	DTMS	Data write	NWTEND	19
	8 bits	1 1 1 1 0 1 0 0	DTSM	Data read	DATA	20
Initial setting	———	1 1 1 1 0 1 0 1	SYS	Await initialization cancel command		18
	———	1 1 1 1 0 1 1 0		Reserved		
Automatic adjust-ment	———	1 1 1 1 0 1 1 1	ABC1	Focus balance adjustment	NAJEND	60
	———	1 1 1 1 1 0 0 0	ADA	Stopping automatic adjustment	NAJEND	60
	———	1 1 1 1 1 0 0 1	AOC	Offset adjustment (focus, tracking)	NAJEND	60
	———	1 1 1 1 1 0 1 0		Reserved		
	———	1 1 1 1 1 0 1 1	ABC2	Tracking balance adjustment	NAJEND	60
	———	1 1 1 1 1 1 0 0	AGC1	Focus rough gain adjustment	NAJEND	60
	———	1 1 1 1 1 1 0 1	AGC2	Tracking rough gain adjustment	NAJEND	60
	———	1 1 1 1 1 1 1 0	FAGC	Focus fine gain adjustment	NAJEND	60
	———	1 1 1 1 1 1 1 1	TAGC	Tracking fine gain adjustment	NAJEND	60

・SENSE signal

SENSE signal can be monitored through STAT pin. The meaning of SENSE signal varies with the input command. The meanings are described below.

OFT	Off-track input signal is output as it is.
FESL	It is set to "H" when the absolute value of the focus error signal amplitude exceeds 30 LSBs by executing the disc detection command.
NACEND	It is set to "L" when the access terminates and the pull-in operation of the tracking servo starts.
NAJEND	It is set to "L" when automatic adjustment terminates.
NWTEND	It is set to "L" when data write terminates normally.
DATA	The contents of the RAM of the specified address is output beginning with MSB by inputting MCLK a minimum of 25 µs after MLD is set to "L" with the data read command, DTSM, sent out for data reading. Refer to Figure 7-1-4.

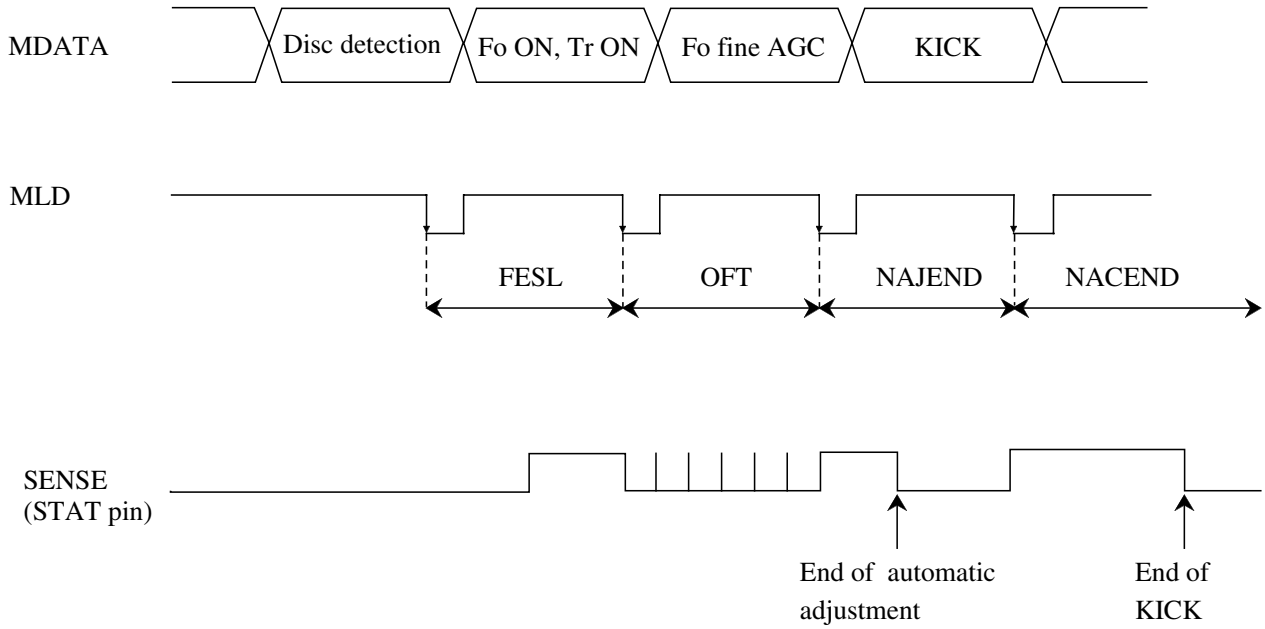


Figure 7-1-2 Switching of SENSE output

7-1 (3) Initial setting

After clearing NRST, the SENSE signal is set to "H" and the system is in the standby status for the SYS command.
After 75-ms continuous standby status for the SYS command, the STANDBY mode starts.
If the SYS command is sent during the period of 75-ms continuous standby status for the SYS command, however, the SENSE signal is set to "L" and the STANDBY mode starts immediately.
In the STANDBY mode, the system is ready for receiving the DTMS and DTSM commands.

Table 7-1-3

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function
D7 D6 D5 D4 D3 D2 D1D0 X X X X X X X X	XX	F5	SYS command

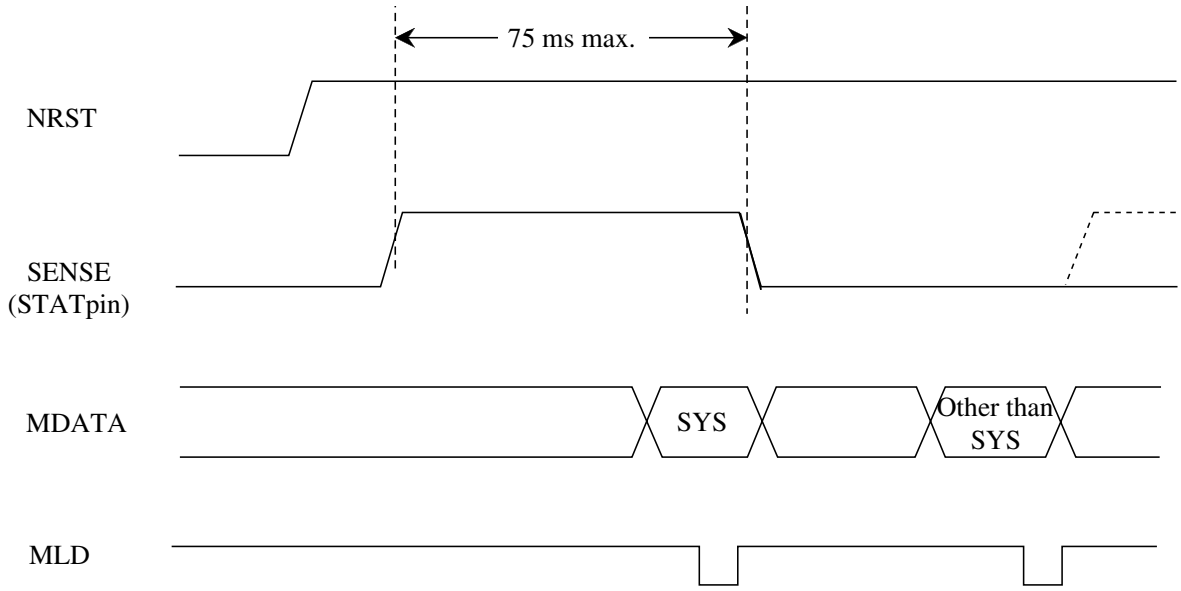


Figure 7-1-3 Timing chart in initial setting

7-1 (4) Data setting for servos

[1] Data write (DTMS)

Various features can be achieved by writing various characteristics of the optical servo system from an external microcomputer to this IC.

DTMS command is used to write the data such as servo parameters.

(Application)

(A) Setting of automatic adjustment value
(B) Setting of the optical servo loop characteristics including the characteristics for anti-vibration
(C) Setting of gain crossover for the optical servo loop
(D) Mode selection for anti-vibration
(E) Various system settings
(F) Various settings for optical servo system
(G) Access command setting

(MDATA format)

D7	D6	D5	D4	D3	D2	D1	D0	: Data
A7	A6	A5	A4	A3	A2	A1	A0	: Address (Label specified)
1	1	1	1	0	0	1	0	: Command (DTMS)

Note)

・Use the DTMS command in the STANDBY or PLAY mode.
・If you write data successively, wait at least 25 µs before each data writing so that the microcomputer finishes DSP processing and becomes ready for writing next data.

[2] Data read (DTSM)

・This IC can read out the parameters such as automatic adjustment results of the optical servo with the DTSM command.

(MDATA format)

A7	A6	A5	A4	A3	A2	A1	A0

: Address (Label specified)

1	1	1	1	0	1	0	0

: Command (DTSM)

(Data output format)

Input an address and command, and after a lapse of at least 25 µs since setting MLD to "H" from "L," input MCLK, thus enabling to read data from STAT pin. (SENSE output)

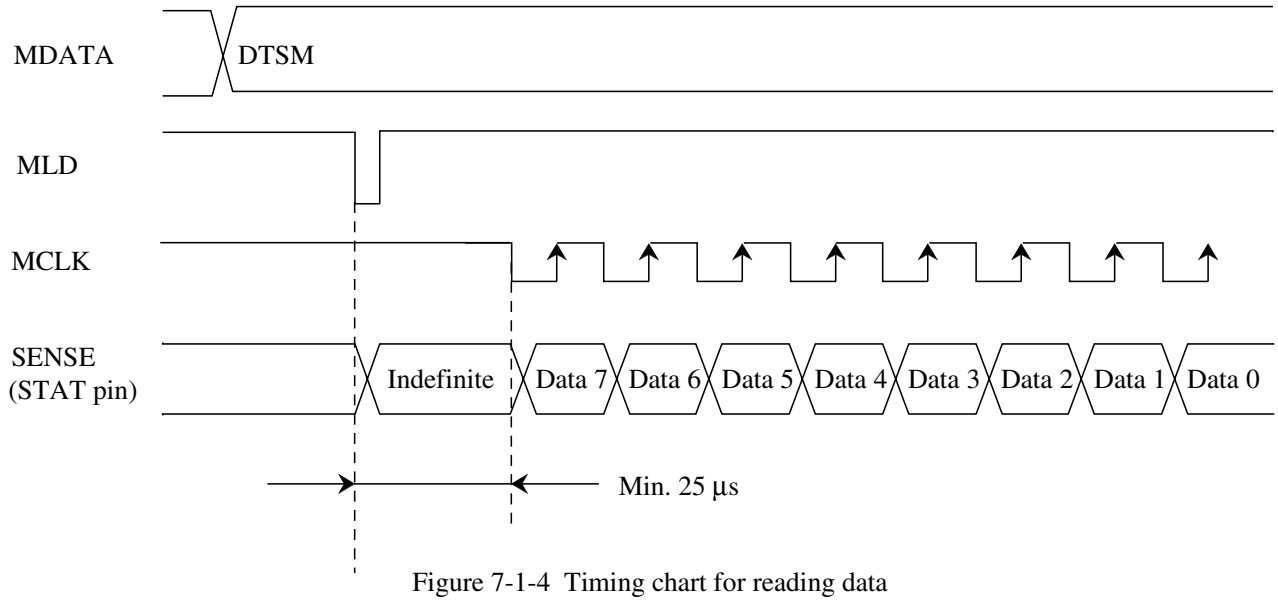


Figure 7-1-4 Timing chart for reading data

Note) Perform either in the STANDBY or PLAY mode.

(List of DTMS/DTSM addresses)

Table 7-1-4 (1)

Address (HEX) (A7 to A0)	Label	Application	Reference page
00	FG0	Focus gain automatic adjustment value in normal-speed mode (for setting use)	23
01	FEXP0	Focus gain automatic adjustment value in normal-speed mode (for setting use)	23
02	FBAL	Focus balance automatic adjustment value	23
03	FOFS	Focus offset automatic adjustment value	23
04	TG0	Tracking gain automatic adjustment value in normal-speed mode (for setting use)	23
05	TEXP0	Tracking gain automatic adjustment value in normal-speed mode (for setting use)	23
06	TBAL	Tracking balance automatic adjustment value	23
07	TOFS	Tracking offset automatic adjustment value	23
08	FC	Focus phase compensation constant	25
09	FR	Focus low-band compensation constant	25
0A	TC	Tracking phase compensation constant	25
0B	TR	Tracking low-band compensation constant	25
0C	FC2	Focus phase compensation constant at vibration	25
0D	FR2	Focus low-band compensation constant at vibration	25
0E	TC2	Tracking phase compensation constant at vibration	25
0F	TR2	Tracking low-band compensation constant at vibration	25
10	GSET	Gain crossover setting	27
11	VSET	Mode selection for anti-vibration	28
12	SET0	System settings	30
13	SET1	System settings	31
14	SET2	System settings	32
16	FES	Focus gain disturbance amplitude	23
17	TES	Tracking gain disturbance amplitude	23
18	CRAM2	Focus search amplitude	38
19	SD	Search direction	38
1A	KS	Kick speed / Kick brake timing	39
1B	TVG	Traverse gain constant in tracking brake operation	40
1C	CRAM3	Fail-safe value for tracking servo	39
1D	CRAM4	Tracking balance disturbance adjustment value	39
1E	SET3	System settings	33
1F	DED0	Traverse drive dead-zone	41

Table 7-1-4 (2)

Address (HEX) (A7 to A0)	Label	Application	Reference page
2B	ECM	Spindle forced acceleration/deceleration output level setting	45
2C	SVOFS	Spindle shaft loss compensation output level setting	45
2D	FG2	Focus gain constant mantissa part at vibration (for setting use)	29
2E	FEXP2	Focus gain constant exponent part at vibration (for setting use)	29
2F	SPG0	Spindle gain setting	45
35	TG2	Tracking gain constant mantissa part at vibration (for setting use)	29
36	TEXP2	Tracking gain constant exponent part at vibration (for setting use)	29
37	TRVG0	Traverse gain setting	43
39	GLF1	Focus gain constant upper limit mantissa part	43
3A	GLF2	Focus gain constant upper limit exponent part	43
3B	GLF3	Focus gain constant lower limit mantissa part	43
3C	GLF4	Focus gain constant lower limit exponent part	43
3D	GLT1	Tracking gain constant upper limit mantissa part	43
3E	GLT2	Tracking gain constant upper limit exponent part	43
3F	GLT3	Tracking gain constant lower limit mantissa part	43
40	GLT4	Tracking gain constant lower limit exponent part	43
49	SETKC	Track count noise elimination width	41
4A	SETTB	System settings	36
4B	KCCNT	Inverted pulse width with tracking brake and servo control turned on	42
		Initial accelerating time with tracking brake turned on	42
6C	FMAX	FE signal maximum value (8-bit 2's complement)	
6D	FMIN	FE signal minimum value (8-bit 2's complement)	
78	KICK	KICK output level	42
79	TRV	Traverse output level	42
7B	VSLT	Vibration detecting level mantissa part	35
7C	SETV1	Soft VDET parameter setting 1	34
7D	SETV2	Soft VDET parameter setting 2	34
80	—	Focus and tracking gains setting for normal gain	37
81	—	Focus and tracking gains setting for forced gain-up	37
AA	—	Software reset	37

※ Do not write illegal data in any of the above addresses, otherwise the existing data in the address is overwritten and the operation of this IC is not guaranteed.

(A) Setting of automatic adjustment value

FG0	(Focus gain mantissa part)	,	TG0	(Tracking gain mantissa part)
FEXP0	(Focus gain exponent part)	,	TEXP0	(Tracking gain exponent part)
FBAL	(Focus balance adjustment value)	,	TBAL	(Tracking balance adjustment value)
FOFS	(Focus offset adjustment value)	,	TOFS	(Tracking offset adjustment value)
FES	(Disturbance amplitude in focus gain adjustment)			
TES	(Disturbance amplitude in tracking gain adjustment)			

Table 7-1-4 (3)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	00	F2	Focus gain constant (FG0) (8-bit mantissa) (1 to 255)	202
D7 D6 D5 D4 D3 D2 D1 D0	01		Focus gain constant (FEXP0) (8-bit exponent) (0 to 7) (Note) (Focus gain constant = mantissa / $2^{8\text{-FEXP0}}$)	2
D7 D6 D5 D4 D3 D2 D1 D0	02		Focus balance constant (FBAL) (8-bit 2' s complement) (−128 to +127)	0
D7 D6 D5 D4 D3 D2 D1 D0	03		Focus offset constant (FOFS) (8-bit 2' s complement) (−128 to +127)	0
D7 D6 D5 D4 D3 D2 D1 D0	04		Tracking gain constant (TG0) (8-bit mantissa) (1 to 255)	150
D7 D6 D5 D4 D3 D2 D1 D0	05		Tracking gain constant (TEXP0) (8-bit exponent) (0 to 7) (Note) (Tracking gain constant = mantissa / $2^{8\text{-TEXP0}}$)	1
D7 D6 D5 D4 D3 D2 D1 D0	06		Tracking balance constant (TBAL) (8-bit 2' s complement) (−128 to +127)	0
D7 D6 D5 D4 D3 D2 D1 D0	07		Tracking offset constant (TOFS) (8-bit 2' s complement) (−128 to +127)	0
D7 D6 D5 D4 D3 D2 D1 D0	16		Disturbance amplitude in focus gain adjustment (FES) (1 to 127)	85
D7 D6 D5 D4 D3 D2 D1 D0	17		Disturbance amplitude in tracking gain adjustment (TES) (1 to 127)	85

(Note) The operation may fluctuate when FEXP0 or TEXP0 setting is 5 or more.

FEXP0/TEXP0 corresponding setting table

MN662783	128	64	32	16
MN662785	1	2	3	4

(B) Setting of the optical servo characteristics including the characteristics for anti-vibration

・Gain constant

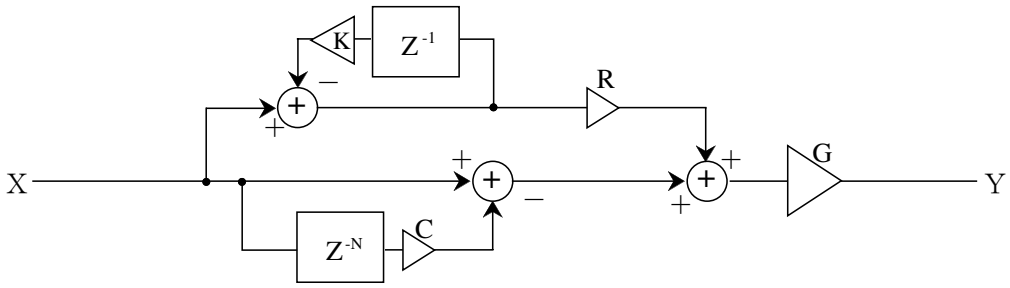
Focus gain mantissa part	FG	Tracking gain mantissa part	TG
Focus gain exponent part	FEXP	Tracking gain exponent part	TEXP

・Phase compensation and low-band compensation constant

Focus phase compensation constant	FC	Tracking phase compensation constant	TC
Focus low-band compensation constant	FR	Tracking low-band compensation constant	TR

The above four constants can be set by writing 8-bit data (0 to 127) directly with the microcomputer command.

Configuration



・f_S of the focus system: 88.2 kHz

・f_S of the tracking system: 88.2 kHz

・f_S of the filter for low-band compensation: 44.1 kHz

$$G(Z) = G\left\{\frac{1}{1-Z^{-1}} \cdot R + (1-C \cdot Z^{-N})\right\}$$

$$G = \frac{TG}{2^{8-TEXP}} \text{ or } \frac{FG}{2^{8-FEXP}} \qquad C = \frac{TC}{128} \text{ or } \frac{FC}{128}$$

$$R = \frac{TR}{2^{15}} \text{ or } \frac{FR}{2^{15}}$$

K=1

N in Z^{-N} can be replaced with :

2 or 1 (by setting bit 1 of SET0) in case of the focus system.

1 in case of the tracking system.

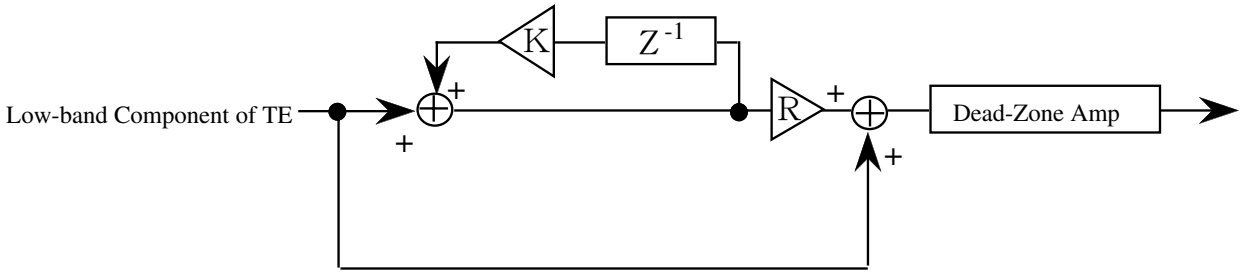
・Setting of loop filter constants

Table 7-1-4 (4)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	08	F2	Focus phase compensation constant : FC (8 bits) (1 to 127)	117
D7 D6 D5 D4 D3 D2 D1 D0	09		Focus low-band compensation constant : FR (8 bits) (1 to 127)	64
D7 D6 D5 D4 D3 D2 D1 D0	0A		Tracking phase compensation constant: TC (8 bits) (1 to 127)	122
D7 D6 D5 D4 D3 D2 D1 D0	0B		Tracking low-band compensation constant : TR (8 bits) (1 to 127)	64
D7 D6 D5 D4 D3 D2 D1 D0	0C		Focus phase compensation constant at vibration : FC2 (8 bits) (1 to 127)	117
D7 D6 D5 D4 D3 D2 D1 D0	0D		Focus low-band compensation constant at vibration : FR2 (8 bits) (1 to 127)	64
D7 D6 D5 D4 D3 D2 D1 D0	0E		Tracking phase compensation constant at vibration : TC2 (8 bits) (1 to 127)	122
D7 D6 D5 D4 D3 D2 D1 D0	0F		Tracking low-band compensation constant at vibration : TR2 (8 bits) (1 to 127)	64

・Setting of the traverse filter

Configuration



Traverse filter sampling frequency＝ 11.02 kHz

$K=1 - 2^{-14}$

$R= 2^{-10}$

・There are three types of dead-zone amps; type A, type B, and type C. They can be selected by setting SET2. The dead-zone width can be specified by setting DED0.

(C) Setting of gain crossover for optical servo loop

Before performing focus and tracking automatic adjustments, gain crossover after automatic adjustment can be determined by writing data to the label name GSET (address: 10h) according to the table below.
In the automatic gain adjustment, disturbance is input to the servo loop, and gain is increased or decreased according to the GSET setting after adjusting the gain so that the feedback gain at the disturbance frequency becomes 0 dB (gain crossover is equal to the disturbance frequency).

(Setting for focus system) Table 7-1-4 (5)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX)	Function (＊ : Setting at reset)
X X X X D3 D2 D1 D0	10	F2	Focus gain at the disturbance frequency of 750 Hz
X X X X 0 1 1 1			Approx. value : −3.92 dB
X X X X 0 1 1 0			Approx. value : −3.36 dB
X X X X 0 1 0 1			Approx. value : −2.80 dB
X X X X 0 1 0 0			Approx. value : −2.24 dB
X X X X 0 0 1 1			Approx. value : −1.68 dB
X X X X 0 0 1 0			Approx. value : −1.12 dB
X X X X 0 0 0 1			Approx. value : −0.56 dB
X X X X 0 0 0 0			＊ Approx. value : 0 dB
X X X X 1 1 1 1			Approx. value : 1.05 dB
X X X X 1 1 1 0			Approx. value : 2.11 dB
X X X X 1 1 0 1			Approx. value : 3.16 dB
X X X X 1 1 0 0			Approx. value : 4.21 dB
X X X X 1 0 1 1			Approx. value : 5.27 dB
X X X X 1 0 1 0			Approx. value : 6.32 dB
X X X X 1 0 0 1			Approx. value : 7.37 dB
X X X X 1 0 0 0			Approx. value : 8.43 dB

(Setting for tracking system) Table 7-1-4 (6)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX)	Function (＊ : Setting at reset)
D7 D6 D5 D4 X X X X	10	F2	Tracking gain at the disturbance frequency of 1 kHz
0 1 1 1 X X X X			Approx. value : −3.92 dB
0 1 1 0 X X X X			Approx. value : −3.36 dB
0 1 0 1 X X X X			Approx. value : −2.80 dB
0 1 0 0 X X X X			Approx. value : −2.24 dB
0 0 1 1 X X X X			Approx. value : −1.68 dB
0 0 1 0 X X X X			Approx. value : −1.12 dB
0 0 0 1 X X X X			Approx. value : −0.56 dB
0 0 0 0 X X X X			＊ Approx. value : 0 dB
1 1 1 1 X X X X			Approx. value : 1.05 dB
1 1 1 0 X X X X			Approx. value : 2.11 dB
1 1 0 1 X X X X			Approx. value : 3.16 dB
1 1 0 0 X X X X			Approx. value : 4.21 dB
1 0 1 1 X X X X			Approx. value : 5.27 dB
1 0 1 0 X X X X			Approx. value : 6.32 dB
1 0 0 1 X X X X			Approx. value : 7.37 dB
1 0 0 0 X X X X			Approx. value : 8.43 dB

(D) Setting for anti-vibration (VSET)

The gain-up amount and gain-up time can be set when VDET is set to "H."
(VDET can be monitored through the EXT1 pin. Refer to 7-1 (5) (I) for details.)

Table 7-1-4 (7)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (＊ : Setting at reset)
X X X X X D2 D1 D0	11	F2	Setting of the focus gain-up amount at vibration
X X X X X 0 0 0			Scale factor : × 1.0 (0 dB)
X X X X X 0 0 1			Scale factor : × 1.125 (+1.0 dB)
X X X X X 0 1 0			Scale factor : × 1.25 (+1.9 dB)
X X X X X 0 1 1			Scale factor : × 1.375 (+2.8 dB)
X X X X X 1 0 0			＊ Scale factor : × 1.5 (+3.5 dB)
X X X X X 1 0 1			Scale factor : × 1.625 (+4.2 dB)
X X X X X 1 1 0			Scale factor : × 1.75 (+4.9 dB)
X X X X X 1 1 1			Scale factor : × 2.0 (+6.0 dB)
X X D5 D4 D3 X X X			Setting of the tracking gain-up amount at vibration
X X 0 0 0 X X X			Scale factor : × 1.0 (0 dB)
X X 0 0 1 X X X			Scale factor : × 1.125 (+1.0 dB)
X X 0 1 0 X X X			Scale factor : × 1.25 (+1.9 dB)
X X 0 1 1 X X X			Scale factor : × 1.375 (+2.8 dB)
X X 1 0 0 X X X			Scale factor : × 1.5 (+3.5 dB)
X X 1 0 1 X X X			Scale factor : × 1.625 (+4.2 dB)
X X 1 1 0 X X X			Scale factor : × 1.75 (+4.9 dB)
X X 1 1 1 X X X			＊ Scale factor : × 2.0 (+6.0 dB)
D7 D6 X X X X X X			Setting of the gain-up time at vibration
0 0 X X X X X X			Time : 23.2 ms
0 1 X X X X X X			Time : 46.4 ms
1 0 X X X X X X			Time : 92.9 ms
1 1 X X X X X X			＊ Time : 185.8 ms

Note) The gain-up amount set by VSET is valid only when FC2 or FR2 for the focus system or TC2 or TR2 for the tracking system is written after VSET setting.
(No operation is performed to set servo parameters in the anti-vibration mode only by VSET setting.)

The gain values can be overwritten when VDET is set to "H."

Table 7-1-4 (8)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1D0	2D	F2	Focus gain constant at vibration (FG2) (8-bit mantissa) (1 to 255)	202
D7 D6 D5 D4 D3 D2 D1D0	2E		Focus gain constant at vibration (FEXP2) (8-bit exponent) (1 to 7) (Focus gain constant = mantissa / $2^{8\text{-FEXP2}}$)	2
D7 D6 D5 D4 D3 D2 D1D0	35		Tracking gain constant at vibration (TG2) (8-bit mantissa) (1 to 255)	150
D7 D6 D5 D4 D3 D2 D1D0	36		Tracking gain constant at vibration (TEXP2) (8-bit exponent) (1 to 7) (Tracking gain constant = mantissa / $2^{8\text{-TEXP2}}$)	1

Note) Be aware that the gain set with VSET applies at the time of fine gain adjustment or writing data to the FC2, FR2, TC2, or TR2.

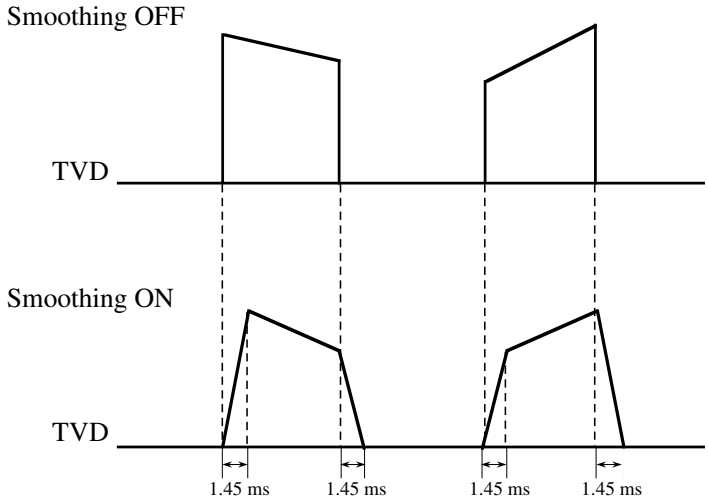
(E) System settings

(E)-1 SET0 setting Table 7-1-4 (9)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (＊ : Setting at reset)
D1 X X X X X X 0 1 X X X X X X 1 1	12	F2	Setting the number of Fo loop filter delay stages ＊ 2nd-order (Z^{-2}) 1st-order (Z^{-1})
D3 D2 X X X X 0 0 X 1 X X X X 0 1 X 1 X X X X 1 0 X 1 X X X X 1 1 X 1			Setting of forced brake operation time OFF ON (5.8 ms) ON (11.6 ms) ＊ ON (23.2 ms)
D5 D4 X X 0 0 X X X 1 X X 0 1 X X X 1 X X 1 0 X X X 1 X X 1 1 X X X 1			Setting of convergence gain during tracking balance adjustment ×1/8192 ＊ ×1/4096 ×1/2048 ×1/1024
D6 X 0 X X X X X 1 X 1 X X X X X 1			Tracking balance adjustment output ＊Conventional method Inverted polarity
D7 0 X X X X X X 1 1 X X X X X X 1			TVD output smoothing OFF ＊ ON

TVD output

Example of the TVD intermittent drive is as follows.



(E)-2 SET1 setting

Table 7-1-4 (10)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (＊ : Setting at reset)
D0 X X X X X X X 0 X X X X X X X 1	13	F2	TVD output at the time of kick pulse output in the traverse stop state TVD output ＊No TVD output
D1 X X X X X X 0 X X X X X X X 1 X			Pull-in method when turning focus on from off Conventional method ＊High-speed pull-in
D2 X X X X X 0 X X X X X X X 1 X X			High-speed kickback ON/OFF Note) ＊ON OFF
D4 X X X 0 X X X X X X X 1 X X X X			Focus offset adjustment method With vibration ＊Without vibration
D5 X X 0 X X X X X X X 1 X X X X X			Focus offset adjustment method ＋direction (Same as MN66271) ＊－direction
D6 D3 X 0 X X 0 X X X X 0 X X 1 X X X X 1 X X 0 X X X X 1 X X 1 X X X			Wait time after TCNT ＊ 50 ms 100 ms 0 ms 10 ms
D7 0 X X X X X X X 1 X X X X X X X			DAC output limiter (FABC, TABC) OFF ＊ON

Note) It is recommended to turn off the high-speed kickback function while the anti-shock memory control function is in use.

(E)-3 SET2 setting

Table 7-1-4 (11)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (＊ : Setting at reset)
D1 D0 X X X X X X 0 X X X X X X X 1 0 X X X X X X 1 1	14	F2	Traverse dead-zone amp Normal (Type A) ＊ ＋ side only (Type B) － side only (Type C)
D2 X X X X X 0 X X X X X X X 1 X X			Tracking offset adjustment wait time None ＊ 30 ms
D3 X X X X 0 X X X X X X X 1 X X X			Convergence judgement condition for tracking balance adjustment ＊ ±2 LSBs at TBAL output stage ±1 LSB at TE input stage
D5D4 X X 0 0 X X X X X X 0 1 X X X X X X 1 0 X X X X X X 1 1 X X X X			Focus balance adjustment convergence gain ＊ 1／8 1／4 1／32 1／16
D6 X 0 X X X X X X X 1 X X X X X X			Disc detection, focus rough gain adjustment frequency 5.4 Hz ＊ 2.6 Hz
D7 0 X X X X X X X 1 X X X X X X X			Traverse intermittent drive ＊ Output enabled Output disabled

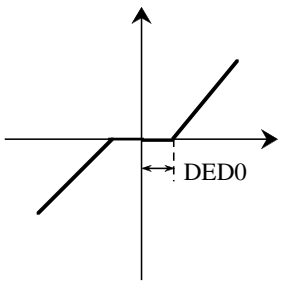


Figure 1 Traverse dead-zone amp Type A

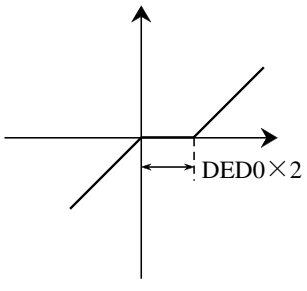


Figure 2 Traverse dead-zone amp Type B

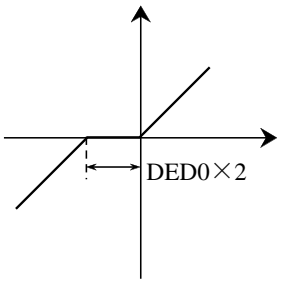


Figure 3 Traverse dead-zone amp Type C

Note) Refer to 7-1 (4) (F)-6 for the DED0 setting.

(E)-4 SET3 setting

Table 7-1-4 (12)

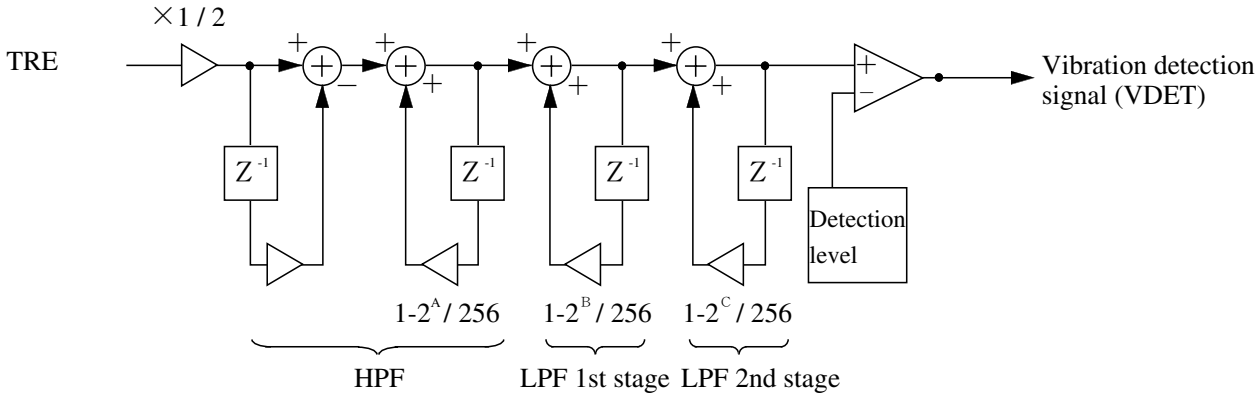
Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (＊ : Setting at reset)
D1 X X X X X X 0 0 X X X X X X 1 0	1E	F2	Focus balance adjustment convergence condition ＊ ±15 LSBs ±7 LSBs
D2 X X X X X 0 X 0 X X X X X 1 X 0			Cancellation of focus balance adjustment Reset to the initial value at the start of adjustment ＊ The adjusting value is on hold
D3 X X X X 0 X X 0 X X X X 1 X X 0			Tracking rough gain adjustment time ＊ 134 ms 319 ms
D4 X X X 0 X X X 0 X X X 1 X X X 0			Focus search mode ＊ Conventional mode Amplitude: 1/4
D6 X 0 X X X X X 0 X 1 X X X X X 0			Focus balance adjustment output ＊ Positive polarity (Conventional mode) Negative polarity
D7 0 X X X X X X 0 1 X X X X X X 0			Focus search frequency 1.3 Hz ＊ 2.6 Hz

(E)-5 Setting of soft VDET

(Setting of vibration detection bandpass filter constant) Table 7-1-4 (13)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
X X X X D3 D2 D1 D0	7C	F2	Setting of HPF constant A SETV1〔D3 to D0〕 (0 to 7)	3
D7 D6 D5 D4 X X X X			Vibration detection level exponent part n setting SETV1〔D7 to D4〕 (0 to 7)	1
X X X X D3 D2 D1 D0	7D		Setting of LPF 2nd stage constant C SETV2〔D3 to D0〕 (0 to 7)	5
D7 D6 D5 D4 X X X X			Setting of LPF 1st stage constant B SETV2〔D7 to D4〕 (0 to 7)	5

* See next page for the setting of vibration detection level.

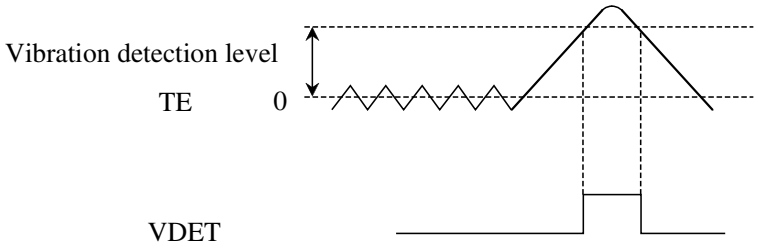


* Sampling frequency for filter arithmetic operation: 11.02 kHz

(Setting of vibration detection level)

Table 7-1-4 (14)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
1 D6 D5 D4 D3 D2 D1 D0	7B	F2	Setting of VDET detecting TE threshold level (Mantissa part) VSLT (128 to 255)	230



Vibration detection level : $\pm VSLT \times 2^n$

n=SETV1〔D7 to D4〕

(E)-6 SETTB setting

Table 7-1-4 (15)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function (＊ : Setting at reset)
D1 0 X 0 X X 0 0 X 0 X 0 X X 0 1 X	4A	F2	Low-band compensation during tracking brake operation Yes ＊ No
D3 0 X 0 X 0 0 X X 0 X 0 X 1 0 X X			DO countermeasure during KICK operation No ＊ Yes
D6 0 0 0 X X 0 X X 0 1 0 X X 0 X X			Hunting countermeasure for focus balance adjustment No ＊ Yes

(E)-7 Forced gain-up setting

The IC can be in forced gain-up mode by accessing the data in 81h address.
This mode is reset by accessing the data in 80h address.

Table 7-1-4 (16)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function
X X X X X X X X	81	F2	Focus / tracking forced gain-up setting (Data is disabled.)
X X X X X X X X	80		Focus / tracking normal gain (Data is disabled.)

Note) ・The status of the VDET can be monitored through the EXT1 pin. For details, refer to 7-1 (5) (I).
・Sending a fine gain adjustment command resets the gain to the normal value.

(E)-8 Software reset

Accessing the data in AAh address initializes servo processing.
(DSP processing starts from the top address.)

Table 7-1-4 (17)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function
X X X X X X X X	AA	F2	Software reset (Data is disabled.)

Note) Only the digital servo section is reset in the software reset operation.

(F) Settings for optical servo system

(F)-1 Focus search setting Table 7-1-4 (18)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	18	F2	Focus search amplitude (CRAM2) setting 8-bit data (p-p) (40 to 127)	96
D0 X X X X X X X 0 X X X X X X X 1	19		Focus search/disc detection direction (SD) setting *FOD decrement FOD increment	0
D2 X X X X X 0 X X X X X X X 1 X X			Max./Min. FE value teaching during focus search *ON OFF	

Note) In focus search/disc detection direction setting, a value of SD will change automatically according to execution of a focus search/disc detection. Consequently, the values written by initial setting and DTMS may have changed when they are read out with DTSM. If you want to perform a focus search/disc detection from the same direction every time, it is necessary to set with DTMS every time before the focus search/disc detection. (Set D0 of SD only.) Check the value of SD with DTSM in the writing operation of SD, and confirm that only the value of set bit of D0 has changed.

Note) There will be no focus pull-in operation during the first excitation period (between the first peak and second peak of triangular FOD output) of the IC in focus search operation right after the system starts. The teaching of the maximum and minimum values (FMAX and FMIN) of the FE signal will be, however, conducted. The focus will be pulled in when the S-shape signal is detected after the first excitation period.
Once the focus is pulled in, the servo DSP automatically sets SD D2 to 1. Then the focus will be pulled in when the S-curve signal is detected after the first peak of excitation.
After offset and focus balance adjustments, SD D2 will be automatically set to 0 and the teaching of FMAX and FMIN will be conducted again.

(F)-2 Setting of tracking servo fail-safe value (CRAM3) Table 7-1-4 (19)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	1C	F2	Fail-safe value clip level 8-bit data (0 to 127) Low-band component of drive output in the tracking brake mode is clipped at the specified value.	36

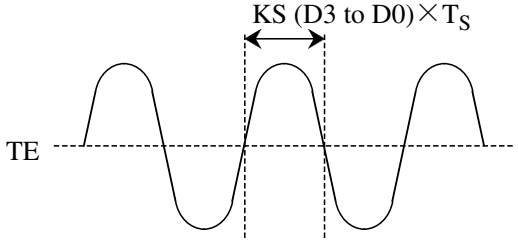
(F)-3 Setting of disturbance amplitude (CRAM4) in tracking balance adjustment mode Table 7-1-4 (20)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	1D	F2	Disturbance amplitude (one side) 8-bit data (0 to 127) Amplitude of the disturbance waves injected in the tracking balance adjustment mode is set. Actual disturbance amplitude is 1/8×CRAM4.	36

(F)-4 KICK setting Table 7-1-4 (21)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
X X X X D3 D2 D1 D0	1A	F2	KICK speed (KS) setting 4-bit data (6 to 15)	6
D7 D6 D5 D4 X X X X			KICK brake timing (OFDE) setting 4-bit data (0 to 15)	0

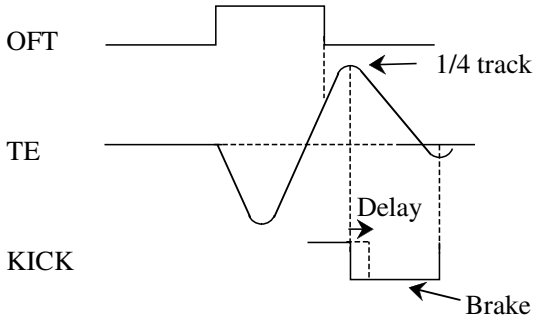
・TE cycle in the speed control mode is determined by the KICK speed setting.



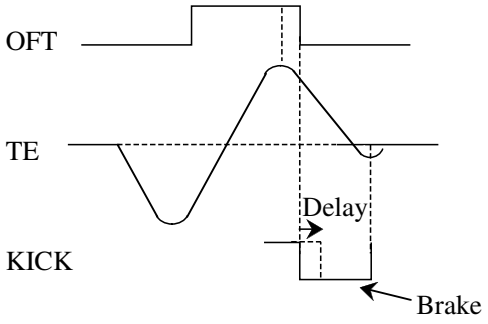
T_S : 11.3 ms

・KICK brake output timing delay time is set in the KICK brake timing setting.
(1 count＝T_S delay) Setting value＝0: No delay

① When OFT is turned to "L" before reaching a position of 1/4 track



② When OFT is turned to "L" after passing the position of 1/4 track



(F)-5 Traverse drive constant in tracking brake (TVG) Table 7-1-4 (22)

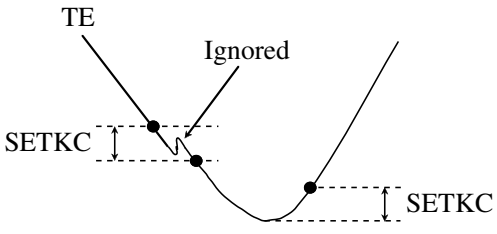
Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
X X X X D3 D2 D1 D0	1B	F2	Traverse drive constant TVG (1 to 15) Only in the tracking brake, traverse will be driven with the traverse error multiplied by the specified constant.	15

(F)-6 Traverse drive dead zone setting (DED0) Table 7-1-4 (23)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	1F	F2	Traverse drive dead zone setting (one side) DED0 (0 to 127)	112

(F)-7 TE noise rejection width setting at track count (SETKC) Table 7-1-4 (24)

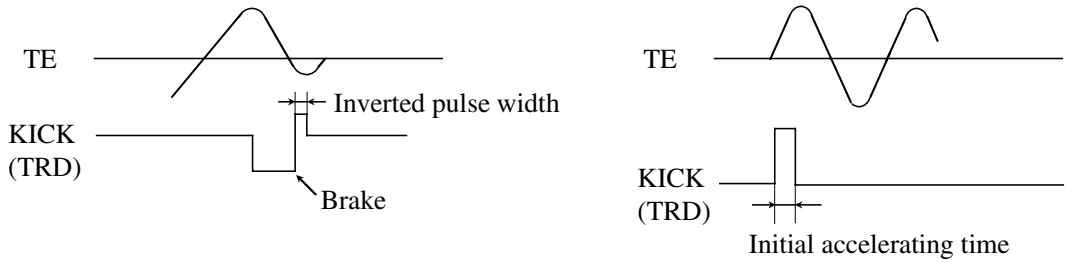
Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	49	F2	TE noise rejection width setting at track count SETKC (0 to 127)	3



※ When the TE slope is inverted and reaches the level of the SETKC, it is regarded that the TE slope has actually changed.

(F)-8 KICK pulse width setting (KCCNT) Table 7-1-4 (25)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 X X X X	4B	F2	Inverted pulse width during servo pull-in operation in KICK operation. (Set value × T_S + T_S/2) µs	1
X X X X D3 D2 D1 D0			KICK pulse initial accelerating time (0 to 15) (Set value × T_S) µs T_S : 11.3 µs	9



(F)-9 KICK pulse level setting (KICK) Table 7-1-4 (26)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	78	F2	KICK pulse level setting KICK (0 to 127)	22

(F)-10 Traverse output gain setting (TRV) Table 7-1-4 (27)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
0 D6 D5 D4 D3 D2 D1 D0	79	F2	Traverse output gain setting TRV (0 to 127)	65

(F)-11 Traverse fine adjustment gain setting (TRVG0) Table 7-1-4 (28)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	37	F2	Traverse gain (0 to 127) TRVG0/16	18

Set the above value after setting the TRV value.

(F)-12 Setting of automatic adjustment range

The limits of adjustment values can be set arbitrarily in the range of $1/2^8$ to 255/2 (or −48 dB to +42 dB).
In order to ensure automatic gain convergence within a limited, narrow adjustment range to prevent excessive gain change, which had difficulty in convergence control, however, make sure that the maximum automatic adjustment range is ±9 dB on the basis of the gain set value.

・Tracking gain
Automatic adjustment range GLT3/GLT4 to GLT1/GLT2 Table 7-1-4 (29)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	3D	F2	Tracking gain upper limit GLT1 (mantissa) (128 to 255)	212
0 0 0 0 D3 D2 D1 D0	3E		GLT2 (exponent) (0 to 7) Upper limit: GLT1/2^{8-GLT2}	2
D7 D6 D5 D4 D3 D2 D1 D0	3F		Tracking gain lower limit GLT3 (mantissa) (128 to 255)	106
0 0 0 0 D3 D2 D1 D0	40		GLT4 (exponent) (0 to 7) Lower limit: GLT3/2^{8-GLT4}	0

・Focus gain
Automatic adjustment range GLF3/GLF4 to GLF1/GLF2 Table 7-1-4 (30)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	39	F2	Focus gain upper limit GLF1 (mantissa) (128 to 255)	143
0 0 0 0 D3 D2 D1 D0	3A		GLF2 (exponent) (0 to 7) Upper limit: GLF1/2^{8-GLF2}	4
D7 D6 D5 D4 D3 D2 D1 D0	3B		Focus gain lower limit GLF3 (mantissa) (128 to 255)	144
0 0 0 0 D3 D2 D1 D0	3C		GLF4 (exponent) (0 to 7) Lower limit: GLF3/2^{8-GLF4}	1

(G) Access command setting

Table 7-1-4 (31)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Function
D15 0 0 0 0 0 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	F1	KICK-count setting/KICK operation start
0 0 0 0 0 0 Kick-count setting (other than 0)		Inner track KICK operation
1 0 0 0 0 0		Outer track KICK operation
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0	F3	Track-count setting / Track counting start
0 Track-count setting		Inner track counting
1		Outer track counting

Note) The track-count means the number of tracks until the brake operation start point is reached.
TE sampling frequency in track counting is 176.4 kHz. Care must be taken so that the maximum TE frequency in track counting does not exceed one fourth of the sampling frequency.

(H) Spindle related settings

(H)-1 Setting of spindle forced acceleration/deceleration (ECM) output level Table 7-1-4 (32)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	2B	F2	ECM acceleration (ACC) level setting ECM (0 to 127)	127

* At the time of deceleration (BREAK), 2's complement of the above setting will be output.
* If the ECM value is set to 127, 128 (ALLH or ALLL) will be output.

(H)-2 Setting of spindle shaft loss compensation value Table 7-1-4 (33)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	2C	F2	Shaft loss compensation value setting SVOFS (-128 to 0)	0

* The shaft loss compensation value will be enabled only when the spindle is in free running condition (STOP). No compensation will be enabled with this value set to 0.

(H)-3 Spindle fine adjustment gain setting (SPG0) Table 7-1-4 (34)

Data (D7 to D0)	Address (HEX) (A7 to A0)	Command (HEX) (B7 to B0)	Function	Setting at reset
D7 D6 D5 D4 D3 D2 D1 D0	2F	F2	Spindle gain (0 to 127) SPG0／16	22

Set the above value after setting the spindle gain with the 45h command.

7-1 (5) Data setting for signal processing section

(A) Audio control

Table 7-1-5 (1)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X X X X X X X X 0 0 X X X X X X X X X X X X X X 0 1 X X X X X X X X X X X X X X 1 0 X X X X X X X X X X X X X X 1 1	41	BIMAIN, BISUB	Bilingual setting ＊Normal stereo L-ch monaural R-ch monaural L- and R-ch reverse
X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X		INV	Audio output polarity selection ＊Normal Inverted
X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 0 X X X X X X X X X X X X X X X 1 1 X X X		MEMP	Emphasis control (Note 1) ＊De-emphasis connected directly Forced ON Forced OFF
X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X		DEPSEL	Serial data output selection ＊Before general attenuation and de-emphasis processing After general attenuation and de-emphasis processing
X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X		SMUTE	Internal serial data muting ＊Disabled Enabled Note) Serial data input to the anti-shock memory controller will be muted.
X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X		LRINV	Selection of polarity of LRCK for DF input ＊Normal (L-ch : H) Inverted
X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X		XBS	XBS mode selection ＊Disabled Enabled
X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X		ASC	ASC mode selection ＊Disabled Enabled
X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X		LIVE	LIVE mode selection ＊Disabled Enabled
X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X X X X		AUDIO1, AUDIO2	Serial data format selection ＊AUDIO mode 1 AUDIO mode 2
X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X X X X X		XMUTE	Serial data output muting ＊Disabled Enabled
X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X X X X X X		MMUTE	Audio output muting ＊Disabled Enabled

Note 1) Care must be taken during the anti-shock memory control operation since the control timing must be shifted based on the remaining memory though it is not needed during the normal operation.

(B) Digital audio interface control

Table 7-1-5 (2)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊: Setting at reset)
X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 0 X X X X X X X X X X X X X X 1 1	42	UBITC	Bit U control ＊LDON control (Inverted LDON) Output enabled Output fixed at high level
X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X		COPYI	Generation status bit setting ＊ 0 setting 1 setting
X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X		TXVSEL	Bit V control 1 ＊High level while the signal is attenuated Signal attenuation ignored Note 1) Soft muting is included. Note 2) Both levels will be high with the gain set to −∞ dB.
X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X		TMUTE	Output data muting ＊Disabled Enabled Note 1) Only audio data is fixed at 0. Note 2) The bit V level is high.
X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X		IPDISEN	Bit V control 2 ＊High level when the level of IPFLAG is high IPFLAG ignored
X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X		TXDSEL	Output speed selection ＊Normal speed 2x speed Note 1) Available only if the anti-shock memory controller is turned off in 2x-speed playback mode. Note 2) Audio signal will be output at 2x-speed as well.
X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X		VFREE	Bit V control 3 ＊The level will be high while the signal is attenuated (including the gain setting to −∞dB) in DMUTE condition. Signal attenuation (including the gain setting to −∞ dB) with DMUTE condition ignored.
X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X		XSEL	Output control ＊Enabled Fixed at low level
X X X X X X 0 X X X X X X X X X X X X X X X 1 X X X X X X X X X		CATC	Category code setting ＊CD mode General mode
X X X X 0 0 X X X X X X X X X X X X X X 0 1 X X X X X X X X X X X X X X 1 0 X X X X X X X X X X X X X X 1 1 X X X X X X X X X X		CFS1, CFS2	Clock precision setting ＊Standard mode Variable pitch mode High precision mode Not defined

(C) Attenuation control

Table 7-1-5 (3)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X X D7 D6 D5 D4 D3 D2 D1 D0	44	MCNT(7:0)	Attenuation level setting Note) The attenuation level is set to n/256. Initially set to 40 (HEX).
X X X X X X 0 0 X X X X X X X X X X X X X X 0 1 X X X X X X X X X X X X X X 1 0 X X X X X X X X X X X X X X 1 1 X X X X X X X X		ATT, MUTEM	＊Normal (0 dB) Soft muting Digital attenuation Soft attenuation

(D) Spindle control 2

Table 7-1-5 (4)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X 0 X 0 X X 0 0 0 0 X X X 0 X X X 0 X 0 X X 0 0 0 0 X X X 1 X X X 0 X 0 X X 0 0 0 1 X X X 0 X X X 0 X 0 X X 0 0 0 1 X X X 1	45	FO1SEL, FO2SEL	f_0 frequency setting ＊ 24 Hz 6 Hz 12 Hz 3 Hz
X X X 0 X 0 X X 0 0 0 X X 0 0 X X X X 0 X 0 X X 0 0 0 X X 0 1 X X X X 0 X 0 X X 0 0 0 X X 1 0 X X X X 0 X 0 X X 0 0 0 X X 1 1 X		SG0, SG1	Loop gain setting ＊×1 ×2 ×4 ×1/2
X X X 0 X 0 X 0 0 0 0 X X X X X X X 0 X 0 X 1 0 0 0 X X X X X		PCINV	PC output polarity selection ＊Normal (ON at low level) Inverted
X X X 0 X 0 0 X 0 0 0 X X X X X X X X 0 X 0 1 X 0 0 0 X X X X X		CLVSEL	Selection of CLV mode transition condition (from rough to CLV) ＊ RESY: High level and rpm condition (±4.6%) RESY: High level Note) Transition from CLV to rough mode is enabled under the condition of BSSEL failure.
X X X 0 0 0 X X 0 0 0 X X X X X X X X 0 1 0 X X 0 0 0 X X X X X		JFMODE	Analog jitter-free mode ＊Disabled Enabled
X X 0 0 X 0 X X 0 0 0 X X X X X X X 1 0 X 0 X X 0 0 0 X X X X X		ACCFIX	Spindle fixed in a single direction (for acceleration only) ＊Disabled Enabled
X 0 X 0 X 0 X X 0 0 0 X X X X X X 1 X 0 X 0 X X 0 0 0 X X X X X		KILL	Signal processing clock stop ＊Disabled Enabled
0 X X 0 X 0 X X 0 0 0 X X X X X 1 X X 0 X 0 X X 0 0 0 X X X X X		CKSTOP	Oscillation stop ＊Disabled Enabled Note) The IC is reset and stops.

(E) PWM output control (Optical servo system) Table 7-1-5 (5)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X X X X 0 0 X X 0 0 X X X X X X X X X X 0 0 X X 0 1 X X X X X X X X X X 0 0 X X 1 0 X X X X X X X X X X 0 0 X X 1 1	46	FBAL1E, FBAL2E	FBAL charge pump current source control Stop ＊×1 ×1/2 ×3/2
X X X X X X X X X X 0 0 0 0 X X X X X X X X X X X X 0 0 0 1 X X X X X X X X X X X X 0 0 1 0 X X X X X X X X X X X X 0 0 1 1 X X		TBAL1E, TBAL2E	TBAL charge pump current source control Stop ＊×1 ×1/2 ×3/2
X X X X X X X X 0 X 0 0 X X X X X X X X X X X X 1 X 0 0 X X X X		MCFSEL	Noise filter for microcomputer interface ＊Enabled Disabled

(F) Playback speed control

Table 7-1-5 (6)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1	49	DSEL	2x-speed playback selection ＊Normal speed 2x speed
X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X		QSEL	4x-speed playback selection (Note 4) ＊Normal speed 4x speed
X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X		OVERDRV	Overdrive mode (Note 4) ＊Disabled Enabled Note 1) Constantly 1.5x speed based on the speed set with DSEL and QSEL. Note 2) Available in jitter-free mode only.
X X X X X X X X X 0 0 0 X X X X X X X X X X X X X 0 0 1 X X X X X X X X X X X X X 0 1 0 X X X X X X X X X X X X X 0 1 1 X X X X X X X X X X X X X 1 0 0 X X X X X X X X X X X X X 1 0 1 X X X X X X X X X X X X X 1 1 0 X X X X X X X X X X X X X 1 1 1 X X X X		SVPC(2:0)	Spindle speed change rate setting ＊×1 ×15/16 ×14/16 ×13/16 ×12/16 ×11/16 ×10/16 × 9/16 Note 3) Available in jitter-free mode only.
X X X X 0 X X X X X X X X X X X X X X X X 1 X X X X X X X X X X X X		VCOE	VCO control for jitter-free ＊OFF Oscillation ON
X X 0 X X X X X X X X X X X X X X X X 1 X X X X X X X X X X X X X X		CPOFF	Charge pump current source stop (for jitter-free) ＊Disabled Enabled

Note 4) If the anti-shock memory controller is turned on, maximum 2.25x-speed playback in decompression mode and maximum 3x-speed playback in compression mode are guaranteed with the jitter-free function turned on.

(G) DO control

Table 7-1-5 (7)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1	4A	DSLDO	DSL's DO processing ＊Enabled Disabled
X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X		CLVDO	Spindle's DO processing ＊Enabled Disabled
X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X		PLLDO	PLL's DO processing ＊Enabled Disabled
X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1		WGEN	DO with faults processing ＊Enabled Disabled

(H) PLL control

Table 7-1-5 (8)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X 0 X X X X X X X X X X 0 0 X X 0 X X X X X X X X X X 0 1 X X 0 X X X X X X X X X X 1 0 X X 0 X X X X X X X X X X 1 1	4B	PLLG1, PLLG2	PLLF current setting ＊×1 (Conventional setting) ×5/4 ×1/2 ×3/4
X X 0 X X X X X X X X X 0 X X X X 0 X X X X X X X X X 1 X X		PCKG	VCO frequency selection ＊×1/2 ×1
X X 0 X X X X X X X X X 0 X X X X X 0 X X X X X X X X X 1 X X X		IROFF	I_{REF} current shut off ＊Normal Shut off
X X 0 X X X X X X X X 0 X X X X X X 0 X X X X X X X X 1 X X X X		PLHLD	PLLF current shut off by tracking failure ＊Disabled Enabled
X X 0 X X X X X X X 0 X X X X X X 0 X X X X X X X 1 X X X X		DET5T	Frequency pull-in method selection ＊2T detection 5T detection
X X 0 X X X D9 D8 D7 D6 X X X X X X		FL02,FL04, FL08,FL16	Pull-in time setting with 2T or 5T detected Calculation formula : 9×32+nD8× 6+ D7× +nD6× + (pck) Note) Initially set to 32 pck
X X 0 X X 0 X X X X X X X X X X X X 0 X X 1 X X X X X X X X X X		FH32	Pull-in time setting with 12T detected ＊64 pck 32 pck
X X 0 0 X X X X X X X X X X X X X X 0 1 X X X X X X X X X X X X		PLLG	Forced double current setting for phase comparison ＊Disabled Enabled
0 0 0 X X X X X X X X X X X X X 0 1 0 X X X X X X X X X X X X X 1 0 0 X X X X X X X X X X X X X 1 1 0 X X X X X X X X X X X X X		PLLG3, PLLG4	Frequency comparison current rate selection ＊×1 ×5/4 ×1/2 ×3/4

(I) I/O control 1

Table 7-1-5 (9)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1	4C	TXT2	CD-TEXT data output pin selection ＊(SUBC, SBCK, NCLDCK) (TXTD, TXTCLK, DQSY)
X X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X		SROUT2	Serial output pin selection ＊(SUBC, SBCK, NCLDCK) (SRDATA, LRCK, BCLK)
X X X X X X X X X X X X X 0 X X X X X X X X X X X X X X X 1 X X		EXT12SEL	EXT1 and EXT2 output pins selection ＊(EXT1, EXT2) (VDET, EFM)
X X X X X X X X X X X X 0 1 X X X X X X X X X X X X X X 1 1 X X		PCKOUT	EXT1 output pin selection 2 ＊VDET PCK Note) Enabled only when the level of EXT12SEL is high.

(J) DSL unbalance compensation control

Table 7-1-5 (10)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X 0 1 X X X X X 0 X X 0 X X X X X 0 1 X X X X X 1 X X 0	4D	DSLBSEL	EFM or SRF selection ＊EFM SRF
X X X X X 0 1 X 0 0 X X X X X 0 X X X X X 0 1 X 0 1 X X X X X 0 X X X X X 0 1 X 1 0 X X X X X 0 X X X X X 0 1 X 1 1 X X X X X 0		DSLB1E, DSLB2E	Charge pump current source control ＊Shut off × 1 × 1/2 × 3/2
X X X X X 0 1 0 X X X X X X X 0 X X X X X 0 1 1 X X X X X X X 0		DSLBEN	Compensation value counter operation control ＊Previous value kept on hold Compensation value taken in

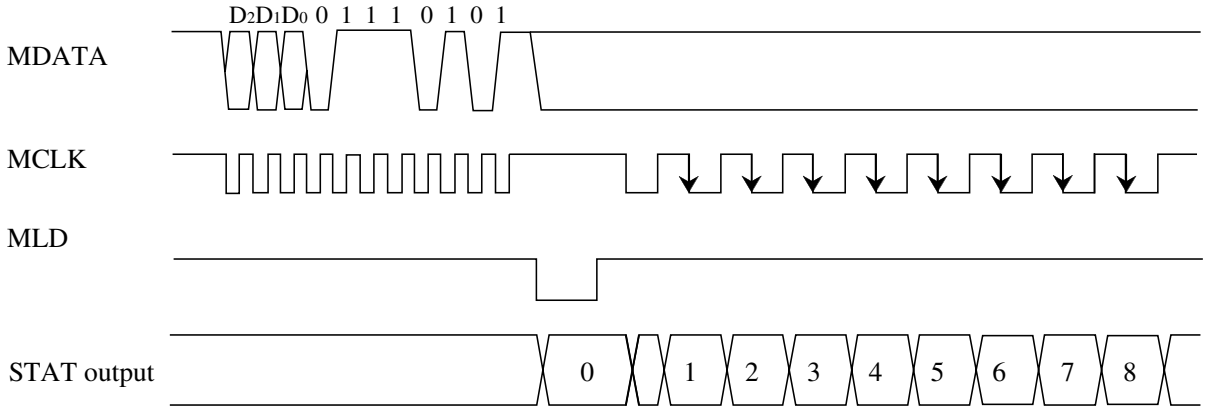
(K) I/O control 2

Table 7-1-5 (11)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (∗ : Setting at reset)
X X X 0 0 X X X X X X X 0 X X 0 X X X 0 0 X X X X X X X 0 X X 1	4E	IOSTOP	Output pin fixed at low level Disabled ∗ Enabled Note 1) Enabled pins: SRDATA, LRCK, BCLK, IPFLAG, SUBC, NCLDCK Note 2) Serial input mode is activated if IOSTOP is disabled. EXT0,EXT1,EXT2 RDATA,LRCK,BCLK
X X X 0 0 X X X X X X X 0 X 0 X X X X 0 0 X X X X X X X 0 X 1 X		MCMSEL	SMCK frequency selection 8.4672 MHz ∗ 4.2336 MHz
X X X 0 0 X X X X X X X 0 0 X X X X X 0 0 X X X X X X X 0 1 X X		DFSEL	DF input selection ∗ Input bypassing the anti-shock memory controller Input from the anti-shock memory controller
X X X 0 0 X X X X X X X 0 X X X X X X 0 0 X X X X X X X 1 0 X X X		OFTSEL	Off-track noise filter ∗ Disabled Enabled
X X X 0 0 X X X X X X 0 X 0 X X X X X X 0 0 X X X X X X 1 X 0 X X X		EXT0SEL	EXT0 pin selection ∗ Normal Serial monitor (for evaluation)
X X X 0 0 X X X X X 0 X X 0 X X X X X X 0 0 X X X X X 1 X X 0 X X X		DSLDR	DRF pin control ∗ Disabled Enabled
X X X 0 0 X X X X 0 X X X 0 X X X X X X 0 0 X X X X 1 X X X 0 X X X		RSEL	RSEL selection Bright levelÅFLow ∗ Bright level : High
X X X 0 0 X 0 0 X X X X 0 X X X X X X 0 0 X 1 0 X X X X 0 X X X X X X 0 0 X X 1 X X X X 0 X X X		MCOM4E BLKCKSEL	BLKCK and SUBQ pins selection ∗ (BLKCK, SUBQ) (ZBLKCK, SUBQ) (DQSY, TXTD) Note) ZBLKCK:Interpolation BLKCK, TXTD:CD-TEXT data
X X X 0 0 0 X X X X X X 0 X X X X X X 0 0 1 X X X X X X 0 X X 0		MPEGIF	Serial output mode selection ∗ Normal Serial output mode Note) DMUTE,SUBQ,SQCK → RDATA,LRCK,BCLK
X X 0 0 0 X X X X X X X 0 X X X X X 1 0 0 X X X X X X X 0 X X X		IPSEL	IPFLAG pin selection ∗ Normal CLVS
X 0 X 0 0 X X X X X X X 0 X X X X 1 X 0 0 X X X X X X X 0 X X X		FLAGSEL	FLAG pin selection ∗ Normal Serial monitor (for evaluation)
0 X X 0 0 X X X X X X X 0 X X X 1 X X 0 0 X X X X X X X 0 X X X		FLAGFIX	FLAG0 output fixed ∗ Disabled Enabled Note) FLAG0 is always output from FLAG pin.

(L) STAT pin control Table 7-1-5 (12)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
XXXX XXXX XXXX XXXX	70		STAT pin output selection ＊ : CRC
XXXX XXXX XXXX XXXX	71		: RESY
XXXX XXXX XXXX XXXX	72		: CLVS
XXXX XXXX XXXX XXXX	73		: NTTSTOP
XXXX XXXX XXXX XXXX	74		: SQOK
XXXX XXXX XXXX XXXX	76		: BSSEL
XXXX XXXX XXXX XXXX	77		: FCLV
XXXX XXXX XXXX XXXX	79		: SUBQ (SQCK sync) / TXTDAT
XXXX XXXX XXXX XXXX	7A		: SUBQ (MCLK sync) / TXTDAT
XXXX XXXX XXXX XXXX	7B		: ZDET (Zero data detection)
D2D1 XXXX XXXX XXXX X0 0 X XXXX XXXX XXXX X0 1 X XXXX XXXX XXXX X1 0 X XXXX XXXX XXXX X1 1 X	75		STAT pin output setting ＊STAT pin output： 0. FLAG6 0. SENSE 0. NFLOCK 0. NTLOCK STAT pin output mode selection by MCLK (excluding the setting of SENSE(01)) 1. FLAG6 2. SENSE 3. NFLOCK 4. NTLOCK 5. SQOK 6. CRC 7. CLVS 8. NTTSTOP
D0 XXXX XXXX XXXX XXX0 XXXX XXXX XXXX XXX1			Clearing FLAG6 output from STAT pin ＊Disabled Enabled (Reset of FLAG6)
XXXX XXXX XXXX XXXX	7E		Disc rotation speed data output from STAT pin (8-bit data)



Timing chart of STAT pin output mode selection by MCLK

7-1 (6) Data setting for anti-shock memory controller

[1] Data write

(A) Memory system command

Table 7-1-6 (1)

Data (D7 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X 0 X X X X X X X 1	80	MSON	＊ Memory system stop Memory system run
X X X X X X 0 X X X X X X X 1 X		WAQV	＊ Q-data disabled Q-data enabled
X X X X 0 0 X X X X X X 0 1 X X X X X X 1 0 X X X X X X 1 1 X X		MSDCN	＊ Comparison connection aborted Direct connection 2-pair comparison connection 3-pair comparison connection
X X X 0 X X X X X X X 1 X X X X		MSRACL	＊ Normal operation Read address reset
X X 0 X X X X X X X 1 X X X X X		MSRDEN	＊ Decoding aborted Decoding executed
X 0 X X X X X X X 1 X X X X X X		MSWACL	＊ Normal operation Write address reset
0 X X X X X X X 1 X X X X X X X		MSWREN	＊ Encoding aborted Encoding executed

(B) Expansion I/O port (I/O setting)

Table 7-1-6 (2)

Data (D7 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X 0 X X X X X X X 1	81	EXT0ST	Expansion I/O Port EXT0 I/O setting ＊ Input Output
X X X X X X 0 X X X X X X X 1 X		EXT1ST	Expansion I/O Port EXT1 I/O setting ＊ Input Output
X X X X X 0 X X X X X X X 1 X X		EXT2ST	Expansion I/O Port EXT2 I/O setting ＊ Input Output

(C) Expansion I/O port (Output data setting)

Table 7-1-6 (3)

Data (D7 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X 0 X X X X X X X 1	82	EXT0WT	Expansion I/O port EXT0 output setting ＊ L output H output
X X X X X X 0 X X X X X X X 1 X		EXT1WT	Expansion I/O port EXT1 output setting ＊ L output H output
X X X X X 0 X X X X X X X 1 X X		EXT2WT	Expansion I/O port EXT2 output setting ＊ L output H output

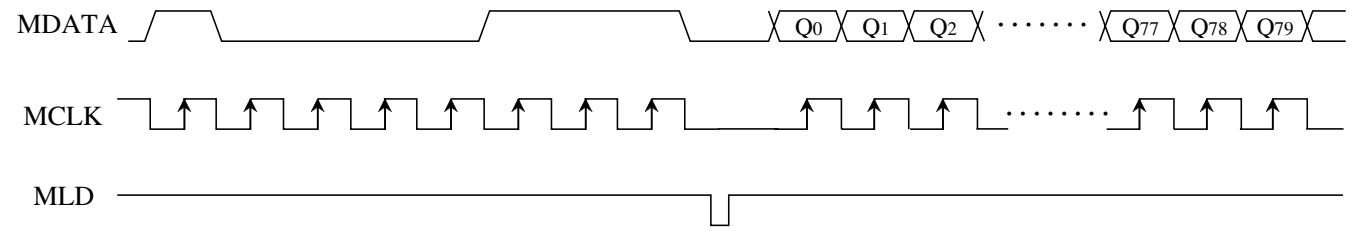
(D) Option setting

Table 7-1-6 (4)

Data (D7 to D0)	Command (HEX) (B7 to B0)	Symbol	Function (＊ : Setting at reset)
X X X X X X X 0 X X X X X X X 1	85	CMOD	＊ Decompression mode 4-bit compression mode
X X 0 X X X X X X X 1 X X X X X			＊ 16M DRAM not used 16M DRAM used (NCAS1 used as A10)
X 0 0 X X X X X X 1 0 X X X X X		RSEL1	＊ One DRAM used Two DRAMs used (NCAS of unused RAM is fixed at high level)
0 X 0 X X X X X 1 X 0 X X X X X		RSEL0	＊ 1M DRAM used 4M DRAM used
0 X X 1 X X 0 0 0 X X 1 X X 0 1 0 X X 1 X X 1 0 0 X X 1 X X 1 1	86	WSEL	＊ No window discrimination Window discrimination 98±4 CLDCK window Window discrimination 98±8 CLDCK window Window discrimination 98±28 CLDCK window
0 X X 1 X 0 X X 0 X X 1 X 1 X X		C2SEL	＊ Interpolated comparison Comparison without interpolation
0 X X 1 0 X X X 0 X X 1 1 X X X		CMPSEL	＊ 16-bit comparison Upper 12-bit comparison
0 X 0 1 X X X X 0 X 1 1 X X X X			Parameter reset at start of encoding during direct connection ＊ No Yes

Note) The D4 bit of the 86h command is by default set to 0. Set this bit to 1 while the memory system is running, otherwise playback data will involve noise.

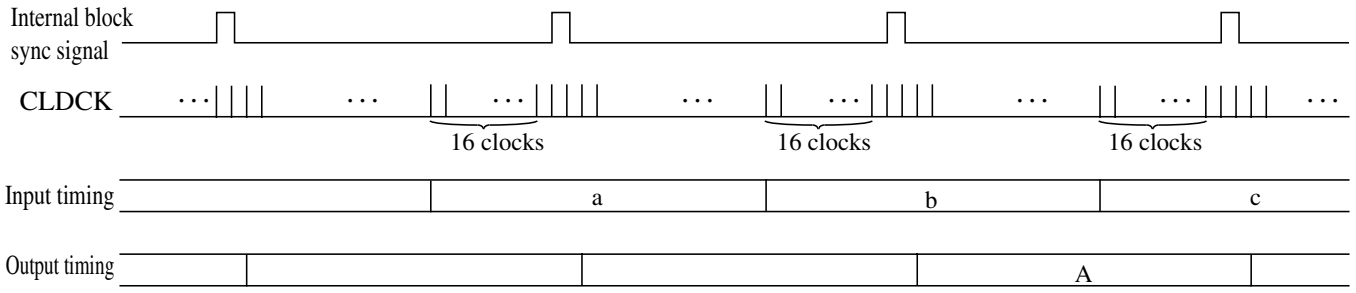
(E) Q code input for optical digital output signal (TX)



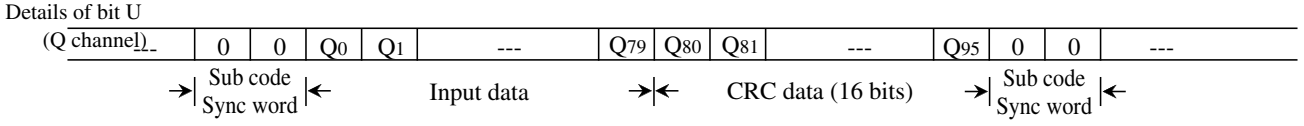
If the anti-shock memory controller is turned on, Q code data can be set for user data on the optical digital output signal.

Table 7-1-6 (5)

Command (HEX) (B7 to B0)	Data	Symbol	Function
87	Q_0 to Q_{79} (80 bits)	MCQ	Q code input for TX

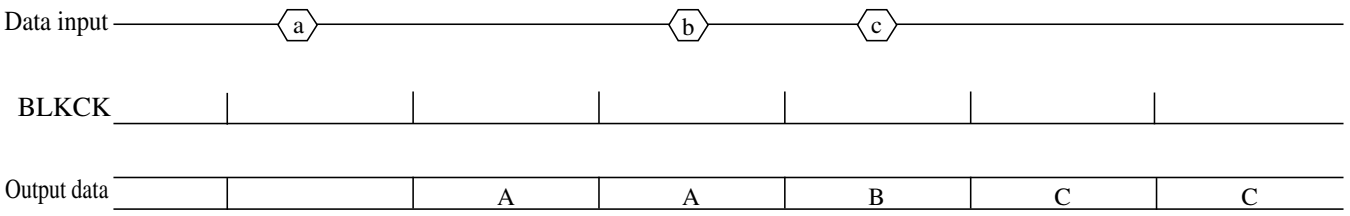


The Q code that is input into a-zone is output as bit U data during period A.



CRC data is generated from the arithmetic operation of input data and added.

Note1) The internal block sync signal is a synchronized with a subcode sync word.



If no Q code is input, the previous value will be kept on hold and bit U will be output. At that time, CRC data is added with disabling data.

Note2) ・Interruption is not allowed while the Q code is input, otherwise the wrong bit U will be output.
・The Q code cannot be input into a single block more than once, otherwise the wrong bit U will be output.

[2] Data read

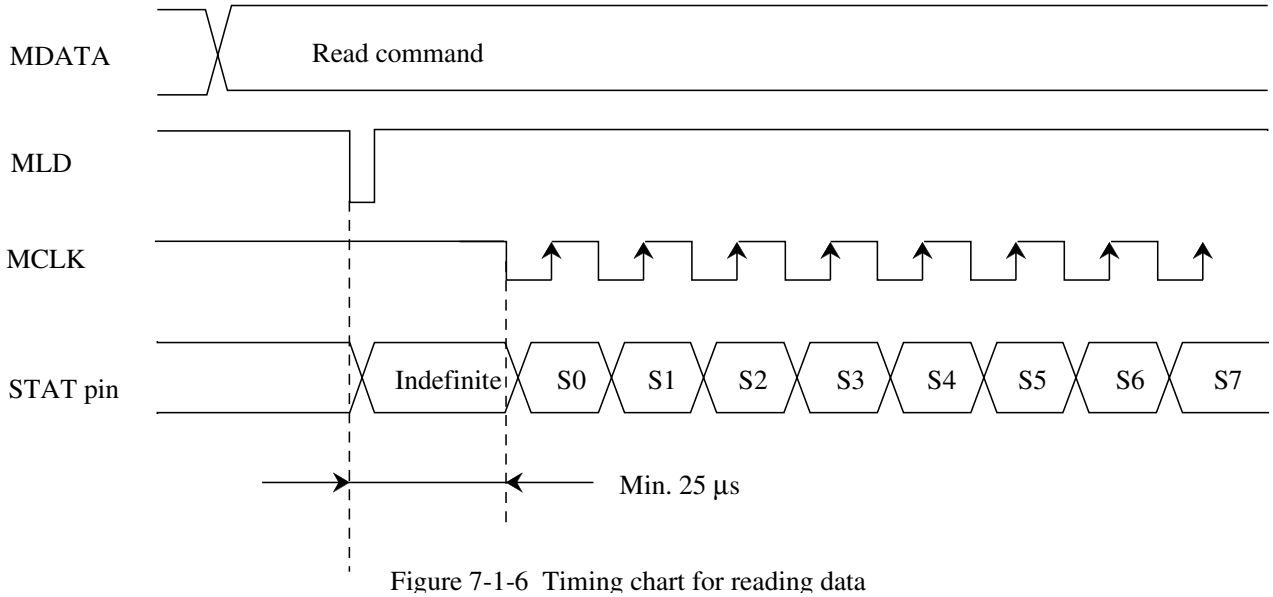


Figure 7-1-6 Timing chart for reading data

(A) Status command

Table 7-1-6 (6)

Command (HEX) (B7 to B0)	Output bit	Symbol	Function
90	S0	FLAG6	L: FLAG6I input normal H: FLAG6I input abnormal
	S1	MSOVF	L: Normal H: Write overflow
	S4	DCOMP	L: Normal H: During comparison connection
91	S0	MSEMP	L: Normal H: No enabled data
	S1	OVFL	L: Normal H: Write overflow

(B) Remaining enabled data

Table 7-1-6 (7)

Command (HEX) (B7 to B0)	Output bit	Function
92	S0	H: 8M bits
	S1	H: 4M bits
	S2	H: 2M bits
	S3	H: 1M bits
	S4	H: 512K bits
	S5	H: 256K bits
	S6	H: 128K bits
	S7	H: 64K bits
	S8	H: 32K bits
	S9	H: 16K bits
	S10	H: 8K bits
	S11	H: 4K bits
	S12	H: 2K bits
	S13	H: 1K bits
	S14	H: 512 bits
	S15	H: 256 bits

(C) Expansion I/O port

Table 7-1-6 (8)

Command (HEX) (B7 to B0)	Output bit	Symbol	Function
93	S5	EXT2RD	Expansion I/O port EXT2 input data
	S6	EXT1RD	Expansion I/O port EXT1 input data
	S7	EXT0RD	Expansion I/O port EXT0 input data

7-1 (7) Automatic adjustment

Following is a list of automatic adjustment.

Table 7-1-7

	Command (HEX) (B7 to B0)	Description	Time required	Traverse operation
Offset AOC1 (Note)	F9	Averages and corrects the focus error values and tracking error values as offset when the laser is turned on or off.	50 ms to 140 ms	FWD/REV enabled
Fo balance ABC1	F7	Inputs the disturbance into the focus servo loop, and makes corrections so that the envelope ripple for the 3T component of the RF signal in the positive and negative parts of the FE signal should be balanced. The output pin for corrections is FBAL.	Within 0.5 s	STOP
Tr balance ABC2	FB	The average tracking error value without the tracking servo is used as a balancing value to make corrections. The output pin for corrections is TBAL.	Within 1 s	STOP
Fo rough gain AGC1	FC	Focus search is performed at approx. 5.4 Hz or 1.3 Hz, and the disturbance input amount for the fine AGC is determined using focus error S-curve p-p value. The gain will be unchanged.	Set between 190 ms and 780 ms	FWD/REV enabled
Tr rough gain AGC2	FD	The p-p value of the tracking error without the tracking servo determines the disturbance input amount for the fine AGC. The gain will be unchanged.	Set between 135 ms and 350 ms	STOP
Fo fine gain FAGC	FE	Inputs the disturbance into the focus servo loop, and adjusts the gain crossover to the frequency set by the microcomputer command.	Within 0.5 s	STOP
Tr fine gain TAGC	FF	Inputs the disturbance into the tracking servo loop, and adjusts the gain crossover to the frequency set by the microcomputer command.	Within 0.5 s	STOP

Note) Do not use FAh, a conventional AOC2 command.

7-2 Input timing

7-2 (1) Subcode interface

A. SUBQ data read

Subcode data can be read at the timing shown in the figure below.

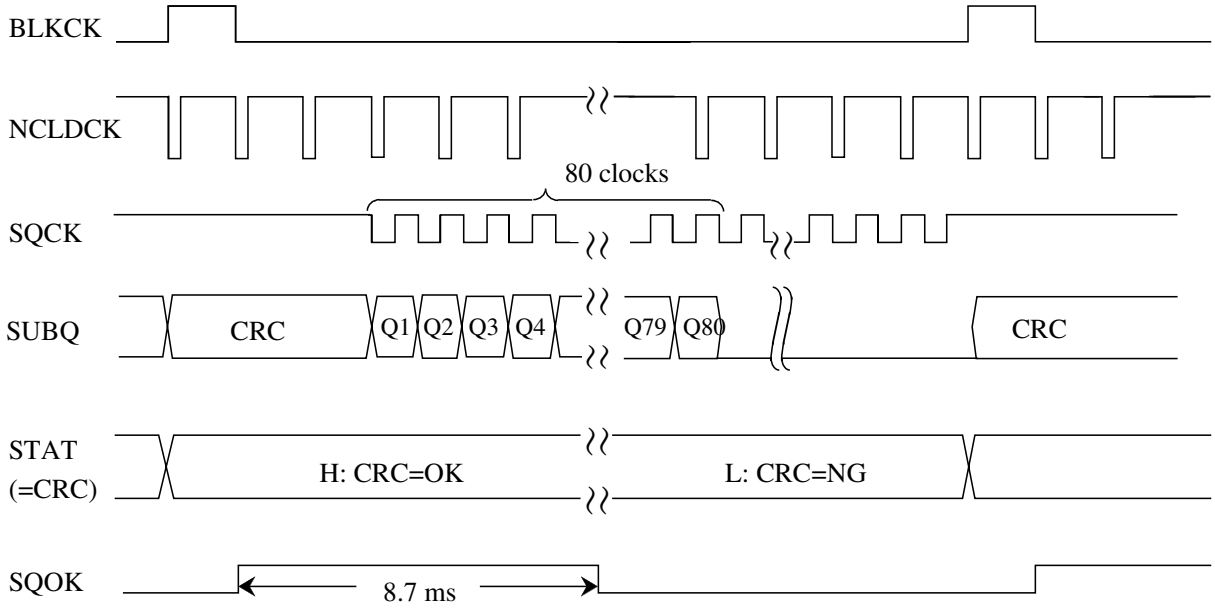
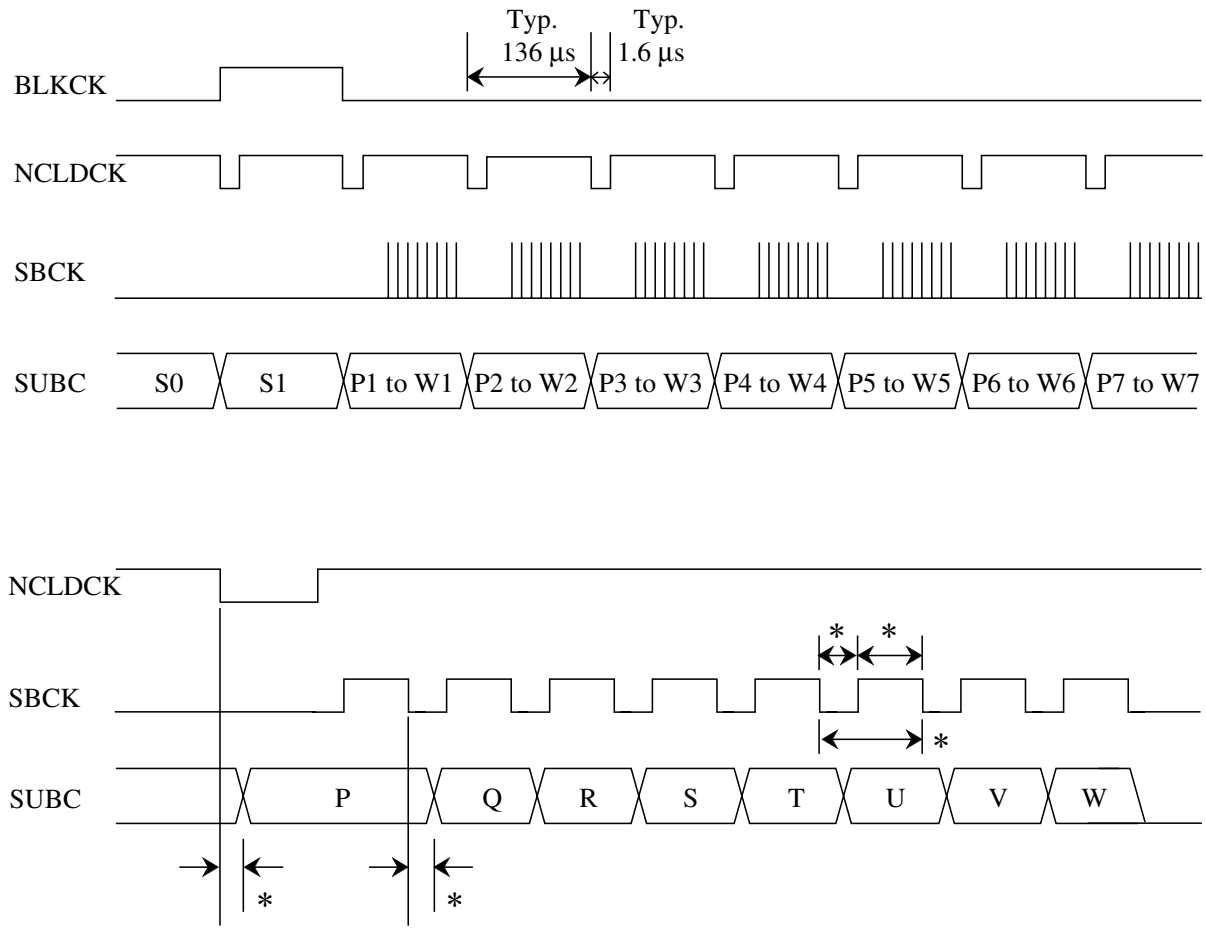


Figure 7-2-1 BLKCK, NCLDCK, SQCK, SUBQ, and CRC timing chart

B. Subcode data read

By inputting a clock from SBCK pin, subcode data, P to W, can be read from SUBC pin. The timing is shown in the figure below.
Since subcode data varies every falling edge of NCLDCK, input 8 clocks of SBCK every falling edge of NCLDCK, and switch the content of SUBC output to P to W.
Then SUBC output which varies in synchronization with the falling edge of SBCK is received at the timing of the rising edge of SBCK. All subcode data can be read by repeating the operation above for each NCLDCK.
By inputting SBCK, the content of FLAG output will vary. So measuring the error rate while reading subcode is not possible. Take it into consideration when designing the system.



*: Refer to the values specified in the PRODUCT STANDARDS.

Figure 7-2-2 NCLDCK, SUBC, and SBCK timing chart

7-2 (2) Serial data output

A. Serial data output mode 1

By executing the following command, the BCLK signal, LRCK signal, and SRDATA signal will be output from pins 65, 66, and 67 respectively.

Table 7-3-1

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol
X X X X X 1 X X X X X X X X 0	4E	MPEGIF, IOSTOP

Note) X can be any value.

B. Serial data output mode 2

By executing the following command, the SRDATA signal, LRCK signal, and BCLK signal will be output from pins 73, 74, and 75 respectively.

Table 7-3-2 (1)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol
X X X X X X X X X X X X X X 1 X	4C	SROUT2

Note) X can be any value.

Table 7-3-2 (2)

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol
X X X X X X X X X X X X X X X 0	4E	IOSTOP

Note) X can be any value.

C. Serial data output selection

The following command determines whether serial data in serial data output mode 1 or serial data output mode 2 is output with or without attenuation and de-emphasis.

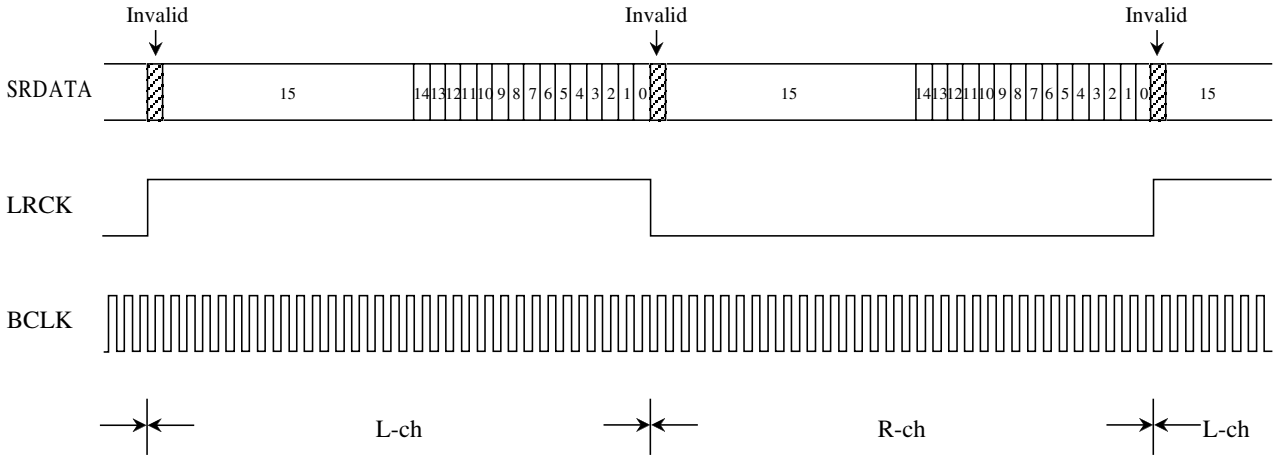
Table 7-3-3

Data (D15 to D0)	Command (HEX) (B7 to B0)	Symbol	Function
X X X X X X X X X X 0 X X X X X	41	DSPSEL	With no attenuation or de-emphasis
X X X X X X X X X X 1 X X X X X			With attenuation and de-emphasis

Note) X can be any value.

D. Serial data output timing

The following timing chart shows the output timing of serial data. Serial data output mode 1 and 2 are the same in the output timing of serial data.



7-2 (3) Serial data input

When the IC is in serial data output mode 1 or 2, the SRDATA signal, LRCK signal, and BCLK signal will be input into pins 57, 58, and 59 respectively so that IOSTOP bit will be set to 0. Therefore, handle pins 57, 58, and 59 as input pins in serial data output mode 1 or 2.
The input timing of serial data is the same as the output timing of serial data.

PRODUCT STANDARDS

A. ABSOLUTE MAXIMUM RATINGS

T_a=25°C

Parameter		Symbol	Rating	Unit	Note
A1	Supply voltage	$DV_{DD1,2}$ $AV_{DD1,2}$	−0.3 to +4.6	V	$DV_{SS1,2}$=0 V $AV_{SS1,2}$=0 V
A2	Input voltage	V_I	$DV_{SS1,2}$−0.3 to $DV_{DD1,2}$+0.3 $AV_{SS1,2}$−0.3 to $AV_{DD1,2}$+0.3	V	$DV_{SS1,2}$=0 V $AV_{SS1,2}$=0 V
A3	Output voltage	V_O	$DV_{SS1,2}$−0.3 to $DV_{DD1,2}$+0.3 $AV_{SS1,2}$−0.3 to $AV_{DD1,2}$+0.3	V	$DV_{SS1,2}$=0 V $AV_{SS1,2}$=0 V
A4	Power dissipation	P_D	570	mW	$DV_{SS1,2}$=0 V $AV_{SS1,2}$=0 V
A5	Operating ambient temperature	T_{opr}	−40 to +85	°C	
A6	Storage temperature	T_{stg}	−55 to +125		

Note 1) The absolute maximum ratings are the limit values beyond which the IC may be broken. They do not assure operations.

Note 2) Each of DV_{SS1}, DV_{SS2}, AV_{SS1}, and AV_{SS2} pins should be directly connected to the ground and used at the same voltage.

Note 3) Each of DV_{DD1}, DV_{DD2}, AV_{DD1}, and AV_{DD2} pins should be directly connected to the specified power supply and used at the same voltage.

Note 4) DV_{DD1}, DV_{DD2}, AV_{DD1}, and AV_{DD2} should be powered up at the same time.

Note 5) The operation of the audio D/A converter is not guaranteed for operations in 2x-speed playback modes (i.e., when anti-shock memory controller is not operating).

Note 6) Connect a bypass capacitor (0.1 µF or more) between DV_{DD1} and DV_{SS1} pins, between DV_{DD2} and DV_{SS2} pins, between AV_{DD1} and AV_{SS1} pins, and between AV_{DD2} and AV_{SS2} pins.

B. OPERATING CONDITIONS

T_a = −40°C to +85°C
$DV_{SS1,2}$ = 0 V
$AV_{SS1,2}$ = 0 V

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
B1	Digital system supply voltage	$DV_{DD1,2}$		3.0	3.3	3.6	V
B2	Audio system supply voltage	AV_{DD1}	(Note 7)	3.0	3.3	3.6	V
B3	Analog system supply voltage	AV_{DD2}	(Note 7)	3.0	3.3	3.6	V
B4	D-RAM interface voltage	DV_{DD3V}		$V_{DD1,2}$		3.6	V

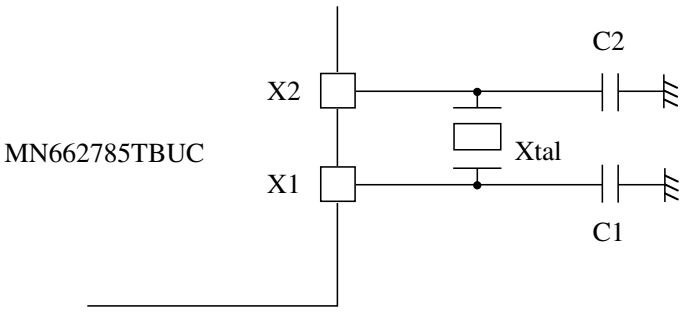
Note 7) It is recommended to basically use AV_{DD1} and AV_{DD2} at the same voltage as DV_{DD}.

$DV_{DD1,2}$ = 3.3 V, $DV_{SS1,2}$ = 0 V
$AV_{DD1,2}$ = 3.3 V, $AV_{SS1,2}$ = 0 V
T_a = −40°C to +85°C

Self-excited Oscillation (Note 8)

B5	Crystal frequency	f_{xtal}	With no external resistor R		33.8688		MHz
B6	External capacitance 1	C1			10		pF
B7	External capacitance 2	C2			10		pF

Note 8) Oscillator Circuit



C. ELECTRICAL CHARACTERISTICS

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

(1) DC Characteristics

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
C1	Supply current	I_{DD}	Anti-shock memory controller is not operating. No external load (in normal-speed playback mode) T_a=25°C		23	46	mA
C2	Total power consumption	P_T			76	152	mW
C3	Supply current	I_{DD}	Anti-shock memory controller is not operating. No external load (in 2x-speed playback mode) T_a=25°C		24	48	mA
C4	Total power consumption	P_T			80	160	mW

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Input Pins (1) ＊1							
C5	Input voltage high level	V_{IH1}		2.64		$DV_{DD1,2}$	V
C6	Input voltage low level	V_{IL1}		$DV_{SS1,2}$		0.66	V
C7	Input leakage current	I_{LK1}	V_{IN}=0 V to 3.3 V			±1	μA

＊1 FSEL, CSEL
TMOD1, TMOD2
EXT0/ISRDATA/SRMON2, EXT1/ILRCK/VDET/PCK, EXT2/IBCLK/EFM
D0, D1, D2, D3, OFT, NRFDET, BDO, NTEST, MCLK, MDATA, MLD,
SQCK/BCLK1/TXTCLK1, DMUTE/SRDATA1, NRST, SBCK/TXTCLK2/LRCK2

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Output Pins (1) ＊2							
C8	Output voltage high level	V_{OH1}	I_{OH1}=−1 mA	$DV_{DD1,2}$ −0.6			V
C9	Output voltage low level	V_{OL1}	I_{OL1}=1 mA			0.4	V
Output Pins (2) ＊3							
C10	Output voltage high level	V_{OH2}	I_{OH2}=−1 mA	$DV_{DD1,2}$ −0.6			V
C11	Output voltage low level	V_{OL2}	I_{OL2}=1 mA			0.4	V
C12	Output leakage current	I_{LK2}	Hi-Z V_O=0 V to 3.3 V			±1	µA

＊2 LDON, FLAG/SRMON1, CLVS/IPFLAG, EXT0/ISRDATA/SRMON2, EXT1/ILRCK/VDET/PCK, EXT2/IBCLK/EFM, TX, BLKCK/DQSY1, SQCK/BCLK1/TXTCLK1, SUBQ/LRCK1/TXTDAT1, DMUTE/SRDATA1, STAT, SPPOL, PMCK, SMCK, SUBC/TXTDAT2/SRDATA2, SBCK/TXTCLK2/LRCK2, NCLDCK/DQSY2/BCLK2, D0, D1, NWE, NRAS, D2, D3, NCAS0, NCAS1, A8, A7, A6, A5, A4, A9, A0, A1, A2, A3

＊2 SPOUT, TRVP, TRVM, TRP, TRM, FOP, FOM,

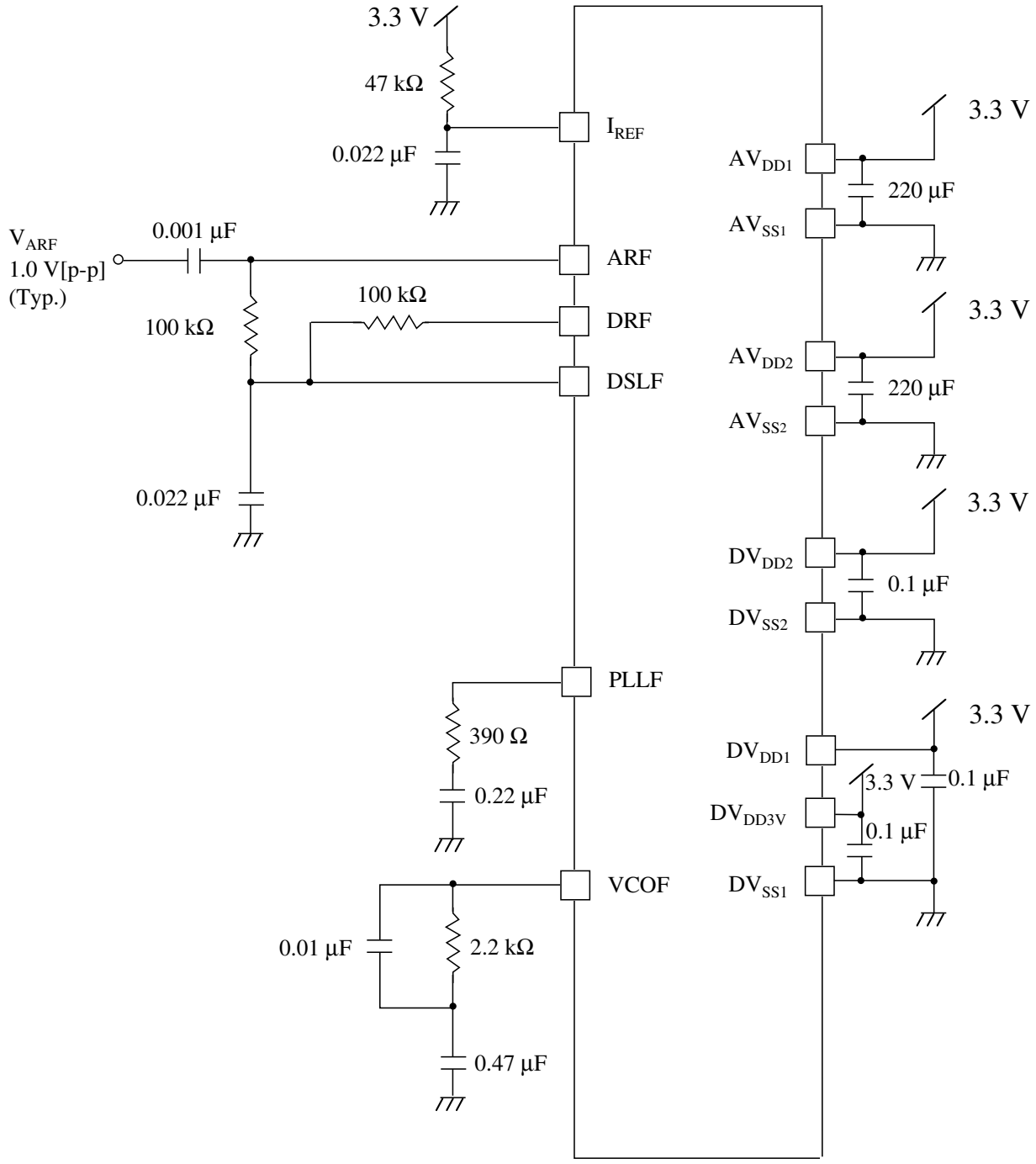
$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	Analog System Input Pin (1)	I_{REF}					
C13	Input current	I_{REF}	When pulled up by a 47-kΩ resistor	25	47	80	µA
	Analog System Input Pin (2)	ARF					
C14	Input signal amplitude	V_{ARF}	Input level of the EFM signal in the application circuit of the DSL circuit block	0.5	1.0		V[p-p]
C15	Input leakage current	I_{LKA}				±1.0	µA
	Analog System Input Pin (3)	DRF					
C16	Input leakage current	I_{LKD}				±1.0	µA
C17	Internal resistance between ARF and DRF	R_{DRF}	ARF=1.65 V			10	kΩ

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Analog System Output Pin (1) DSLF (I_{REF} pin is pulled up to AV_{DD2} by a 47-kΩ resistor.)							
C18	Output current (N)	I_{DSH}	BDO=L, Tracking ON-state DSLF=1.65 V, ARF=3.3 V	98	130	169	µA
C19	Output current (P)	I_{DSL}	BDO=L, Tracking ON-state DSLF=1.65 V, ARF=0 V	−169	−130	−98	µA
C20	Output current balance in normal current mode	I_{DSBL}	BDO=L, Tracking ON-state Normal current mode	−8.0	−2.0	+4.0	µA
Analog System Output Pin (2) PLLF (I_{REF} pin is pulled up to AV_{DD2} by a 47-kΩ resistor.)							
C21	Phase comparison output current (N)	I_{PFH}	BDO=L, Tracking OFF-state	105	140	182	µA
C22	Phase comparison output current (P)	I_{PFL}	BDO=L, Tracking OFF-state	−182	−140	−105	µA
C23	Input leakage current	I_{LKP}	Hi-Z			±1	µA
C24	Output current balance in normal current mode	I_{PLBL}	BDO=L, Tracking ON-state Normal current mode	−15.0	−6.0	+3.0	µA
C25	PCK oscillator frequency	f_{VCO1}	Normal- to 2x-speed jitter-free mode VCO frequency (for PCK) switching =×0.5	4.32		8.65	MHz
Analog System Output Pin (3) VCOF (I_{REF} pin is pulled up to AV_{DD2} by a 47-kΩ resistor.)							
C26	Phase comparison output current (N)	I_{VFH}		98	130	169	µA
C27	Phase comparison output current (P)	I_{VFL}		−169	−130	−98	µA
C28	Input leakage current	I_{LKV}	Hi-Z			±1	µA
C29	VCO oscillator frequency	f_{VCO4}	Variable pitch jitter-free mode VCO frequency (for variable pitch jitter-free) switching=×0.5	8.46		16.94	MHz
Analog System Output Pins (4) TBAL, FBAL (I_{REF} pin is pulled up to AV_{DD2} by a 47-kΩ resistor.)							
C30	Output current (N)	I_{BAH}	At default setting (×1)	23	32	41	µA
C31	Output current (P)	I_{BAL}	At default setting (×1)	−41	−32	−23	µA

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz



DSL／PLL Block Recommended Circuit Diagram

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	Analog System Input Pins (4) TE, FE, RFENV						
C32	Input voltage high level	V_{IH4}				$0.9AV_{DD2}$	V
C33	Input voltage low level	V_{IL4}		$0.1AV_{DD2}$			V

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
A/D Converter (for Servo)							
C34	Resolution	RES				8	bit
C35	Integral nonlinearity	INL	A/D output=99 to 66 (2's complement)			±2	LSB
C36	Differential nonlinearity	DNL				±3	LSB

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D/A Converter Analog Characteristics (Note 9), (Note 12)							
C37	Signal-to-noise ratio	S/N	EIAJ	90	97		dB
C38	Dynamic range	D.R.	EIAJ	86	94		dB
C39	Total harmonic distortion	THD+N	EIAJ		0.005	0.009	%
C40	Crosstalk		EIAJ	80	89		dB
C41	Output level 1		Reference input signal of 1 kHz Full scale (Note 10)	1.04	1.33	1.62	V_{rms}
C42	Output level difference		Difference of OUTL and OUTR pins at output level 1. 20 log (V_R/V_L)	−0.99		+0.99	dB
C43	Output level 2		Reference input signal of 1 kHz Full scale (Note 11)	0.69	0.88	1.07	V_{rms}

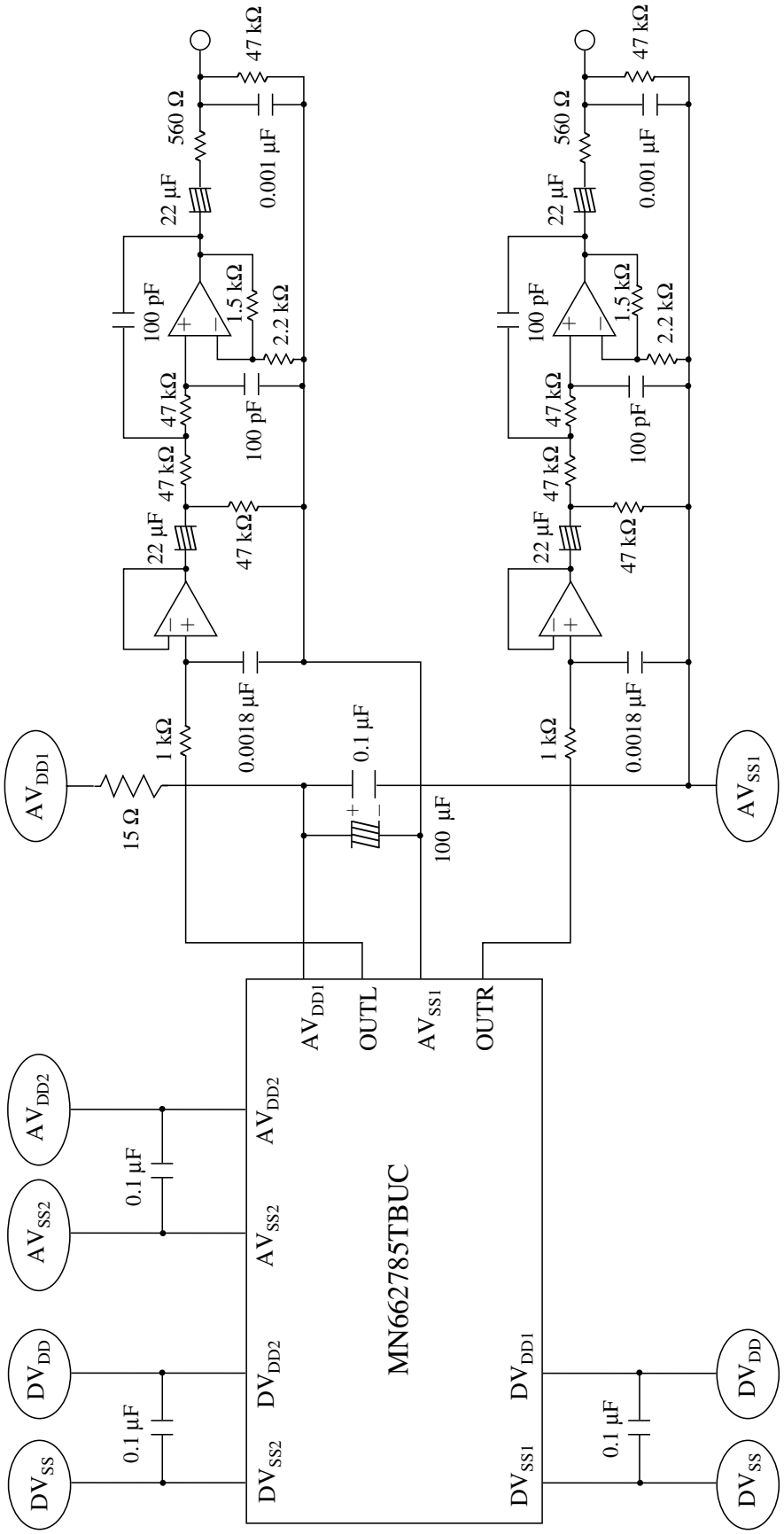
Note 9) The analog characteristics indicate the values measured by inserting a 15-Ω resistor between the AV_{DD1} pin and power supply. The typical values are only reference values. They are not guaranteed.

Note 10) The output level 1 shows the measured value at the output pins of the application circuit.

Note 11) Output level 2 is calculated by taking the measured value of output level 1, dividing it by the external circuit gain of the application circuit, and converting the result to the value at the output pin of this IC.

Note 12) The D/A converter always operates in the normal-speed playback mode.

[D/A Converter Application Circuit]

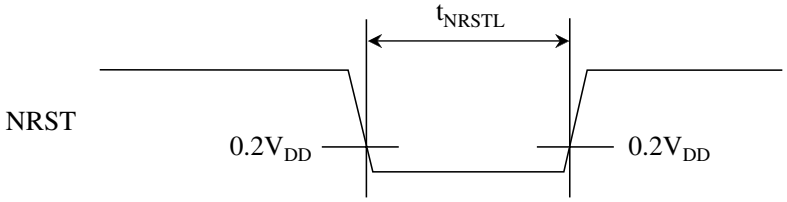


(2) AC characteristics

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

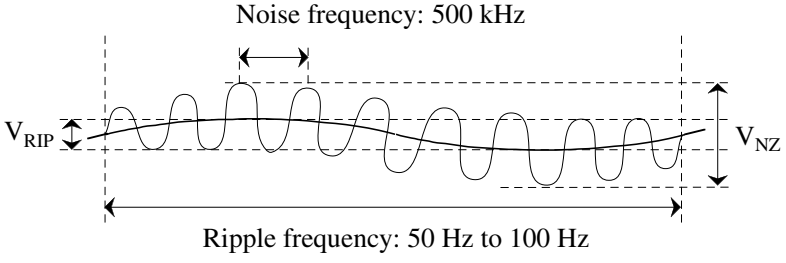
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
	Reset Timing (Note 13)						
C44	NRST pulse width	t_{NRSTL}		200			ms
	Power Supply Ripple Noise (Note 14)						
C45	Ripple amplitude	V_{RIP}				15	mV[p-p]
C46	Ripple noise amplitude	V_{NZ}				50	mV[p-p]

Note 13) When the power is turned on, reset with the NRST pulse which is equal to or exceeds the above pulse width only after the clock oscillation is stabilized within ±10% of error of the specified oscillator frequency.
When designing, be careful to eliminate noise from the reset line as much as possible.



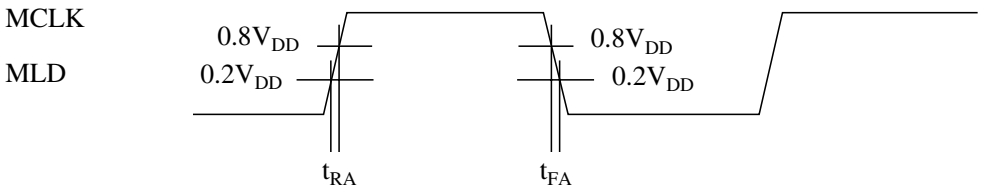
Note 14) The permissible ripple and noise of power supply to this IC are guaranteed on condition that the ripple frequency range is between 50 Hz and 100 Hz, the noise frequency is at 500 kHz, and that both ripple and noise are sine wave signals as shown below.

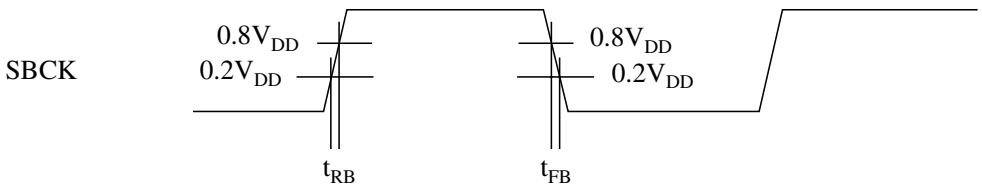
Pay utmost attention to these ripple signal and noise signal because they may exceed the permissible values under the influence of the location of peripheral parts.



$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

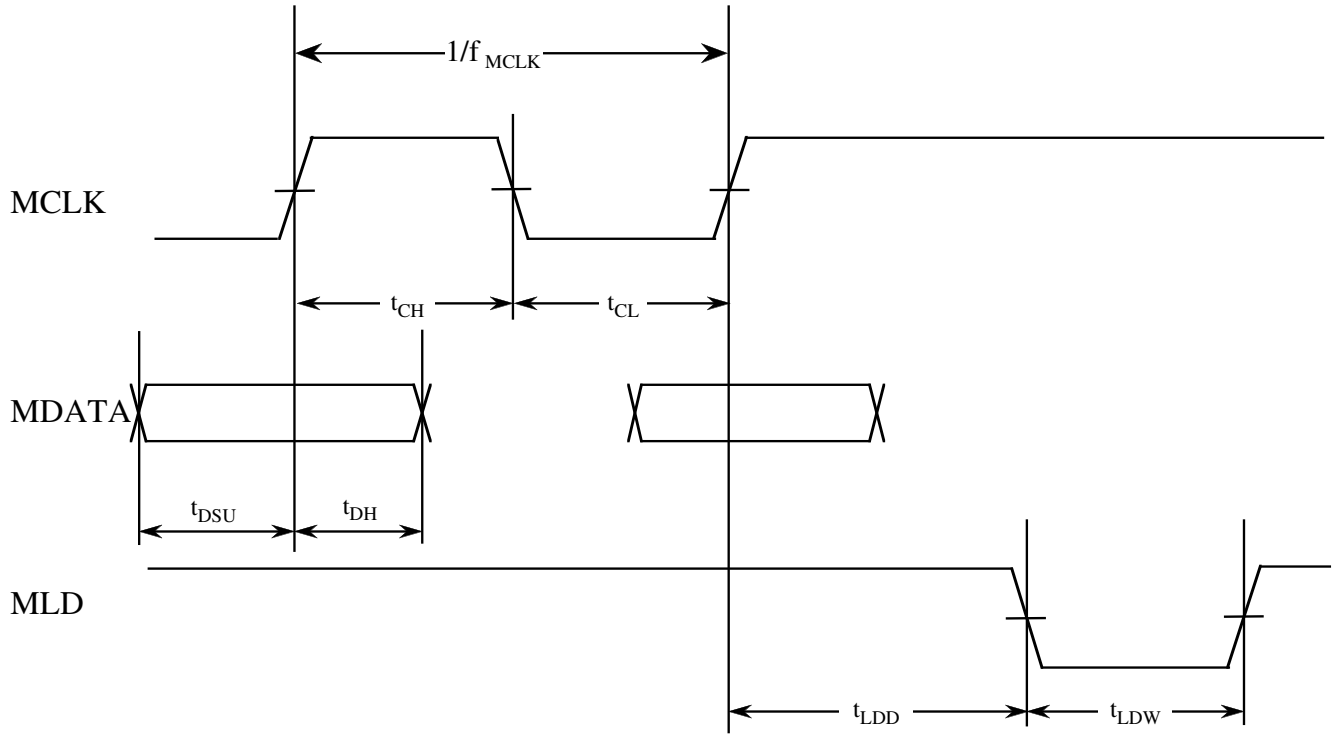
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
C47	Rise time	t_{RA}				100	ns
C48	Fall time	t_{FA}				100	ns
C49	Rise time	t_{RB}				50	ns
C50	Fall time	t_{FB}				50	ns





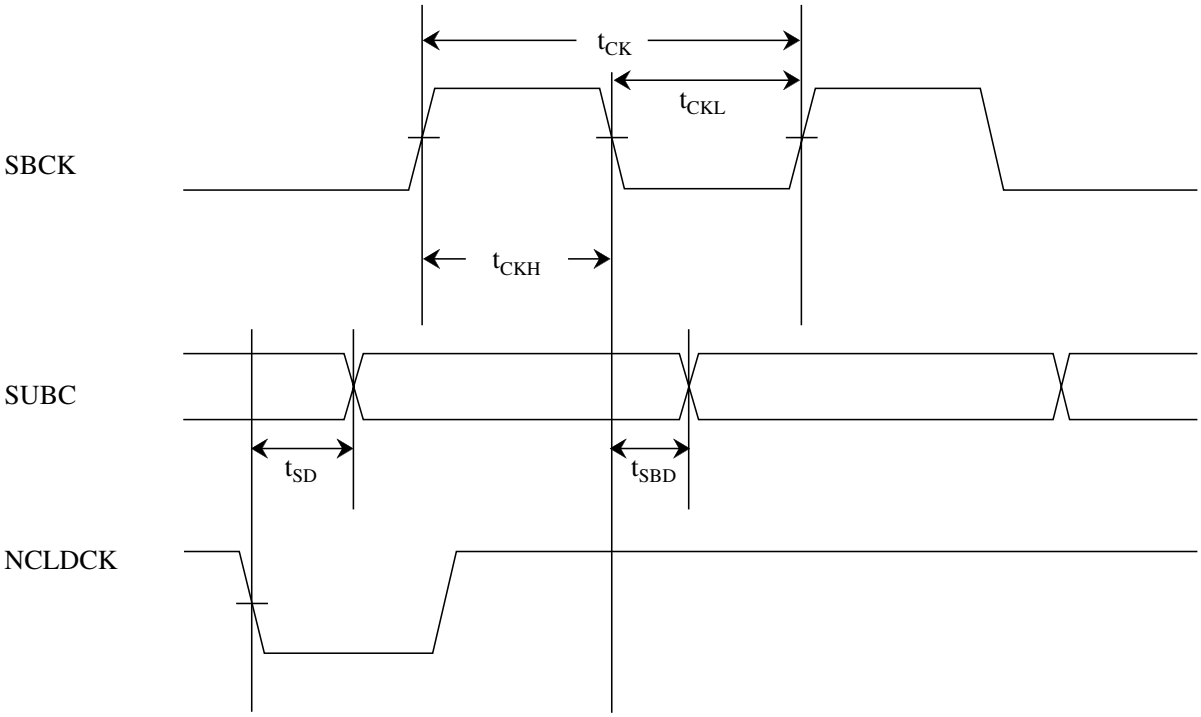
$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

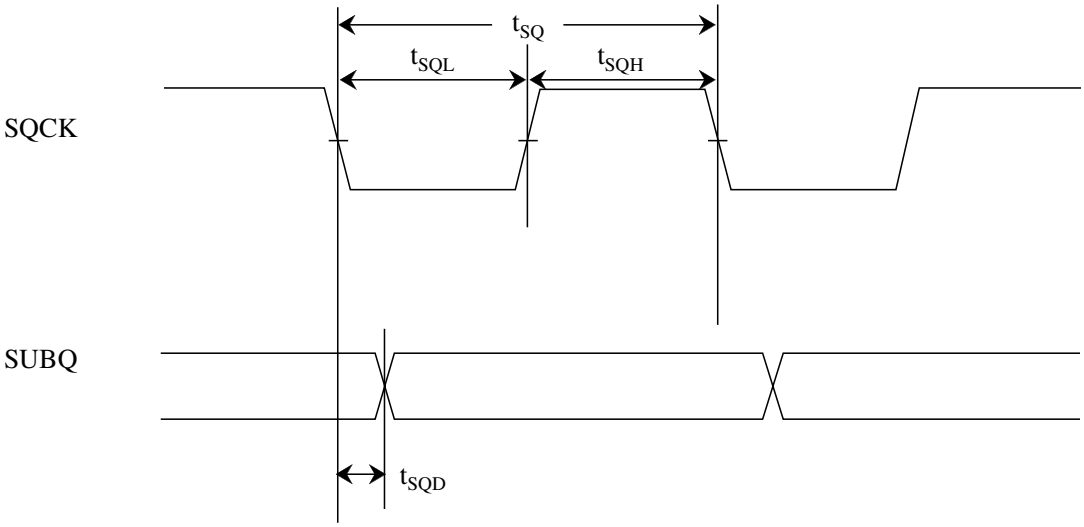
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Microcomputer Instruction Input Timing							
C51	Clock frequency	f_{MCLK}				1.1	MHz
C52	Clock pulse width	$t_{CH,CL}$		300			ns
C53	Data setup time	t_{DSU}		300			ns
C54	Data hold time	t_{DH}		300			ns
C55	Delay time	t_{LDD}		300			ns
C56	Latch pulse width	t_{LDW}		0.5		5	µs



$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

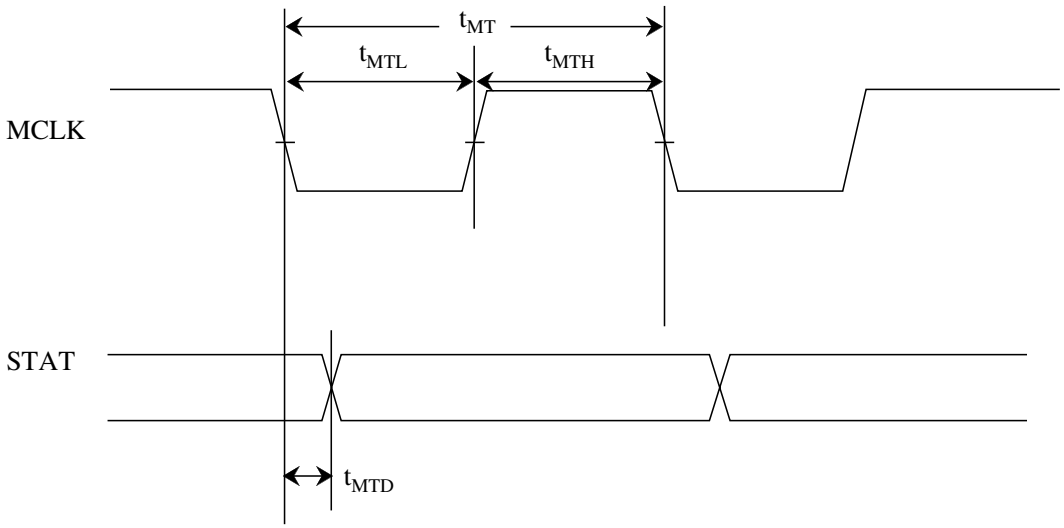
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Subcode Interface (1) (FSEL=L)							
C57	Clock width	t_{CK}, t_{SQ}		700			ns
C58	High-level pulse width	t_{CKH}, t_{SQH}		300			ns
C59	Low-level pulse width	t_{CKL}, t_{SQL}		300			ns
C60	Delay time	t_{SBD}, t_{SQD}				250	ns
C61	Setup delay time	t_{SD}				150	ns
Subcode Interface (2) (FSEL=H)							
C62	Clock width	t_{CK}, t_{SQ}		500			ns
C63	High-level pulse width	t_{CKH}, t_{SQH}		200			ns
C64	Low-level pulse width	t_{CKL}, t_{SQL}		200			ns
C65	Delay time	t_{SBD}, t_{SQD}				150	ns
C66	Setup delay time	t_{SD}				150	ns


t_{CK}
t_{CKL}
SBCK
t_{CKH}
SUBC
t_{SD}
t_{SBD}
NCLDCK


t_{SQ}
t_{SQL}
t_{SQH}
SQCK
SUBQ
t_{SQD}

$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

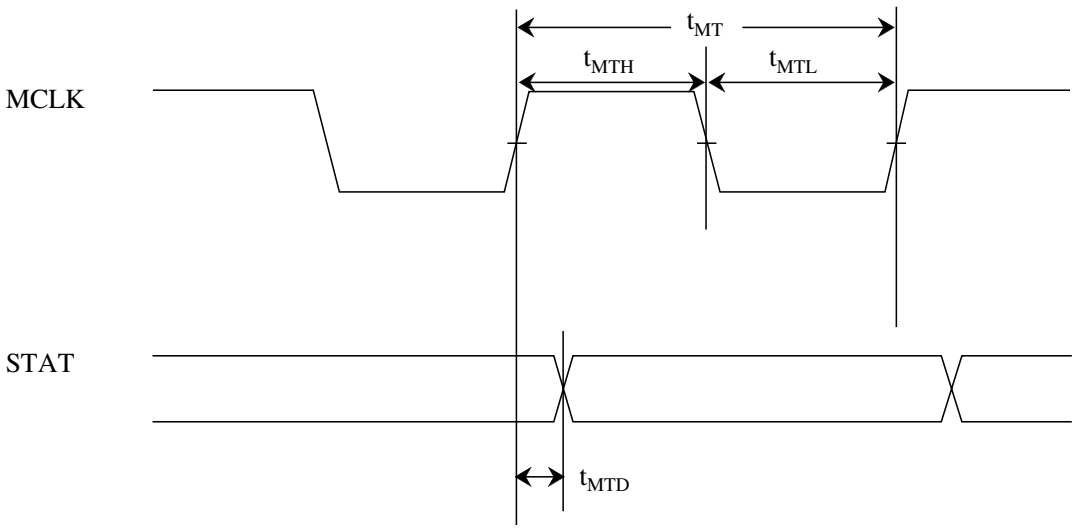
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
STAT output Interface (1) (FSEL=L)							
C67	Clock width	t_{MT}		909			ns
C68	High-level pulse width	t_{MTH}		300			ns
C69	Low-level pulse width	t_{MTL}		300			ns
C70	Delay time	t_{MTD}				250	ns
STAT output Interface (2) (FSEL=H)							
C71	Clock width	t_{MT}		909			ns
C72	High-level pulse width	t_{MTH}		300			ns
C73	Low-level pulse width	t_{MTL}		300			ns
C74	Delay time	t_{MTD}				150	ns



$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

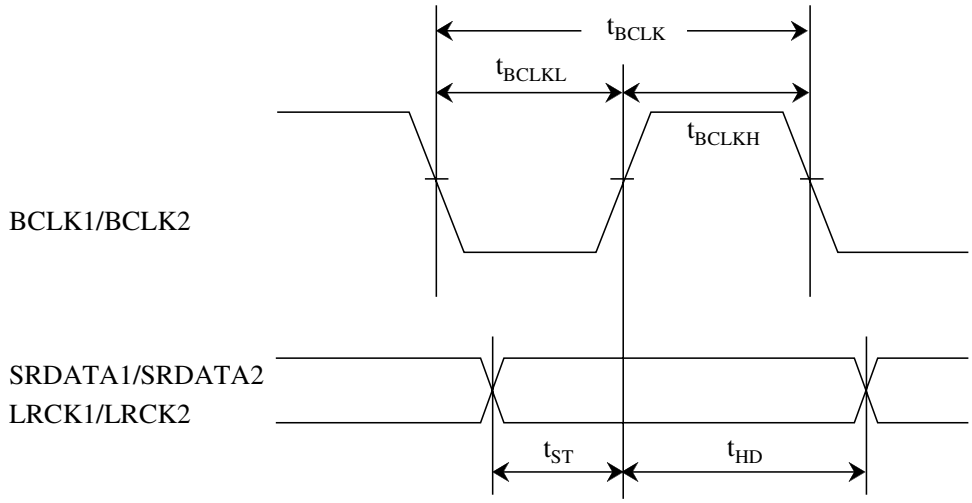
Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
STAT output Interface (3) (FSEL=L) (Note 15)							
C75	Clock width	t_{MT}		909			ns
C76	High-level pulse width	t_{MTH}		300			ns
C77	Low-level pulse width	t_{MTL}		300			ns
C78	Delay time	t_{MTD}				250	ns
STAT output Interface (4) (FSEL=H) (Note 15)							
C79	Clock width	t_{MT}		909			ns
C80	High-level pulse width	t_{MTH}		300			ns
C81	Low-level pulse width	t_{MTL}		300			ns
C82	Delay time	t_{MTD}				150	ns

Note 15) STAT output data switching with MCLK when using 75h command



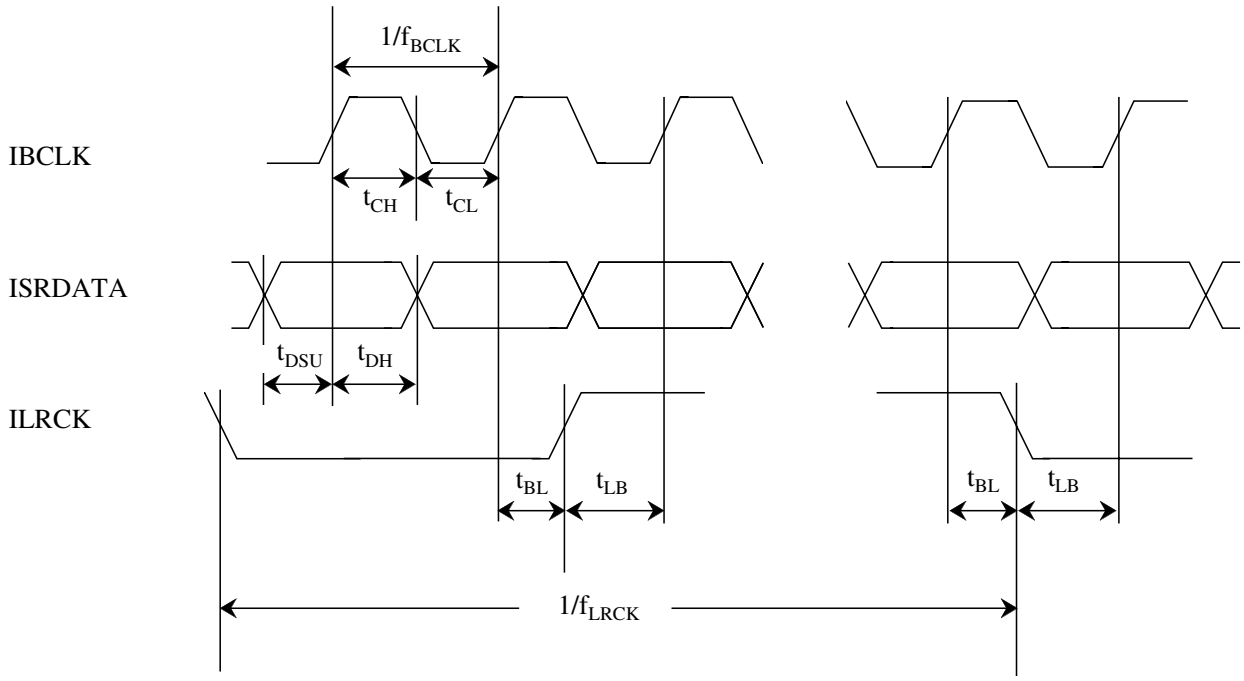
V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D/A output Interface (1)							
C83	Clock width	t_{BCLK}	Normal-speed playback mode		354		ns
C84	High-level pulse width	t_{BCLKH}			177		ns
C85	Low-level pulse width	t_{BCLKL}			177		ns
C86	Setup time	t_{ST}		70			ns
C87	Hold time	t_{HD}		70			ns
D/A output Interface (2)							
C88	Clock width	t_{BCLK}	2x-speed playback mode		177		ns
C89	High-level pulse width	t_{BCLKH}			88.5		ns
C90	Low-level pulse width	t_{BCLKL}			88.5		ns
C91	Setup time	t_{ST}		50			ns
C92	Hold time	t_{HD}		50			ns



V_{DD}=3.3 V, V_{SS}=0 V
AV_{DD}=3.3 V, AV_{SS}=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

Parameter		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
D/A converter input timing							
C93	BCLK frequency	f_{BCLK}				4	MHz
C94	BCLK pulse width	t_{CH}, t_{CL}		100			ns
C95	Data setup time	t_{DSU}		65			ns
C96	Data hold time	t_{DH}		65			ns
C97	LRCK frequency	f_{LRCK}			44.1		kHz
C98	BCLK-LRCK timing	t_{BL}, t_{LB}		65			ns



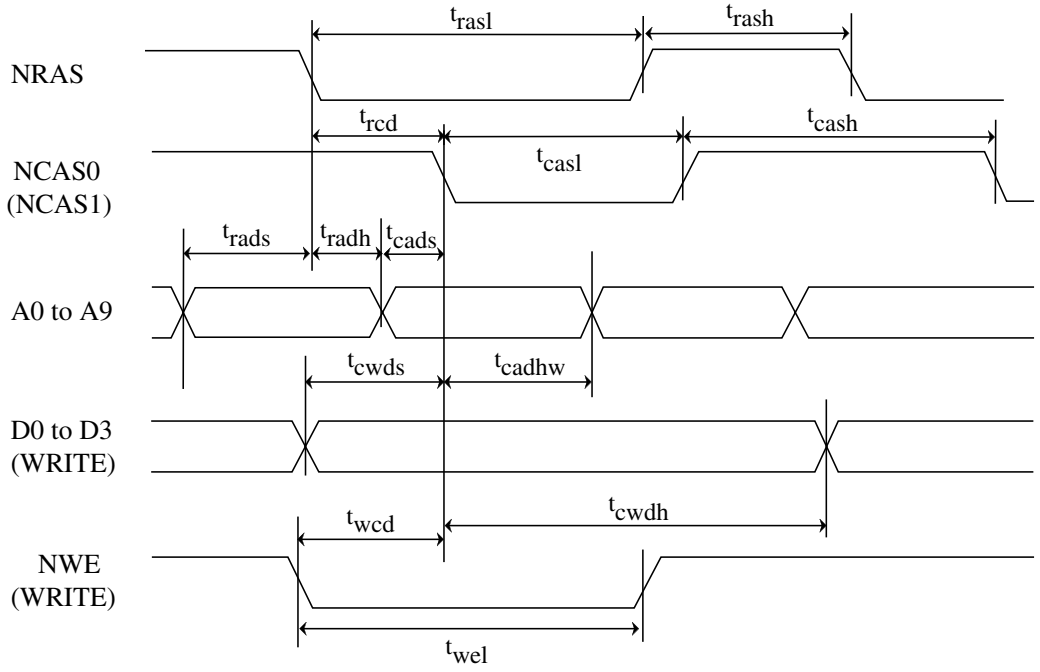
$DV_{DD1,2}$=3.3 V, $DV_{SS1,2}$=0 V
$AV_{DD1,2}$=3.3 V, $AV_{SS1,2}$=0 V
T_a=−40°C to +85°C
f_{X1}=33.8688 MHz

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
DRAM Interface							
C99	NRAS low-level pulse width	t_{rasl}			6		tcy
C100	NRAS high-level pulse width	t_{rash}		2			tcy
C101	NCAS0 / NCAS1 low-level pulse width	t_{casl}			4		tcy
C102	NCAS0 / NCAS1 high-level pulse width	t_{cash}		4			tcy
C103	NRAS address setup time	t_{rads}			1		tcy
C104	NCAS0 / NCAS1 address hold time	t_{radh}			1		tcy
C105	NCAS0 / NCAS1 address setup time	t_{cads}			2		tcy
C106	NCAS0 / NCAS1 address hold time	t_{cadhw}			3		tcy
C107	NCAS0 / NCAS1 data setup time	t_{cwds}			3		tcy
C108	NCAS0 / NCAS1 data valid time	t_{cadv}			120		ns
C109	NRAS data valid time	t_{radv}			300		ns
C110	Data hold time	t_{cadhr}			0		ns
C111	NWE delay time	t_{wcd}			3		tcy
C112	NWE pulse width	t_{wel}			5		tcy
C113	Refresh period (Playback f_S=44.1 kHz) Memory system ON with decode sequence executed.	t_{ref}	16 Mbits, full bits			5.9	ms
C114		t_{ref}	16 Mbits, 4-bit compression			23.3	ms
C115		t_{ref}	4 Mbits, full bits			3.0	ms
C116		t_{ref}	4 Mbits, 4-bit compression			11.7	ms
C117		t_{ref}	1 Mbit, full bits			1.5	ms
C118		t_{ref}	1 Mbit, 4-bit compression			5.9	ms

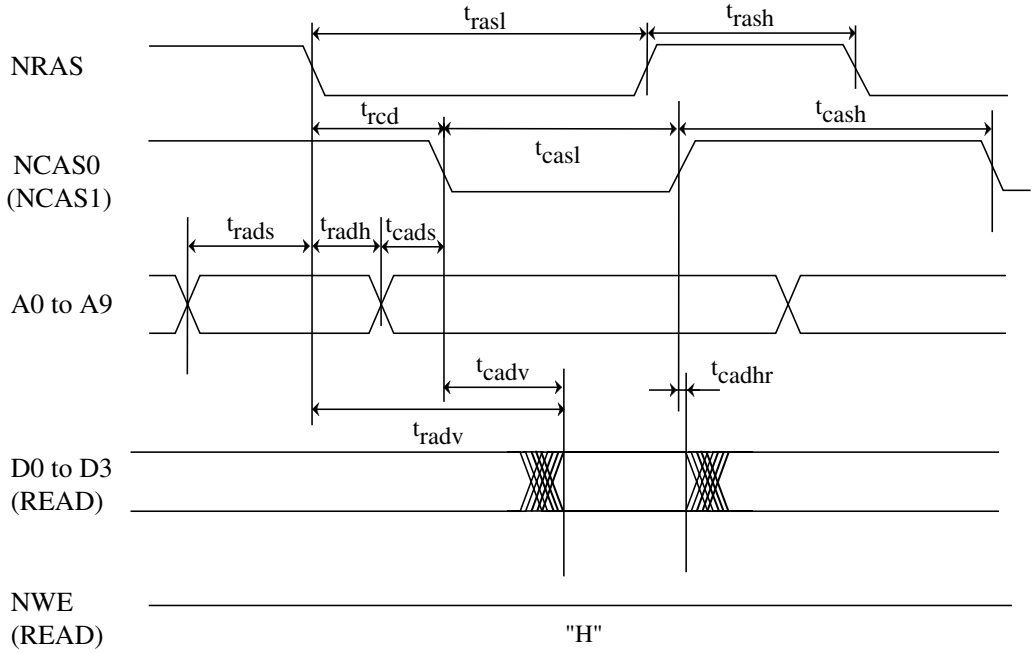
tcy: One system clock cycle which is indicated as 1/(16.9344 MHz) seconds.

DRAM Access Timing (NRAS, NCAS0, NCAS1, NWE, A0 to A9, D0 to D3)

・Write Timing

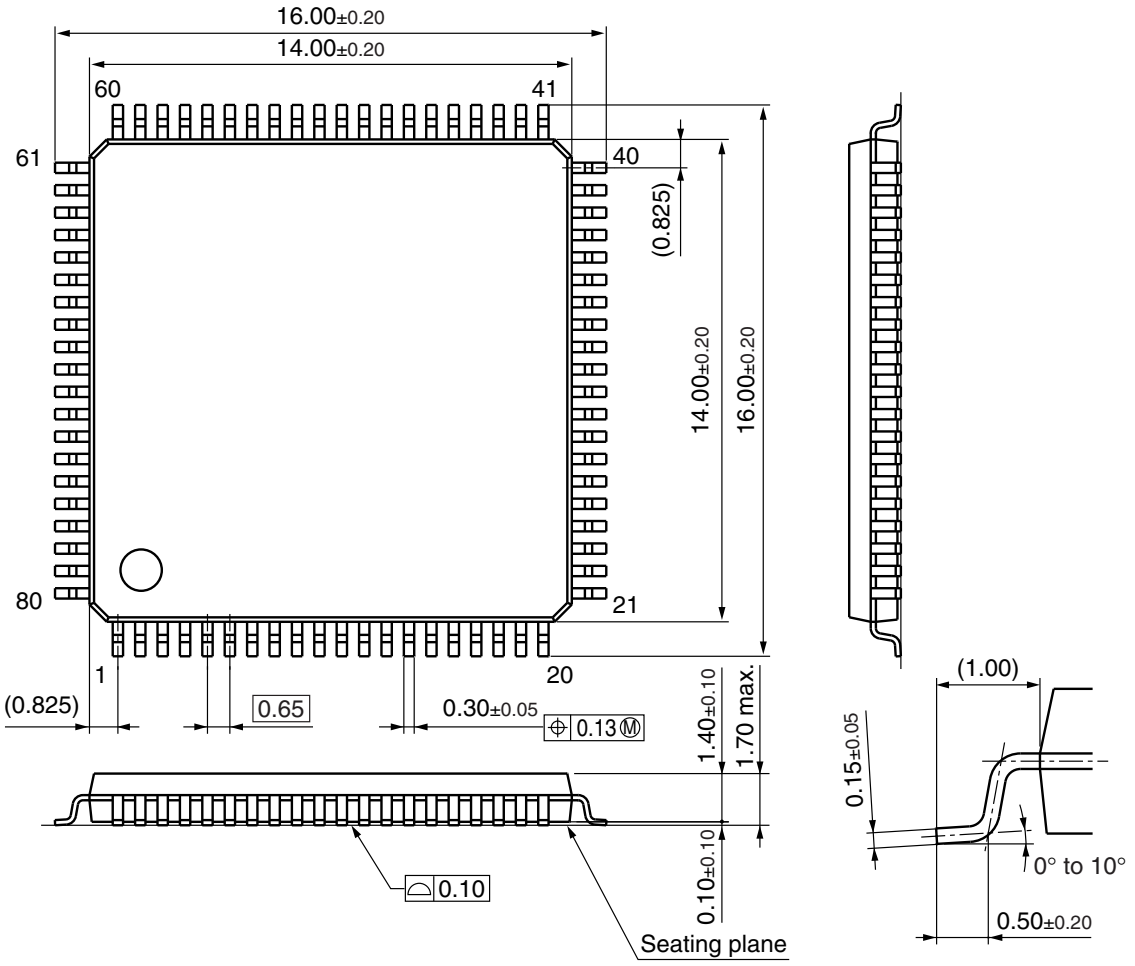


・Read Timing



Package Dimensions (Unit: mm)

• LQFP080-P-1414A (lead-free package)



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Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

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