Advance Product Information

VSC7969

3.125Gb/s Integrated Transimpedance and Limiting Amplifier with Signal Detect

Features

- Integrated TIA and Limiting Amplifier
- Low Power Consumption for SFF Applications
- TO Package-Compatible Layout
- On-Chip Signal Detect
- On-Chip Linear Photocurrent Monitor
- Single 3.3V Supply
- 5V Supply Operation via Wirebond Option
- Compatible with PIN or Avalanche Detectors
- Packages: 16-Pin TSSOP, TO-46, Bare Die

Applications

- 2.488Gb/s, 3.125Gb/s SONET OC-48/ SDH STM-16
- 2.125Gb/s Fibre Channel
- 2.5Gb/s or 3.125Gb/s Ethernet Applications with 8B/10B Overhead
- SFF Transceivers

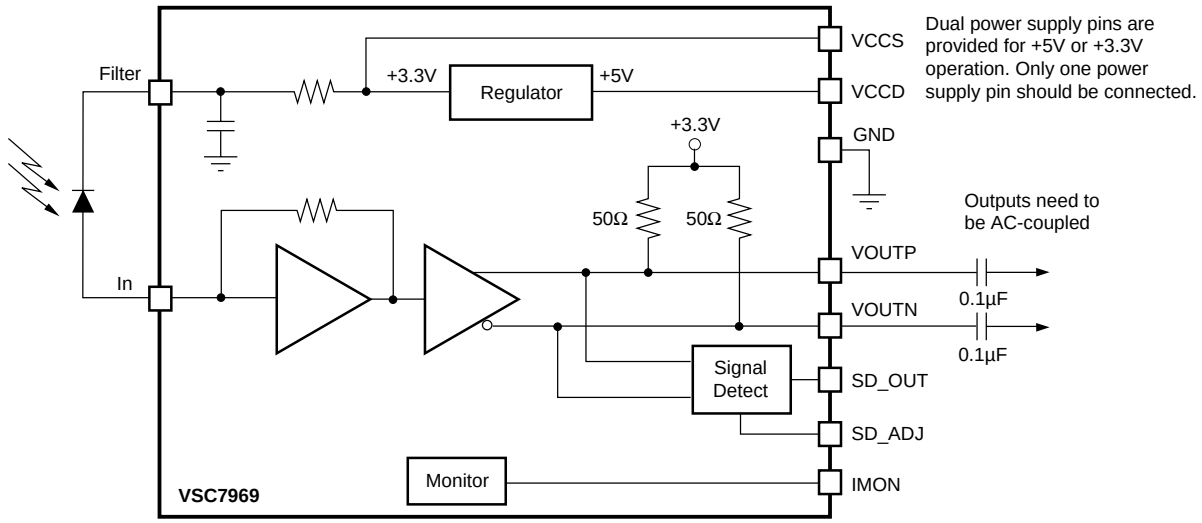
General Description

The VSC7969 is a 3.125Gb/s transimpedance amplifier IC with a built-in limiting amplifier, a signal detect feature and a photocurrent monitor. The VSC7969 does not require any external electrical components in the construction of a high performance optical receiver such as for SONET/SDH applications. The analog output is a differential signal with a minimum amplitude of 200mVp-p (single-ended). The VSC7969 operates with a single power supply with a maximum power dissipation of 300mW. A PIN photodiode or APD can be connected and separately biased to provide optimal performance.

The VSC7969 provides filtered bias for MSM and PIN photodetectors; applications using an APD photodetector must supply bias separately. The VSC7969 also provides a photocurrent monitor whose output is linearly proportional to the input photocurrent.

The VSC7969 can operate from a single +3.3V supply or a +5V or -5.2V supply. The VSC7969 is offered in die form and in a 16-pin plastic thin-shrink small outline package (TSSOP-16). A fully tested TO-46 outline packaged receiver with a photodetector is also available.

Block Diagram



Electrical Characteristics

Table 1: AC Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
ΔI_{PH}	Input Photocurrent Swing			2.2	mA	Peak-to-peak AC current amplitude
$I_{PHS-AVG}$	Average Photocurrent Sensitivity		4		µA	-23dBm average optical power with a detector responsitivity of 0.8A/W.
$I_{PHS-PEAK}$	Peak Input Photocurrent Sensitivity		8		µA	-23dBm average optical power with a detector responsitivity of 0.8A/W.
ΔV_{OUT-SE}	Single-Ended Output Voltage Amplitude	200	250	300	mV	Single-ended peak-to-peak measurement, I_{IN} >20µA.
$\Delta V_{OUT-DIFF}$	Differential Output Voltage Amplitude	400	500	600	mV	Differential peak-to-peak measurement, I_{IN} >20µA.
t_R, t_F	Rise and Fall Time		60	100	ps	At 2.2mAp-p input photocurrent swing. 20% to 80%.
Z_T(1)	Transimpedance Gain	20k	27k	40k	Ω	Differential measurement
ΔZ_T(1)	Ripple in Passband Transimpedance		1		dB	Modulation frequency between F_L and BW
BW	Upper -3dB Bandwidth	2.2	2.5	3.0	GHz	Referenced to 10MHz, CPD = 0.6pF
F_L	Lower -3dB Cutoff Frequency			100	kHz	Referenced to 10MHz, CPD = 0.6pF with no external components
Z_O	Output Impedance		50		Ω	Single-ended
PSRR	Power Supply Rejection Ratio		TBD			
I_{NOISE}	Input-Referred rms Noise Current		500		nA	30kHz to 2.5GHz
C_{PD}	Photodetector Capacitance	0.4	0.6	0.8	pF	Bias voltage on detector at 2.0V
SD_H	Signal Detect Hysterisis	1	2	4	dB	Electrical measurement on SD pin
SD_{A-OPEN}	Signal Detect Assertion Level	3	5	9	µA	Average photocurrent with SD open.
SD_{D-OPEN}	Signal Detect Deasseration Level	1.0	2.2	3.0	µA	Average photocurrent with SD open.
$SD_{A-SHORT}$	Signal Detect Asseration Level	6	10	18	µA	Average photocurrent with SD shorted to ground.
$SD_{D-SHORT}$	Signal Detect Deasseration Level	2.0	4.4	6.0	µA	Average photocurrent with SD shorted to ground.
SD_{HIGH}	Signal Detect HIGH Logic Level		V_{CCS} - 0.3		V	
SD_{LOW}	Signal Detect LOW Logic Level		0.5	0.8	V	

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
MON	Slope of Linear Analog Photocurrent Monitor vs Input Optical Power		0.8		µA/µW	0Ω to 2kΩ to V_{CC} with a detector responsitivity of 0.8A/W
DC	Duty Cycle	-5		+5	%	
$IMON_{RANGE}$	Photocurrent Monitor Linearity Range	5		200	µA	
$IMON_{OFFSET}$	Photocurrent Monitor Offset	0		10	µA	
R_J	Random Jitter(2)		TBD		ps	Peak-to-peak
D_J	Deterministic Jitter(3)		TBD		ps	Peak-to-peak

NOTES: (1) The transimpedance gain is defined as $Z_T = (\Delta V_{OUT - DIFF})/\Delta I_{PH}$. (2) Using 1111100000 pattern at 2.5Gb/s to measure the standard deviation of the edge of the pattern, multiply the standard deviation by 14 to achieve the total random jitter. (3) +K28.5 - K28.5 (0011111010110000010l).

Table 2: DC Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
GND	Negative Supply Rail		0		V	
V_{CCS}	Positive Supply Rail for 3.3V Operation	3.0	3.3	3.6	V	
V_{CCD}	Positive Supply Rail for 5V Operation	4.5	5.0	5.5	V	
ICC	Power Supply Current		65	75	mA	3.3V
V_{OUT-CM}	Common-Mode Voltage on Output Pins		V_{CCS} - 125mV			Applicable to VOUTP and VOUTN pins at 50Ω load.
V_{ANODE}	Internal DC Bias Voltage on Detector Anode Contact	0.8	0.9	1.0	V	
$V_{CATHODE}$	Interal DC Bias Voltage on Detector Cathode Contact	V_{CCS} - 0.15V		V_{CCS}	V	
$V_{CAT-EXT}$	External DC Bias Voltage Permissable on Detector Cathode Contact		3.3	10	V	
V_{APD}	External DC Bias Voltage for Use with Avalanche Photodetector		60		V	

Absolute Maximum Ratings(1) (at T_A = +25°C, unless otherwise specified)

Power Supply Voltage (V_{CCS}) 3.6V
Power Supply Voltage (V_{CCD}) 5.5V
Junction Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -40°C to +125°C
Relative Ambient Humidity ..... 85%/+85°C

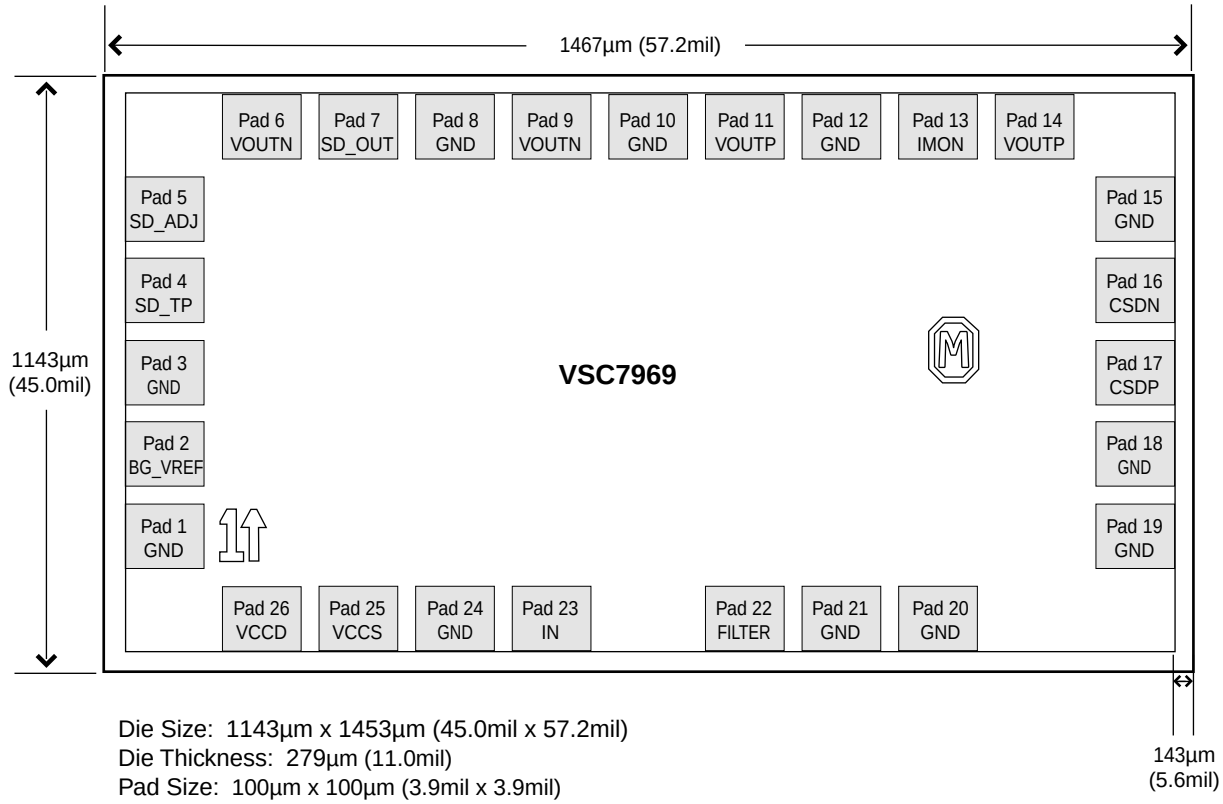
NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Positive Voltage Supply (V_{CCS}) 3.3V
Positive Voltage Supply (V_{CCD}) 5.0V
Negative Voltage Rail (GND) 0V
Ambient Temperature Range (T_A)(1) ..... -40°C to +85°C

Bare Die Descriptions

Figure 1: Pad Assignments



Die Size: 1143µm x 1453µm (45.0mil x 57.2mil)
Die Thickness: 279µm (11.0mil)
Pad Size: 100µm x 100µm (3.9mil x 3.9mil)
Pad Passivation Opening: 86µm x 86µm (3.4mil x 3.4mil)
Scribe Size: 143µm (5.6mil)

Table 3: Pad Coordinates

Signal Name	*Pad Number*	*Coordinates (µm)*		*Description*
		X	*Y*	
GND	1	130	250	Negative power supply rail (typically 0V)
BG_VREF	2	130	375	Band Gap voltage reference 1.24V for testpoint, no connect
GND	3	130	500	Negative power supply rail (typically 0V)
SD_TP	4	130	625	Signal Detect test point, DO NOT CONNECT.
SD_ADJ	5	130	750	Signal Detect threshold adjustment (see *Application amd Usage* section)
VOUTN	6	137	875	Complementary logic output (logic LOW when photocurrent is HIGH)
SD_OUT	7	280	875	Signal detect output (logic HIGH when photocurrent exceeds SD_A)
GND	8	405	875	Negative power supply rail (typically 0V)
VOUTN	9	530	875	Complementary logic output (logic LOW when photocurrent is HIGH)
GND	10	655	875	Negative power supply rail (typically 0V)
VOUTP	11	780	875	Positive logic output (logic HIGH when photocurrent is HIGH)
GND	12	905	875	Negative power supply rail (typically 0V)
IMON	13	1030	875	Photocurrent Monitor
VOUTP	14	1173	875	Positive logic output (logic HIGH when photocurrent is HIGH)
GMD	15	1180	750	Negative power supply rail (typically 0V)
CSDN	16	1180	625	Test point for Signal Detect capacitor. DO NOT CONNECT.
CSDP	17	1180	500	Test point for Signal Detect capacitor. DO NOT CONNECT.
GND	18	1180	375	Negative power supply rail (typically 0V)
GND	19	1180	250	Negative power supply rail (typically 0V)
GND	20	1030	125	Negative power supply rail (typically 0V)
GND	21	905	125	Negative power supply rail (typically 0V)
FILTER	22	780	125	Photodetector cathode connection (filtered V_{CC})
IN	23	530	125	Photodetector anode connection
GND	24	405	125	Negative power supply rail (typically 0V)
VCCS	25	280	125	Positive power supply rail for 3.3V operation
VCCD	26	137	125	Positive power supply rail for 5V operation

Package Pin Descriptions

Figure 2: Pin Diagram

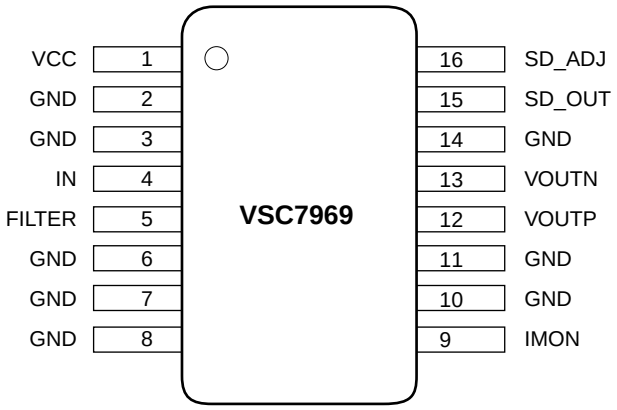
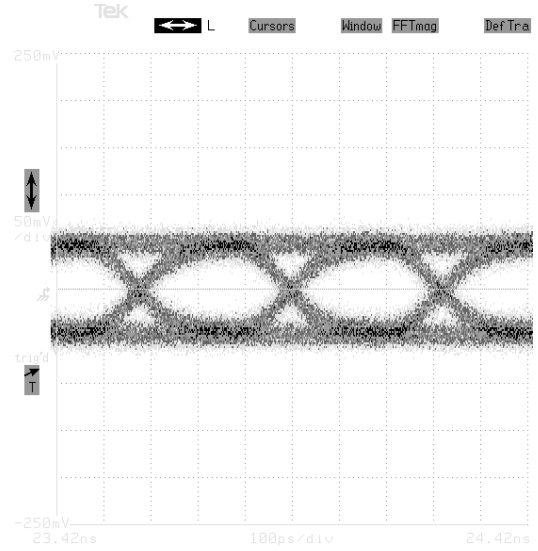
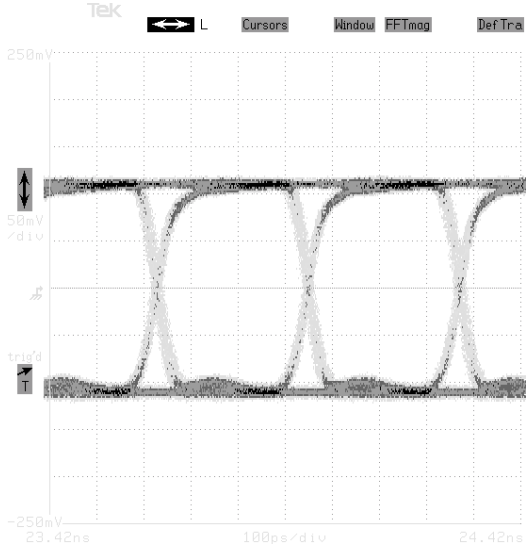
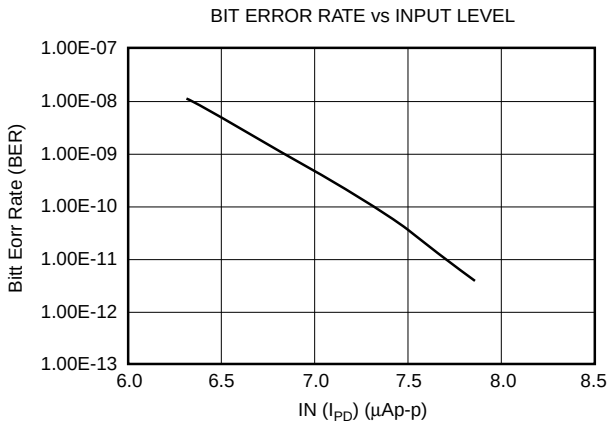
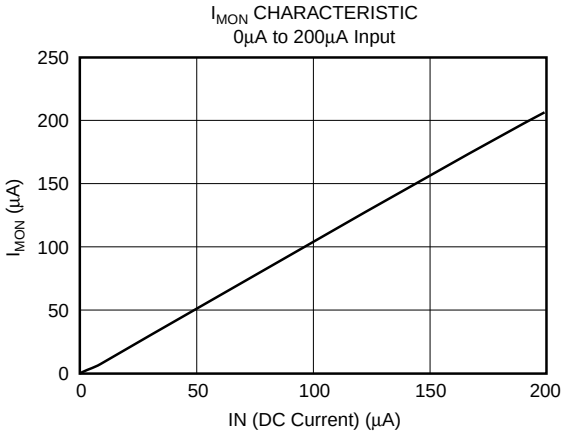


Table 4: Pin Identifications

Pin Name	*Pin No.*	*Description*
VCC	1	Power Supply
GND	2	Ground
GND	3	Ground
IN	4	Photodetector Anode Connection
FILTER	5	Photodetector Cathode Connection (filtered V_{CC})
GND	6	Ground
GND	7	Ground
GND	8	Ground
IMON	9	Photocurrent Monitor
GND	10	Ground
GND	11	Ground
VOUTP	12	Positive Logic Output (logic HIGH when photocurrent is HIGH)
VOUTN	13	Complementary Logic Output (logic LOW when photocurrent is HIGH)
GND	14	Ground
SD_OUT	15	Signal Detect Output (logic HIGH when photocurrent exceeds SD_A)
SD_ADJ	16	Signal Detect Threshold Adjustment (see *Applications and Usage* section)

Typical Operating Characteristics

Electrical Eye Diagram, ***Input = 8µAp-p, 3.125Gb/s, PRBS 2^{31}-1*** ***T_A = º+25C, V_{CC} = 3.3V***	***Electrical Eye Diagram,*** ***Input = 100µAp-p, 3.125Gb/s, PRBS 2^{31}-1*** ***T_A = º+25C, V_{CC} = 3.3V***
	

Bit Error Rate vs Input Level	***IMON Characteristic, 0µA to 200µA Input***
	

Circuit Description

The VSC7969 data path consists of several stages: transimpedance input stage, limiting amplifier, and output driver. The transimpedance amplifier accepts current from a photodetector connected to the input pad 'IN' and converts the input current to a differential output voltage. The signal then travels to the second stage limiting amplifier which provides DC restoration, eliminating the DC component of the input signal. The linear photocurrent monitor and signal detect function is also provided by this stage. The final stage consists of an output driver with a differential pair connected to V_{CC} via 50Ω internal pull-up resistors. The overall effective differential transimpedance of the VSC7969 is typically 27kΩ. The limited output single-ended voltage swing is typically 250mVp-p.

Design Guidelines

Power Supply

The VSC7969 is supplied by a single supply voltage; for +3.3V operation, the supply votlage should be applied to only V_{CCS}. For +5V operation, the supply voltage should be applied to only V_{CCD}.

Data Outputs

The outputs of the VSC7969 need to be AC-coupled. This capacitor will determine the low frequency cutoff for the system, which is directly related to the receiver's deterministic jitter. For ATM/SONET or other applications using PRBS NRZ data, select a capacitor of at least 0.1µF or greater, which provides less than 32kHz low frequency cutoff. For Fibre Channel, Gigabit Ethernet, or other applications requiring 8B/10B data coding, select a capacitor of at least 0.01µF or greater, which provides less than 320kHz low frequency cutoff.

The outputs can be used single-ended or differential. For best performance, differential operation is recommended. If single-ended operation is necessary, the unused output should be AC-coupled and terminated with an impedance equal to the load on the pin in use.

Signal Detect

The signal detect feature of the VSC7969 provides a CMOS level output corresponding to the input current level to the transimpedance amplifier. The assert and deassert levels of the signal detect pin can be adjusted by placing an optional resistor from SD_ADJ to ground. The following tables show the two extremes at which the signal detect pin will operate; open circuit and short-ciruit to ground.

Table 5: Signal Detect Function, SD_ADJ Open

	Electrical			
	Min	***Typ***	***Max***	***Units***
Assert	3	5	9	µA
Deassert	1	2.2	3	µA
Hysteresis	1	2	4	dB

With SD_ADJ (pin 16) shorted to ground, thresholds are 3dB higher, as shown in Table 6.

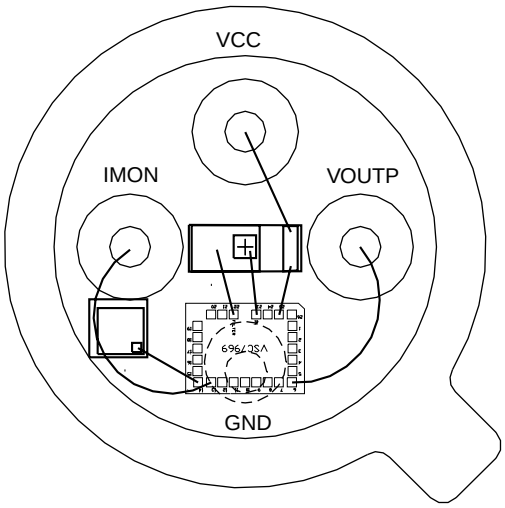
Table 6: Signal Detect Function, SD_ADJ Shorted to Ground

	Electrical			
	Min	***Typ***	***Max***	***Units***
Assert	6	10	18	µA
Deassert	2	4.4	6	µA
Hysteresis	1	2	4	dB

Photodetector Current Monitor

The IMON pin provides a linear measurement of the average input current from the photodetector to the transimpedance amplifier. For example, if 20µA is the average input current to the transimpedance amplifier, the current through the IMON pin will be 20µA (see the typical operating curve "*IMON Characteristic, 0µA to 200µA*). To use this feature, connect the IMON pin to V_{CC} using a resistor less than 2kΩ. If this feature is not used, the IMON pin can be left unconnected.

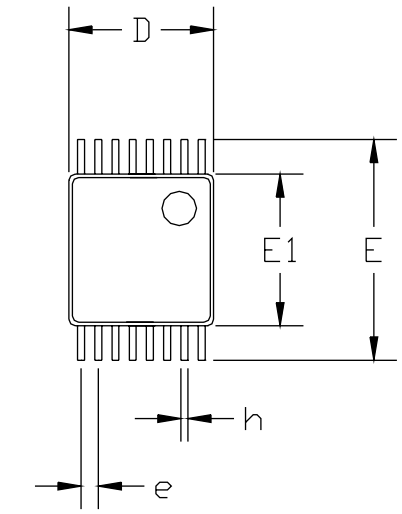
Application Information



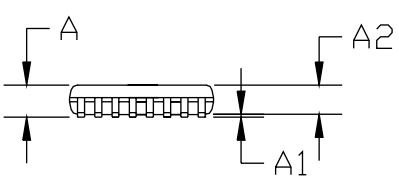
NOTES:
No external components required.
Unused output is AC-coupled and terminated to 50Ω.

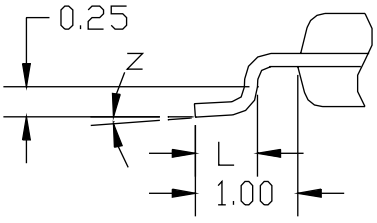
Package Information

TSSOP-16



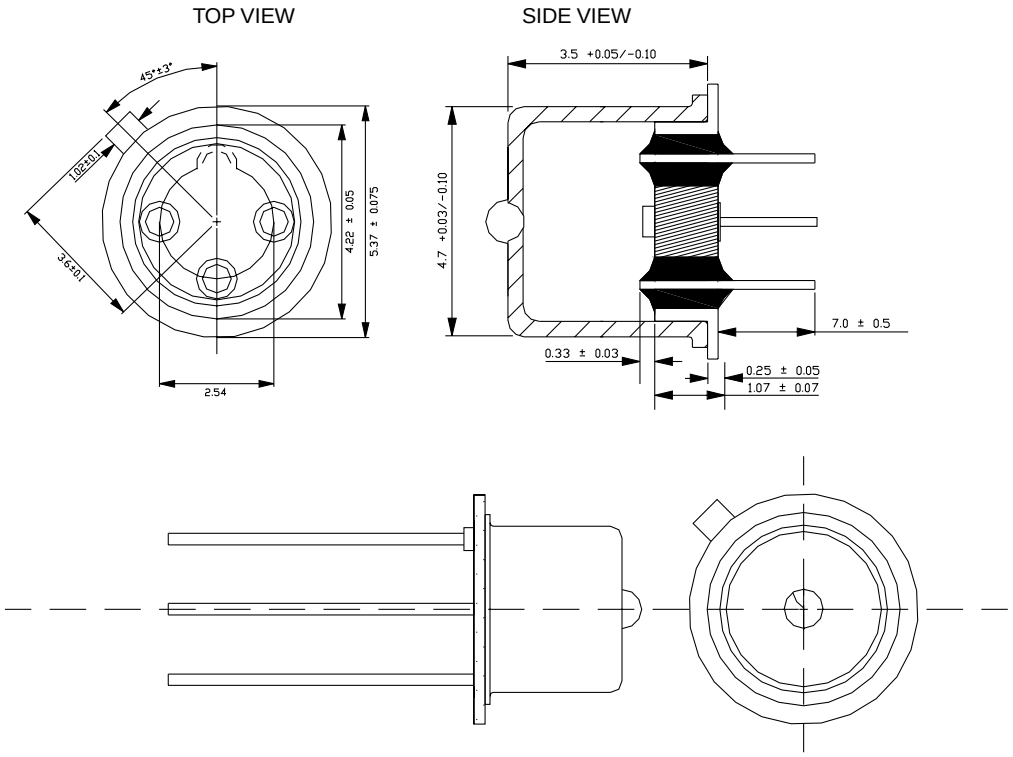
SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	TSSOP		
	MIN.	NOM.	MAX.
A	---	---	1.10
A_1	0.05	---	0.15
A_2	0.85	0.90	0.95
D	5.00 BSC.		
E	6.40 BSC.		
E_1	4.30	4.40	4.50
L	0.50	0.60	0.70
e	0.65 BSC.		
h	0.19	---	0.30
z	0	---	8





1. All dimensioning and tolerancing per ASME. Y14.5-1994
2. Controlling dimension: millimeter
3. This outline conforms to JEDEC Publication 95 Registration MS-026

TO-46 Ball Lens Package



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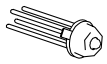
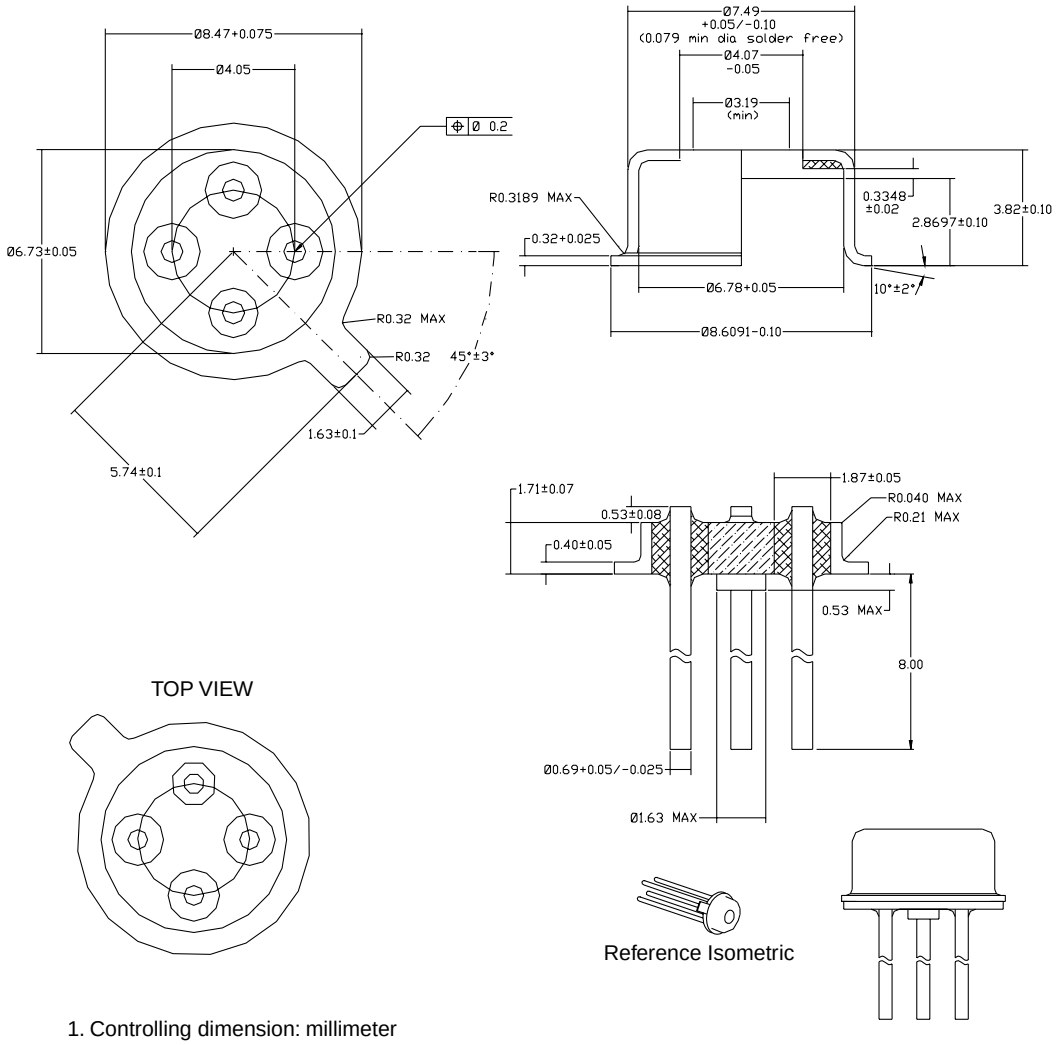


Reference Isometric

TO-46 Flat Window Package



1. Controlling dimension: millimeter

Ordering Information

The order number for this product is formed by a combination of the device type and package type.

VSC7969 xx

Device Type
3.125Gb/s Integrated Transimpedance and Limiting Amplfier with Signal Detect

Package
YD1: TSSOP-16, 3.3V Supply
YD2: TSSOP-16, 5V Supply
W: Dice Waffle Pack
WD1A: TO-46 Ball Lens, 3.3V Supply, VOUTN/VOUTP Outputs
WD1B: TO-46 Ball Lens, 3.3V Supply, VOUTN/IMON Outputs
WD2A: TO-46 Ball Lens, 5V Supply, VOUTN/VOUTP Outputs
WD2B: TO-46 Ball Lens, 5V Supply, VOUTN/IMON Outputs

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