W90100F PA-RISC
Embedded Micro-Controller

(Preliminary)

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1. General Description

The W90100 Embedded Micro-controller is part of Winbond's W90K Embedded processor family. The W90100 is a high-performance, highly integrated 32-bit processor and it is designed to be easily interfaced to a variety of laser printer mechanisms including: laser, ink-jet and thermal types.

The W90100 CPU core is based on the HP PA-RISC architecture and is upward code compatible with the W90K. The PA-RISC architecture incorporates traditional RISC elements, such as instruction pipelining, a register-to-register instruction set and a large, general-purpose register file. Separate on-chip instruction and data caches allow the W90100 to fetch an instruction and access data in a single processor cycle.

The W90100 includes several features that greatly increase performance, reduce system component count and ease the overall system design task in a printer application. These features include a DRAM controller, FLASH ROM controller, serial port with FIFO, IEEE 1284 parallel port, timer/counters, Programmable I/O port, DMA controller, DPI interface, and enhanced debug support; all features that are commonly required in general embedded applications. In addition, the W90100 supports generic printer video and communications interface signals for easy interfacing with generic laser printer engine. To further increase the overall performance of the W90100 printer system, both image enhancement, including edge enhancement and gray scale enhancement; as well as frame memory compression are integrated into the W90100 micro-controller.

2. W90100 Features

- PA-RISC architecture
  - PA-RISC 1.1 third edition instruction set
  - PA-RISC level zero implementation
  - Support PA-RISC Multimedia Extension 1.0 instruction set
  - W90K binary compatible for user software
- High-performance, singlesaclar implementation
  - Five-stage pipeline
  - Precise, efficient handling of pipeline stalls and exceptions
  - Delayed branch with static branch prediction
    - Forward: not taken; Backward: taken
    - One-cycle stall when prediction is wrong
  - Load Scheduling
    - Both load and store can be queued when miss
    - Load/store single cycle execution after previous miss
- On-chip cache memory
  - Internal I-cache: Direct mapped, 4 KB cache (256 entries, four words/entry)
    - Wrap around fetching when cache miss; Cache freeze capability
  - Internal D-cache: 2-way set associative, 2 KB cache (256 entries, 4words/entry)
    - Write-back cache with write buffer; Write-through option
    - New line send to CPU before dirty line write back
- Enhanced debug capability
  - Debug SFU supports both instruction breakpoint and data breakpoint
    - Two sets of instruction breakpoint regiters are provided (Mask and Offset)
    - Two sets of data breakpoint regiters are provided (Mask and Offset)
  - JTAG TAP controller for JTAG ICE support
  - IEEE 1149.1 JTAG boundary scan
- High on-chip integration and simple I/O interface
  - Memory controller to interface with DRAM, ROM, FLASH, and DPI interface
    - Support both Fast-Page mode and EDO DRAM
    - Upto 4 banks of DRAM, 64M Bytes per bank
    - Support 8-bit, 16-bit, and 32-bit ROM
    - Upto 4 banks of ROM or FLASH, 4M Bytes per bank
  - Internal 2-channel 16-bit DMA controller
  - Serial port with FIFO
  - IEEE 1284 parallel port for input
  - IEEE 1284 parallel port for output
  - 8-bit Programmable I/O port
  - Two 24-bit timer/counters
  - Image Enhancement Technology
    - Edge enhancement as well as 1 bit and 8 bit grayscale enhancement to enhance the output print quality.
  - PowerBand® Frame Memory Reduction
    - Built-in CODEC's to reduce the system memory requirements by up to 8X in printer applications.
- Direct Generic Printer Engine Interface
- Economy mode: Power down and toner saver modes for economical operation

W90100 Microcontroller Feature Sets

Basic Features	W90100
Bus	CPU Bus
Data Cache	Yes
Size	2K Bytes
Associativity	2 Way
Instruction Cache	Yes
Size	4K Bytes
Associativity	Direct mapped
Multimedia extension	Yes
JTAG Debug support	JTAG ICE support
H/W Breakpoints	Yes
Instruction H/W Breakpoints	2 sets (mask and offset)
Data H/W Breakpoints	2 sets (mask and offset)
DX/2 support	Yes
ROMInterface	Yes
Banks	4
Width	8, 16, 32 bits
Max size/bank	4 MBytes/Bank
Boot-up ROM Width	8, 16, 32 bits
Burst-mode access	Supported
DRAM Interface	Yes
Banks	4
Width	32 bits
Max size/bank	64 MBytes/Bank
Initial /Burst access cycles	3/2/2/2 or 2/1/1/1
DRAM Parity	No
On-Chip Line Store SRAM	Yes
Width	16 bits
Size	8K Bytes
External CODEC SRAM Interface	Yes
Width	8-bit
Max size	64K Bytes
On-chip DMA	Yes
Total number of channels	2
Mem-CODEC transfer	Yes
Mem-to-Mem transfer	Yes
Mem-to-ECP transfer	Yes
On-chip generic video interface	Yes
On-chip interrupt controller	Yes
Interrupt pins	INT1, INT2
On-chip timer	Yes
Number of channels	2 Channels (24-bit)
Serial Ports	1
16550 FIFO support	Yes
Parallel Ports	2
ECP support	Yes
FIFOsupport	Yes
1284 support	Yes
Endian	Big-Endian
Operating voltage	5V, 3.3V
Clock speed	40 MHz
Package	208 PQFP

W90100 Microcontroller Feature Sets

Advanced Features	W90100
On-chip Codec	Yes
JBIG	Yes
Contone	Yes
On-chip Enhancement Support	Yes
Edge Enhancement	Yes
Resolution Doubling 300 dpi to 600 dpi 600 dpi to 1200 dpi	Yes
Grayscale Enhancement 1 bit 8 bit	Yes
Toner Saver	Yes

3. 208-Pin PQFP Pin Configuration

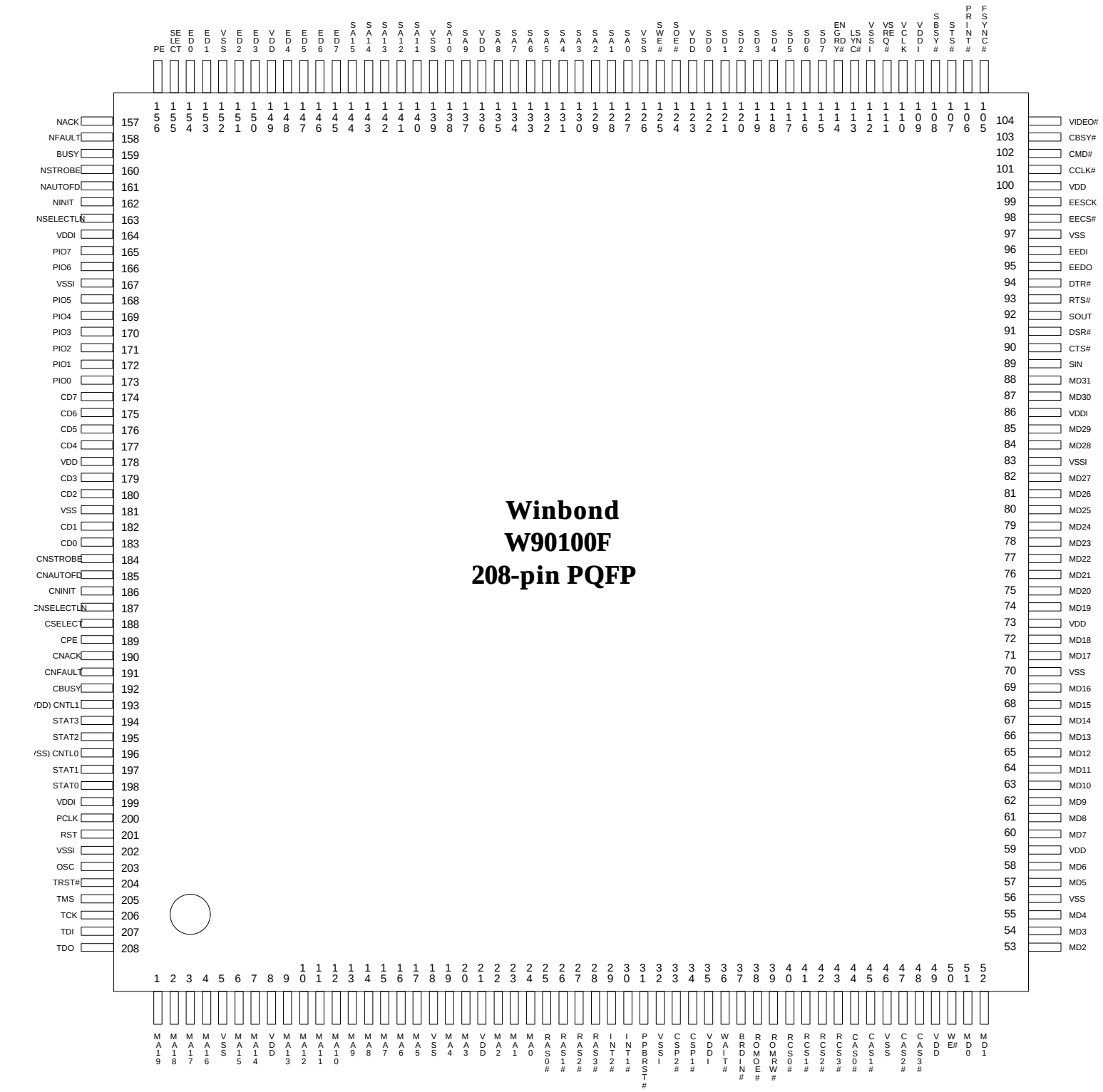


Figure 3.1 W90100 Pin Configuration

4. W90100 Pin Description

PIN Name	DIR	PIN #	DESCRIPTION
JTAG Boundary Scan Interface			
TCK	I	206	JTAG test clock input
TRST#	I	204	JTAG test reset input
TMS	I	205	JTAG test mode select input
TDI	I	207	JTAG test data input
TDO	O	208	JTAG test data output
CPU Signal			
RST	I	201	RESET input
PCLK	I	200	CLOCK input
OSC	I	203	Oscillator input for Timer, UART, and DRAM refresh
STAT[0:3]	O	198,197,195,194	CPU status output
Generic Printer Engine Interface			
PRINT#	O	106	Print Request
FSYNC#	I/O	105	Frame Sync
LSYNC#	I	113	Line Sync
VIDEO#	O	104	Video Data Stream
VCLK	I	110	Video Shift Rate Clock
CBSY#	O	103	Command Busy
SBSY#	I	108	Status Busy
CMD#/STS#	I/O	102	Command/Status Data
STS#	I	107	Status Data
CCLK#	I/O	101	Command Clock
ENGRDY_	I	114	Printer Enginer Ready
VSREQ#	I	111	Vsync Request
ECP Interface (Peripheral side)			
Busy	O	159	ECP busy input signal
nFault	O	158	ECP fault input
nAck	O	157	ECP acknowledge input
PError	O	156	ECP parity error
Select	O	155	ECP Select
nSelectIn	I	163	ECP select output
nInit	I	162	ECP initialization
nAutoFd	I	161	ECP Autofeed
nStrobe	I	160	ECP Strobe
ED[0:7]	I/O	154,153,151,150,148,147,146,145	ECP Data bus
Centronics Output Port			
CBusy	In	192	Centronics printer busy input
CnFault	In	191	Centronics Error input
CnAck	In	190	Centronics Acknowledge input
CPE	In	189	Centronics Paper End input
CSelect	In	188	Centronics Select input
CnSelectIn	O	187	Centronics Select in output
CnInit	O	186	Centronics Init output
CnAutoFd	O	185	Centronics auto feed output
CnStrobe	O	184	Strobe pulse to write data
CD[0:7]	I/O	183,182,180,179,177,176,175,174	Centronics Data bus
Programmable Input/Output Port			
PIO[0:7]	I/O	173,172,171,170,169,168,166,165	Programmable input/output port
Memory Controller Interface			
RAS#[0:3]	O	25,26,27,28	DRAM Row Address Strobe, Banks 0-3
CAS#[0:3]	O	44,45,47,48	DRAM Column Address Strobes, Byte 0-3
WE#	O	50	DRAM Write Enable

RCS#[0:3]	O	40,41,42,43	ROM/FLASH Chip Selects, Banks 0-3
MA[19:0]	O	1,2,3,4,6,7,9,10,11,12,13,14,15,16,17,19, 20,22,23,24	Memory controller Memory Address bus
MD[0:31]	I/O	51,52,53,54,55,57,58,60,61,62,63, 64,65,66,67,68,69,71,72,74,75,76, 77,78,79,80,81,82,84,85,87,88	Memory controller Data bus
ROM_OE_	O	38	ROM/FLASH output enable
ROM_RW_	O	39	ROM/FLASH read/write control signal
PPB_CSP1_	O	34	DPI interface chip select 1
PPB_CSP2_	O	33	DPI interface chip select 2
PPB_RST_	O	31	DPI interface reset signal
PPB_WAIT_	I	36	DPI interface wait signal
PPB_BRDIN_	I	37	DPI interface Board exist signal
PPB_INT1_	I	30	DPI interface interrupt 1
PPB_INT2_	I	29	DPI interface interrupt 2
CODEC SRAM interface			
SA[0:15]	O	127,128,129,130,131,132,133,134,135,13 7,138,140,141,142,143,144	CODEC SRAM address output
SD[0:7]	I/O	122,121,120,119,118,117,116,115	CODEC SRAM data bus
SWE	O	125	CODEC SRAM write enable
SOE	O	124	CODEC SRAM output enable
EEPROM interface			
EESCK	O	99	EEPROM clock
EECS_	O	98	EEPROM chip select
EEDI	O	96	EEPROM serial data output
EEDO	I	95	EEPROM serial data input
Serial Port Signal			
RTS_	O	93	Serial port request-to-send output
CTS_	I	90	Serial port clear-to-send input
DTR_	O	94	Serial port data-terminal-ready output
DSR_	I	91	Serial port data-set-ready input
SIN	I	89	Serial port input data
SOUT	O	92	Serial port output data
Power			
VDD	I	8,21,35,49,59,73,86,100,109,123,136,149,164,178,193,199	
GND			
VSS	I	5,18,32,46,56,70,83,97,112,126,139,152,167,181,196,202	

5. W90100 Application System Diagram

5.1 W90100 System Diagram

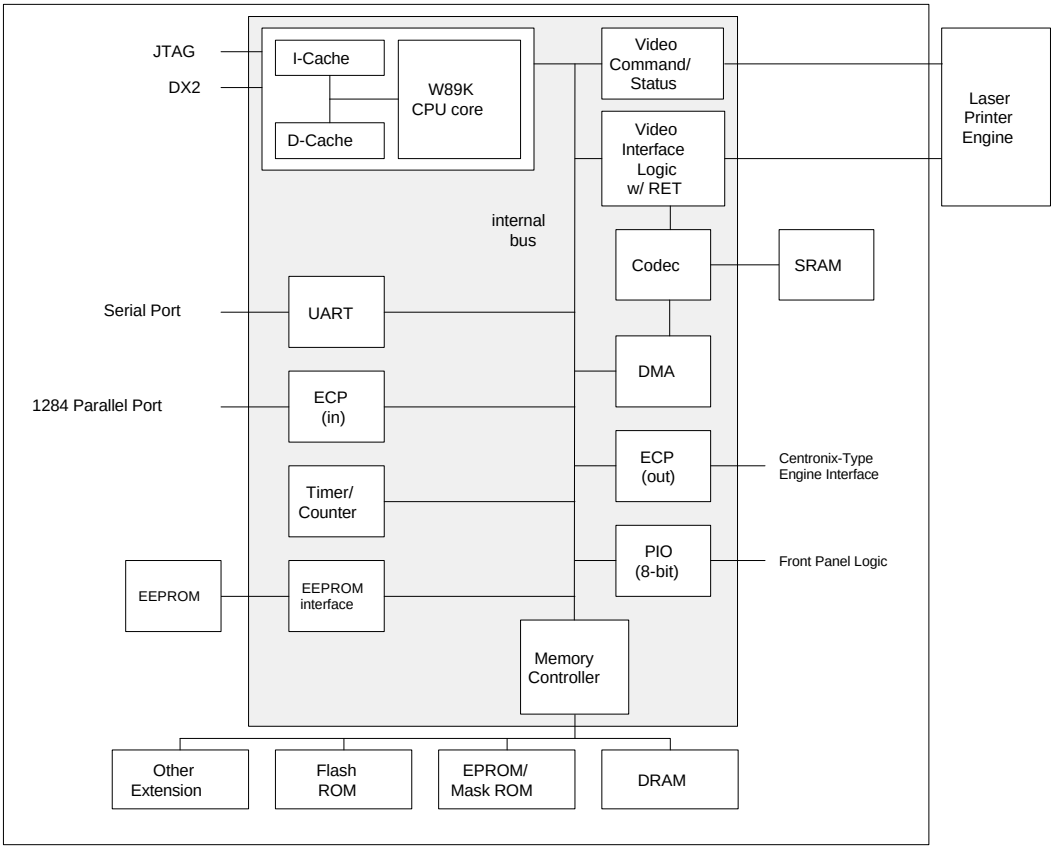


FIGURE 5.1 W90100 SYSTEM DIAGRAM

5.2. Reference Controller Features

W90100 Microcontroller Reference Board Feature Sets

Reference Board Features	W90100
Input/output	
Serial ports	1 on chip
Parallel ports	2 on chip
Network	
DPI daughter card	DPOdaughter card I/F connector on board
Image enhancement	
Image Enhancement Module	On-chip XLI image enhancement
PowerBand compression Codec	
Contone	On-chipPipeline proprietary contone codec
1-bit	On-chip Pipeline proprietary JBIG-like codec
Video engine I/F	On-chip
Connectors	
Serial	DB-25
Parallel 1 (printer input)	Centronics 36
Parallel 2 (engine i/f)	36 pin header (male)
Network	DPO interface header
Video i/f	NEC and SHARP Engine Connector

TABLE 5.2 W90100 CONTROLLER BOARD FEATURE SET

5.3 W90100 Controller Board

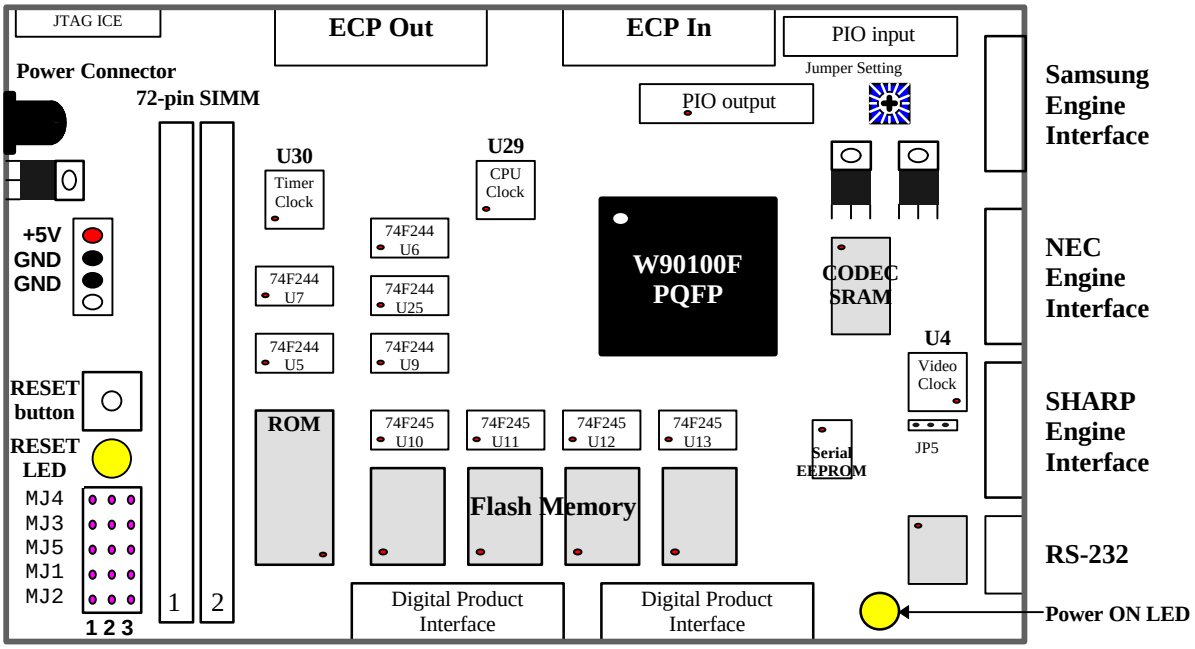


FIGURE 5.3 W90100 CONTROLLER BOARD

6. W90100 Block Diagram

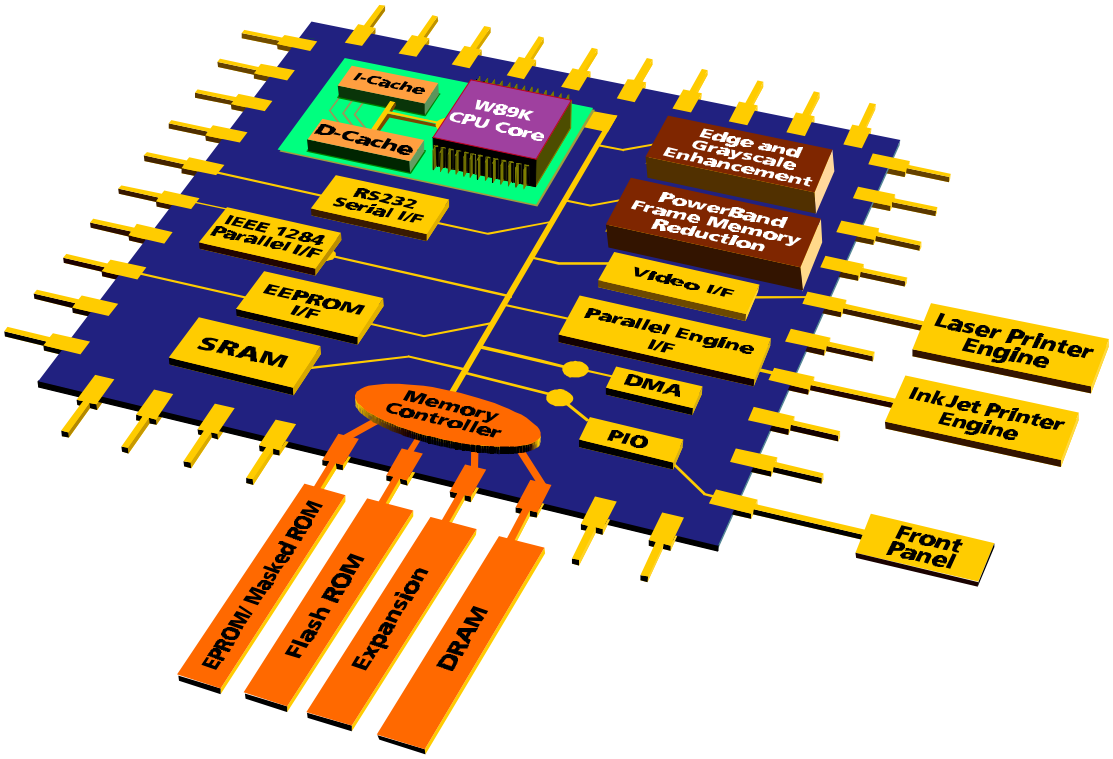


FIGURE 6.1 W90100 BLOCK DIAGRAM

7. W90100 Functional Description

The W90100 significantly reduces overall system cost because it integrates most printer system functions onto a single chip.

7.1 DRAM Controller and ROM Controller

7.1.1 DRAM controller

The DRAM controller supports four separate banks of dynamic memory. Either X8 or X32 SIMMs are supported. CAS#-before-RAS# refresh cycles are performed periodically, as determined by the refresh timer. The DRAM controller must arbitrate between access requests and refresh requests. Both EDO and page mode DRAM's are supported.

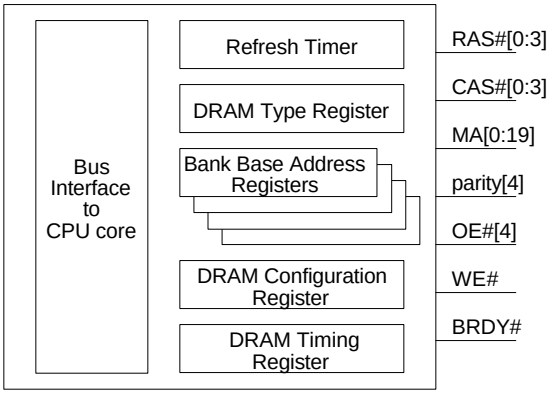


FIGURE 7.1 DRAM CONTROLLER BLOCK DIAGRAM

7.1.2 ROM, FLASH, and DPI interface controller

The ROM controller also supports upto four banks of ROM and the ROM can be 8-bit, 16-bit, or 32-bit.

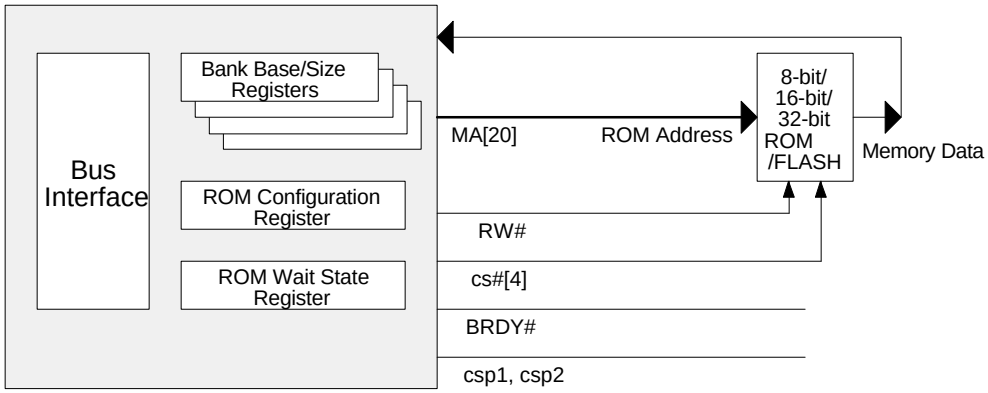


FIGURE 7.2 ROM CONTROLLER DIAGRAM

For each bank of ROM, two registers are used to specify the bank address range:

ROM Bank Base Address Register.

ROM Bank Size Register.

ROM Configuration Register is used to program the ROM data bus size of each bank.

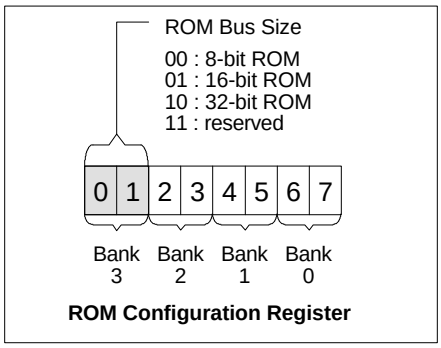


FIGURE 7.3 ROM CONFIGURATION REGISTER PROGRAMMING

ROM Read Wait State Register is used to program the number of wait states needed to access ROM. The cycle needed for writing the ROM is fixed.

Also, there are two base address registers provided for the DPI interface. The DPI interface always use 16-bit access for memory access and 8-bit access for the registers. The base register must be programmed with a value of 128K boundary

7.2 DMA Controller

The DMA Controller megacell provides two DMA channels to support DMA transfers between 16-bit I/O devices and main memory. The DMA mechanism will provide two different methods for performing DMA transfers: demand-mode transfers and block-mode transfers. The DMAC hardware is responsible for synchronizing transfers with memory or I/O devices.

When the DMAC is configured for demand mode, a device requests a DMA transfer with a request input (DREQ1:0#). The DMAC acknowledges the requesting device with an acknowledge signal (DACK1:0#) when the requesting device is accessed.

In block mode, DMA transfers are not requested by an external device. The DMA operation is initiated by software and continued until terminated or suspended. The DMA operation is started when the enable bit in the Configuration Register is set.

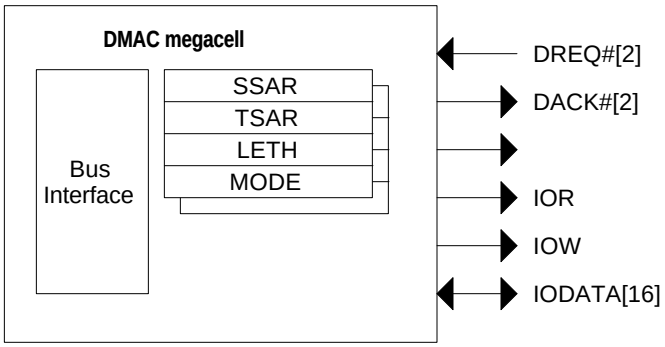


FIGURE 7.4 DMA CONTROLLER

In programming the megacell registers, the register address is defined by the BASE register plus the offset value.

7.3 Timer / Counter

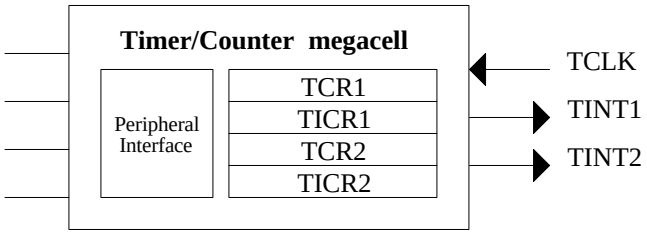


FIGURE 7.5 TIMER/COUNTER MEGACELL

Two 24-bit decrementing timers are implemented. When the timer's interrupt enable bit is set to one and the counter decrements to zero, the timer will assert the associated interrupt signal. The interrupt signal will assert one of the 32 external interrupts defined by the EI bits in the control register. When a timer reaches zero, the timer hardware reloads the counter with the value from the timer initial count register and continues decrementing.

Each timer is controlled and initialized by two registers: a timer control register and an timer initial count register. These registers are all memory mapped I/O registers.

7.3.1 Timer Control register:

TCR

Pre-Scalar (PS): A pre-scalar value can be used to divide the input clock.

Interrupt Enable bit (IE): When IE is set to one and the counter decrements to zero, the timer asserts its interrupt signal to interrupt the CPU.

Counter Enable bit (CE): Setting the CE bit to one causes the timer to begin decrementing. Setting the CE bit to zero stops the timer.

Timer Interrupt bit (TI): The timer sets this bit to one to indicate that it has decrement to zero. This bit remain one until software sets it to zero.

7.3.2 Timer Initial Count Register:

TICR

A 24-bit read/write register for the initial counter value.

7.4 Serial I/O (UART) Megacell

The serial I/O (UART) megacell implements a full-duplex, bi-directional UART with FIFO.

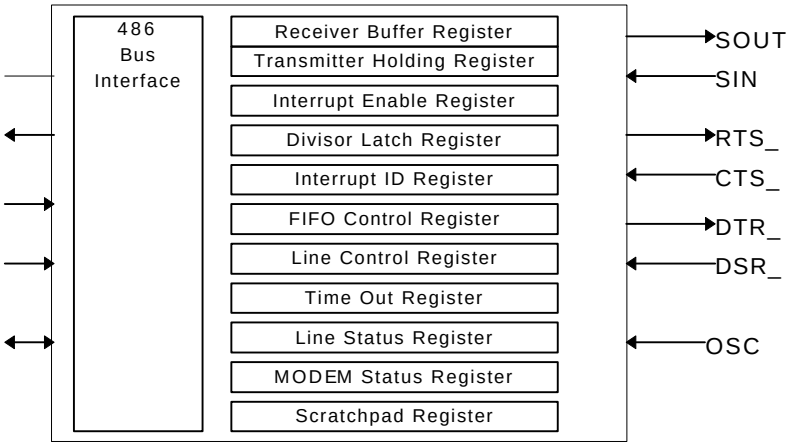


FIGURE 7.6 SERIAL I/O (UART) WITH FIFO

7.5 Parallel Port

The parallel port megacell implements the IEEE 1284 parallel port. The IEEE 1284 standard provides for high speed bi-directional communication between the PC and an external peripheral.

The parallel port defines 5 modes of data transfer. Each mode provides a method of transfering data in either the forward direction, reverse direction, or bi-directional data transfer. The defined modes are:

- Standard parallel port mode
- PS/2 parallel port mode
- Parallel port FIFO mode
- ECP parallel port mode
- Centronix Peripheral mode (Vendor specified mode)

Other modes defined in the IEEE 1284 standard like test mode and configuration mode are also supported.

7.6 Frame Memory Reduction Module

The CODEC Module consists of two Compressors and Decompressors, and a pass-through function (Zero Compressor).

Input to the compressors and decompressors comes from the system memory through the DMA Module. The output is saved in a 64-byte FIFO. The output from the FIFO can be returned to memory (to a different location than the input) or sent to the Video Interface/RET Module to be printed, but not both at the same time.

All compressors and decompressors operate on 32-byte (8-word) blocks of input data. If there are fewer bytes of data, the input must be padded to a multiple of 32 bytes. A Byte Counter is provided to limit the output if the padding would otherwise result in extra bytes after the desired output.

The CODEC's generate two signals to the processor to signal completion of the operation. One of these, "*proc_done*", comes on when the CODEC is finished, but before the FIFO data has been transferred to memory or to the Video Interface. The other, "*done_all*",' comes on after *proc_done* when the FIFO becomes empty.

Much of the CODEC hardware is shared, so that only one compression or decompression can be in progress at a time.

7.6.1 Zero Compressor

The Zero Compressor copies the input to the output unchanged. It can be used to print data that has not been compressed.

7.6.2 Byte Compressor

This compressor is used for byte data, such as gray-scale images. It encodes the differences between bytes. It first computes the effectiveness of three types of differences for each 32-byte block. It then uses the method which results in maximum compression. If none of the three methods results in any compression, then the input data is copied to the output without compression. The encoding type is determined separately for each 32-byte block.

An SRAM, external to the W90100, must be provided to save one line of input data. The compressor uses this to form the difference between the current byte and bytes on the previous line.

The first scan line is treated differently, since there is no previous line with which to form differences. Instead, it uses an in-line difference and does not test to determine which encoding type would be best.

The maximum number of pixels (bytes) per line is determined by the size of the external SRAM. There are 16 address bits for the SRAM, so the maximum size is 65,535 bytes per line. The maximum number of output bytes is 16,777,215 bytes.

7.6.3 JBIG Compressor

The JBIG compressor is used for processing one-bit images. It implements the ISO/IEC IS 11544 specification, also published as ITU-T T.82.

The CODEC does not process the 20-byte JBIG header. If required, the header must be processed by the CPU. For encoding, the header must be prefixed to the CODEC output; when decoding, the header must be stripped from the decoder input.

The same SRAM described in 7.6.2 is also used for this compressor. The maximum image width is 65,535 pixels (8192 Bytes) per line, assuming an SRAM of at least this size. The maximum number of lines is 65,535.

7.7 Image Enhancement Module

7.7.1 Setup

Setup requirements consist of programming the control registers and downloading LUT (look_up_table) information into LUT memory. All internal register and memory locations can be read by the host CPU to check status and/or hardware integrity. In addition to the LUT memory and control registers, the Line Store memory can be written and read for testing. The memory map for the control registers and internal memories are:

Memory Map	From (PA15:0)	To (PA15:0)
Internal LUT (256 x 8)	0000	01FF
Control Registers (5 x 16)	0400	040F
Line Store Memory (4K x 16)	4000	5FFF

POWER-UP CONDITIONS:

Control Registers are powered up in their inactive state. In order to make any mode operational, specific values must be written to the control registers as well as the LUT's, which will be powered up in a random state.

LOOK-UP TABLES:

Look-up tables are required to be loaded by the CPU. Final tables will be provided after characterization on a sampling of representative engines.

LINE MEMORY SIZE:

Line store memory is organized as 4K words. This is segmented by the hardware architecture according to what operating mode is selected.

MODE	BUFFERS
600x600x1	8
300x300x1	16
200x200x1	16
200x100x1	16
1200x1200x1	4
600x600x8	NOT BUFFERED
300x300x8	1

7.7.2 Margin Offset Control:

Control register **C** contains the 11 bit register that sets the left-hand margin position of the image. The count will reflect the amount of 600dpi positions (1/600") from the selected edge of the beam detect (BD) signal, regardless of the mode selected.

7.7.3 Vertical Margin Control

The top of page detection is controlled by fsync_en (frame synch enable - control register **A,** bit 10) and frame sync, (fsynch). Fsync_en is set by software to begin a page (lsynch's will be ignored until the fsynch signal is received). When fsync_en is high we wait for fsynch to go high and then lsynch clocks will begin counting the vertical margin counter. When the vertical margin counter equals the vertical margin top register, (control register **E**) data transfer will begin. The vertical margin counter will continue to increment on each hysnc and when it reaches the value set in the vertical margin bottom register, (control register **F**) data transfer will terminate for the remainder of the page. The CPU is required to reset fsync_en after it has moved the all of the line data into the W90100 chip and allowed it to image that data. (one, two, or three additional lines depending on mode). The CPU will then set fsync_en again to prepare the fsynch logic for the next page synch signal, fsynch.

7.7.4 Input Ports

The data input is parallel, eight bit. Data is transferred into the design on the rising edge of the parallel video clock. The first clock after the hysnc signal will transfer the first eignt bits of data into the design.

7.7.5 Look-Up Table Memory (LUT):

To Load or Read the LUT memory the following bit in control register **A** must be set:

CPU2InternalLUT = Load LUT Memory (512x10)

Subsequent reading or writing to memory locations 0000-03FF will address the LUT memory, Data Bit 0 = LUT Bit 0. *What are LUT's for?* Look-up tables translate the fixed image values that are affected by engine linearity, temperature, aging, environmental, toner exhaustion, and other variables as well as features such as toner saver, paper type, type of input, etc. into values that will reproduce the highest quality image possible. The number of variables that influence the printed image are numerous and in order to correctly image the job these variables have to be compensated for. This is the job of the LUT memory..

7.7.6 OPERATING MODES

7.7.6.1 1200x1200x1

1200 Mode is selected by programming control register **A** bits [3:0] with a 1010. Source data must be in the two line format that can be used. The two line format requires that two lines of 1200 data must be transferred for each hysnc received by the design. The design will transfer two lines of sequential 1200 data per hysnc. The length of the lines is tracked via the line length register value (control register **D**, [11:0]) and when it reaches the programmed count it repeats the count for the second line. The CPU must program the line length (control register **D**) with the length of a single line of 1200 data into the Image Enhancement module.

To set up the W90100 for 1200 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	1010
Mfunction **(see table 2.0)**	[6:5}	XX
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Line Synch Width Register	[15:11}	0 - 1Fh
D: Line Length Register	[11:0]	0 - FFFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

7.7.6.2 600x600x1

600 Mode is selected by programming control register **A**,bits [3:0]. There are four different 600x1 operating modes to choose from. 0h is selected for enhanced text only, 1h is the test mode for 0h. 2h is for enhanced text and enhanced one bit gray scale. 3h is for unenhanced text and enhanced one bit gray scale. The CPU must program the line length (Control Register **D**) of a single line of 300 data into the Winbond chip.

To set up the Winbond chip for 600 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	0h, 1h, 2, 3h
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

7.7.6.3 300x300x1

300 Mode is selected by programming control register **A** bits [3:0]. There are two different 300x1 operating modes to choose from. 4h is selected for enhanced text only, 5h is the test mode for 4h.

To set up the W90100 chip for 300 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	4h, 5h
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh

F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

7.7.6.4 200xNx1

200 Mode is selected by programming control register **A** bits [3:0]. There are four different 200x1 operating modes to choose from. 6h is selected for enhanced text only, 7h is the test mode for 6h. 8h is selected for 200x100x1 enhanced text. 9h is the test mode for 8h.

To set up the Winbond chip for 200 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	6h, 7h, 8h, 9h
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

7.7.6.5 600x600x8

600x8 Mode is selected by programming control register **A** bits [3:0].

To set up the W90100 chip for 600x8 the LUT memory must be loaded and the following control registers must be programmed:

Control Register **A**	BITS	VALUE
Mode	[3:0]	Bh
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register **B**	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh

C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

7.7.6.5 300x300x8

300x8 Mode is selected by programming control register 'A' bits [3:0]. The CPU must program the line length (Control Register 'D') of a single line of 300 data into the Winbond chip.

To set up the Winbond chip for 300x8 Enhanced the LUT memory must be loaded and the following control registers must be programmed:

Control Register 'A'	BITS	VALUE
Mode	[3:0]	Ch
Mfunction **(see table 2.0)**	[6:5}	00
vidkill	7	1
bdedge (0 = rising edge, 1 = falling edge)	8	0 or 1
vidpol (0 = normal, 1 = inverse)	9	0 or 1
fsync_en (see paragraph for operational desc)	10	0 or 1
Unused	[12:11]	00
Other	4, 13, 14, 15	0,0,0,0

Control Register 'B'	BITS	VALUE
Unused	[15:0]	00h

Other Control Registers	BITS	VALUE
C: Horizontal Margin Register	[10:0]	0 - 3FFh
C: Unused	[15:11}	00000
D: Line Length Register	[10:0]	0 - 3FFh
D: Unused	[15:12]	0000
E: Vertical Margin (Top) Register	[15:0]	0 - FFFFh
F: Vertical Margin (Bottom) Register	[15:0]	0 - FFFFh

7.7.6.6 ONE BIT (600/300/200) TEST MODES

Test modes are different from normal one bit modes in that they bypass the Edge Enhancement Unit, (EEU). The input data is sampled just prior to the LUT memories. Selecting 600x600x1t, 600x600x1tg, 300x300x1t, 200x200x1t, or 200x100x1t one bit modes in register **A** will operate this way. The purpose of the test mode is to be able to bypass the EEU logic and present the assembled data directly to the modulator in order to isolate faults. Output will appear exactly like the input bit map.

8. Control and Status Register

8.1 CPU Registers

The W90100 CPU core implements all the registers needed for a Level 0 processor as defined in the PA-RISC specifications. Some registers or register bits are not needed in a Level 0 processor and are defined as nonexistent registers or register bits. The W90100 CPU implements three AIRs (Architecture Invisible Registers) that can be accessed by executing DIAG instructions.

8.1.1 General registers

Thirty-two 32-bit general registers provide the central resource for all computation. They are numbered GR 0 through GR 31, and are available to all program at all privilege levels. GR 0, when referenced as source operand, delivers zeros. When GR 0 is used as destination, the result is discarded. GR 1 is the target of the ADD IMMEDIATE LEFT instruction. GR 31 is the instruction address offset link register for the base relative interspace procedure call instruction. GR 1 and GR 31 can also be used as general register.

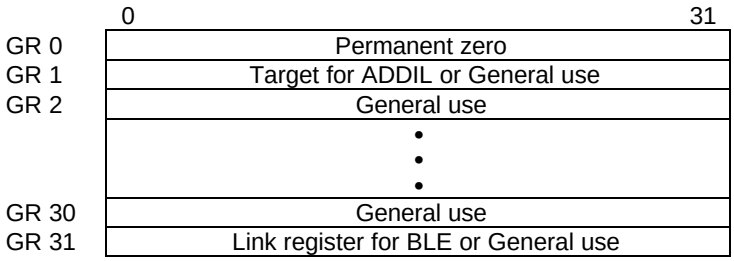


FIGURE 8.1 GENERAL REGISTERS

8.1.2 Shadow registers

W90100 CPU core provides seven registers called shadow registers as defined in the PA-RISC architecture. The contents of GR1,8,9,16,17,24 and 25 are copied upon interruptions. Shadow registers reduce the state save and restore time by eliminating the need for general register saves and restores in interruption handlers. The behavior of the shadow registers is described below.

Before entering interrupt routine: Contents of seven general registers are copied into shadow registers in one cycle.

When executing RFIR: Contents of shadow registers are copied into general registers automatically in one cycle.

8.1.3 Processor Status Word (PSW)

The processor state of W90K is encoded in a 32-bit register called the Processor Status Word (PSW). The format of PSW is shown in figure 8.2. The old value of the PSW is saved in the Interrupt Processor Status Word (IPSW) when interruption occurs. The PSW is set to the contents of the IPSW by the RFIR (RETURN FROM INTERRUPTION and RESTORE) instruction.

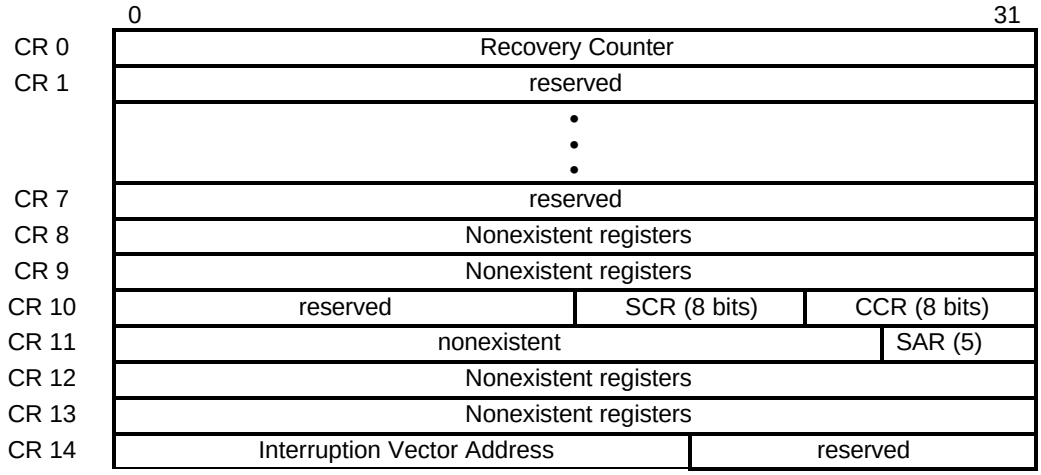
0	1	2 ... 4	5	6	7	8	9	10	11	12	13	14	15	16 ... 23	24	25	26	27	28	29	30	31
Y	Z	rv	E	S	T	H	L	N	X	B	C	V	M	C/B	rv	G	F	R	Q	P	D	I

Field	Description
rv	Reserved bits.
Y	Data debug trap disable.
Z	Instruction debug trap disable.
E	Little endian mode enable. When 1, all instruction fetches and loads/stores are little endian. The E bit after RESET is set according to the state of ENDIAN pin.
S	Secure Interval Timer. When 1, the Interval Timer is readable only by code executing at the most privileged level. When 0, the Interval Timer is readable by code executing at any privilege level.
T	Taken branch enable. When 1, any taken branch is terminated with a taken branch trap.
H	Higher-privilege transfer trap enable.
L	Lower-privilege transfer trap enable.
N	Nullify. The current instruction is nullified when this bit is 1.
X	Non-existent register bit.
B	Taken branch. The B-bit is set to 1 by any taken branch instruction and set to 0 otherwise.
C	Non-existent register bit.
V	Divide step correction. The integer primitive instruction records intermediate status in this bit to provide a non-restoring divide primitive.
M	High-priority machine check mask. When 1, High Priority Machine Checks (HPMCs) are masked. Normally 0, this bit is set to 1 after HPMC and set to 0 after all other interruptions.
C/B	Carry/borrow bits. These bits are updated by some instructions from the corresponding carry/borrow outputs of the 4-bit digit of the ALU.
G	Debug trap enable.
F	Non-existent register bit.
R	Recovery counter enable. When 1, recovery counter traps occur if bit 0 of the recovery counter is a 1. This bit also enables decrementing of the recovery counter.
Q	Interrupt state collection enable. When 1, interruption state is collected.
P	Non-existent register bit.
D	Non-existent register bit.
I	External interruption, power failure interrupt, and low-priority machine check interruption unmask. When 1, these interruptions are unmasked and can cause an interruption.

FIGURE 8.2 PROCESSOR STATUS WORD

8.1.4 Control registers

There are twenty-five control registers in W90100, numbered CR0, and CR8 through CR31, which contain system state information. Figure 8.3 shows the control registers. The access of CR 11, 16, 26, and 27 are described in the following table (table 8.4). Those control registers not listed in table 8.4 are only accessible by code executing at the most privileged level. Control registers 1 through 7 are reserved registers. The unused bits of the Coprocessor Configuration Register are reserved bits. The unused bits of the Shift Amount Register are nonexistent bits. In Level systems, CRs 8, 9, 12, 13, 17, and 20 are nonexistent registers.



CR 15	External Interrupt Enable Masks
CR 16	Interval Timer
CR 17	Nonexistent registers
CR 18	Interruption Instruction Address Offset Queue
CR 19	Interruption Instruction Register
CR 20	Nonexistent registers
CR 21	Interruption Offset Register
CR 22	Interruption Processor Status Word
CR 23	External Interrupt Request Register
CR 24	Temporary Registers
	• • •
CR 31	Temporary Registers

FIGURE 8.3 CONTROL REGISTERS

	Privilege level for the access
CR 11	read/write at any privilege level
CR 16	PSW 'S'=0: read/write by any privilege level PSW 'S'=1: read/write by privileged software
CR 26, 27	readable at any privilege level writable at the most privileged level
Others	Accessible only at most privileged level

TABLE 8.4 ACCESS OF CONTROL REGISTERS

8.1.5 W90100 External Interrupt Request register (EIRR; CR23)

Bit #	EI[0:4]	External Interrupt	Description
0	00000	Timer_INT	Interval Timer (CR16) Interrupt Request: the same as W90K
1	10000	-	
2	01000	-	
3	11000	PINTR	Special Interrupt Request : the same as W90K used by 8259 compatible interrupt controller
4	00100	INT1	DPI Bus INT1# Interrupt Request
5	10100	INT2	DPI Bus INT2# Interrupt Request
6	01100	-	
7	11100	-	
8	00010	PARINT-I	Parallel Port Interrupt Request 1 (ECP slave)
9	10010	SERINT	Serial Port Interrupt Request
10	01010	DMAINT	DMA Interrupt Request
11	11010	TINT	External Timer Internal Request
12	00110	PARINT-O	Parallel Port Interrupt Request 2 (ECP master)
13	10110	ENGINT1	Engine Interrupt Request 1 : Engine CMD/STS completion interrupt
14	01110	ENGINT2	Engine Interrupt Request 2 : Engine not ready interrupt
15	11110	CODECINT1	CODEC Interrupt Request 1 : Compress or decompress done
16	00001	CODECINT2	CODEC Interrupr Request 2 : data transfer completion
17	10001	-	
18	01001	-	
19	11001	-	
20	00101	-	
21	10101	-	
22	01101	-	
23	11101	-	
24	00011	-	
25	10011	-	
26	01011	-	
27	11011	-	
28	00111	-	
29	10111	-	
30	01111	-	
31	11111	-	

TABLE 8.5 EXTERNAL INTERRUPT REQUEST REGISTER

8.1.6 AIRs (Architecture Invisible Registers)

There are eight AIRs in the W90100. AIR[0] controls the internal cache configuration, burst mode, and default endian. AIR[0] is documented in this data sheet. AIR[1] and AIR[2] are reserved for chip testing by Winbond, and their functions will not be disclosed to users. Attempting to access these two registers may cause programs to be executed with unpredictable results. Memory configuration registers are used for programming the configuration of W90100 memory space. AIR[7] is the PCO register, this AIR can only be accessed through the JTAG ICE interface.

AIR[0]	Internal configuration register
AIR[1]	PSW register
AIR[2]	TMR register
AIR[3]	Memory configuration register 1
AIR[4]	Memory configuration register 2
AIR[5]	reserved
AIR[6]	reserved
AIR[7]	PCO register (program counter)

TABLE 8.6 W90100 CPU CORE AIRS

Important: Enabling or disabling the data cache will not change the contents of the data cache.

Disabling the internal D-cache with MTAIR[0] will cause dirty data to be left in the D-Cache and not automatically written into memory. When a program references the dirty data location, stale data in memory will be returned. To prevent this, a cache invalidation routine should be performed before the internal D-cache is disabled. The invalidation routine must flush all cache entries one by one. This will invalidate the cache and also write back any dirty data.

AIR[1] and AIR[2] are reserved registers and should never be written to or read from them. Accessing these registers will cause unpredictable result.

AIR[3] : Write_through base register & region size register
[0:15] Write_through region base register[0:15]
[16:19] system Non_cacheable region
0000 = all cacheable
0001 = above 1M
0010 = above 2M
0011 = above 4M
0100 = above 8M
0101 = above 16M
0110 = above 32M
0111 = above 64M
1000 = above 128M
1001 = above 256M
[20] address A0000 ~ FFFFF Non_cacheable
0 : Cacheable (default)
1 : Non_cacheable
[21:23] Non_cacheable region 1 size
[24:26] Non_cacheable region 2 size
000 = disable
001 = 64K
010 = 128K (the base address must be 128K boundry)
011 = 256K (the base address must be 258K boundry)
100 = 512K (the base address must be 512K boundry)
101 = 1M (the base address must be 1M boundry)
110 = 2M (the base address must be 2M boundry)
111 = 4M (the base address must be 4M boundry)

[27:29] Write_through region size
000 = disable
001 = 64K
010 = 128K (the base address must be 128K boundry)
011 = 256K (the base address must be 258K boundry)
100 = 512K (the base address must be 512K boundry)
101 = 1M (the base address must be 1M boundry)
110 = 2M (the base address must be 2M boundry)
111 = 4M (the base address must be 4M boundry)

AIR[4] : Non_cacheable Base register
[0:15] Non_cacheable region 1 base address[0:15]
[16:31] Non_cacheable region 2 base address[0:15]

8.2 Memory Controller Registers

The addresses of all the megacell registers in W90100 are defined by a base value plus an offset value. The base value is specified by the base register BASE[0:19], which is at the absolute address 0xF0000000. The default value of the BASE register is 0x00000000. The offset value [20:29] is defined by each megacell.

Memory controller register :

In Memory Controller, two IO ports are used to access the entire register set: the index port is at address **22h** and the data port is at address **23h**. To access a register, first write the index into the index port and then read or write the data through the data port.

8.2.1 DRAM controller registers

The DRAM controller can interface directly to the Fast Page Mode DRAM or EDO type DRAM. And there can be upto four banks of DRAM installed. The internal register for the DRAM controller is listed as follows:

Index	Bit No.	Description
20h	[0:7]	DRAM bank 0 base address register[0:7]
21h	[0:3]	DRAM bank 0 base address register[8:11]
22h	[0:7]	DRAM bank 1 base addressregister[0:7]
23h	[0:3]	DRAM bank 1 base address register[8:11]
24h	[0:7]	DRAM bank 2 base address register[0:7]
25h	[0:3]	DRAM bank 2 base address register[8:11]
26h	[0:7]	DRAM bank 3 base address register[0:7]
27h	[0:3]	DRAM bank 3 base address register[8:11]

The registers 20~27 has no default value.
Also, the base address must be set according to the bank size boundary value

28h	[0:7]	[0:1] DRAM bank 3 type : 00→ 256K, 01 → 1M, 10 → 4M, 11 → 16M, [2:3] DRAM bank 2 type : 00→ 256K, 01 → 1M, 10 → 4M, 11 → 16M, [4:5] DRAM bank 1 type : 00→ 256K, 01 → 1M, 10 → 4M, 11 → 16M, [6:7] DRAM bank 0 type : 00→ 256K, 01 → 1M, 10 → 4M, 11 → 16M, Default 256K type.
29h	[0:7]	[0] reserved(default 0) [1] Enable DRAM bank 3.(default 0) [2] Enable DRAM bank 2.(default 0) [3] Enable DRAM bank 1.(default 0) [4] Enable DRAM bank 0.(default 0) [5] Disable DRAM address range from A0000 to FFFFF.(default 0) [6] Fast write mode enable.(default 0) [7] EDO fast page mode enable.(default 0)
2ah	[0:7]	[0:1] RAS# precharge time.(default 0) [2] CAS# precharge time.(default 0) [3] Write cycle CAS# pulse width.(default 1) [4:5] Read cycle RAS# to CAS# delay.(default 'b01) [6:7] Write cycle RAS# to CAS# delay.(default 'b01)
2bh	[0:7]	[0:1] Refresh period. 00 : → 15us. (default). 01 : → 30us. 10 : → 60us. 11 : → disable refresh (for test only). [2] Refresh cycle. RAS# active pulse width after CAS# disactive. [3:4] Refresh cycle. RAS# active to CAS# inactive delay.(default 'b01) [5] Refresh cycle. CAS# active to RAS# active delay.(default 0) [6:7] Read cycle CAS# pulse width.(default 'b01)

TABLE 8.7 W90100 DRAM CONTROLLER REGISTERS

8.2.2 ROM controller registers

In Memory Controller, two IO ports are used to access the entire register set: the index port is at address **22h** and the data port is at address **23h**. To access a register, first write the index into the index port and then read or write the data through the data port.

The ROM controller can interface to either ROM or FLASH memory. Any write to ROM has no effect at all. The FLASH memory can be read or written through the control of ***oe***_ or ***we***_ signals. The internal register for the ROM controller is listed as follows:

ROM controller register :

Index	Bit No.	Description
00h	[0:7]	ROM bank 0 base address register[0:7]
01h	[0:7]	ROM bank 0 base address register[8:15]
02h	[0:7]	ROM bank 1 base address register[0:7]
03h	[0:7]	ROM bank 1 base address register[8:15]
04h	[0:7]	ROM bank 2 base address register[0:7]
05h	[0:7]	ROM bank 2 base address register[8:15]
06h	[0:7]	ROM bank 3 base address register[0:7]
07h	[0:7]	ROM bank 3 base address register[8:15] The register 0~7 has no default value.
08h	[0:7]	[0:3] ROM bank 0 size. [4:7] ROM bank 1 size.
09h	[0:7]	[0:3] ROM bank 2 size. [4:7] ROM bank 3 size. 0XXX → disable. 1000 → 64K, 1001 → 128K, 1010 → 256K, 1011→ 512K, 1100 → 1M, 1101 → 2M, 1110 → 4M, 1111 → 16M. The default value is 0.
0ah	[0:7]	[0:1] bank 3 band width: 00→ 8_bit, 01→ 16_bit, 10→ 32_bit, 11→ reserved [2:3] bank 2 band width: 00→ 8_bit, 01→ 16_bit, 10→ 32_bit, 11→ reserved [4:5] bank 1 band width: 00→ 8_bit, 01→ 16_bit, 10→ 32_bit, 11→ reserved [6:7] bank 0 band width: 00→ 8_bit, 01→ 16_bit, 10→ 32_bit, 11→ reserved The default width of bank 0~3 is set by memory data bus bit 30 and 31.
0bh	[0:7]	[0:2] ROM access wait state. 000 → wait 2 state. 001→ wait 3 state. 010 → wait 4 state. 011→ wait 5 state. 100 → wait 6 state. 101→ wait 7 state. 110 → wait 8 state. 111→ wait 9 state. The default wait state is 9. [3] access ROM bank0 only. Default bank0 only. [4] LA mode. Default LA mode.

TABLE 8.8 W90100 ROM CONTROLLER REGISTERS

8.2.3 DPI interface

The DPI interface can interface to Digital Product's expansion card. The Base register define the base address. Each segment is 128K. The address space from base+0 to base+ffffh is for the 64K memory on the expansion card. The address base+10000h and base+10001h are addresses for registers on the expansion card. The address above base+10002 is not used.

DPI interface register :

Index	Bit No.	Description
10h	[0:7]	Ext_BUS 1 base address register[0:7]
11h	[0:6]	Ext_BUS 1 base address register[8:14]
12h	[0:7]	Ext_BUS 2 base address register[0:7]
13h	[0:6]	Ext_BUS 2 base address register[8:14] The register 10~13 has no default value.
148h	[0:2]	[0] Ext_Bus card detect bit. 1: card exist, 0: card not exit. (read only) [1] Ext_Bus base address 1 enable. (default 0) [2] Ext_Bus base address 2 enable. (default 0)

TABLE 8.9 W90100 DPI INTERFACE CONTROLLER REGISTERS

8.3 DMA Controller (DMAC) Registers

Source Starting Address Register (SSAR0=200, SSAR1=210): SSAR is a read/write 32-bit register that contains the starting address of the DMA transfer source.

Target Starting Address Register (TSAR0=204, TSAR1=214): TSAR is a read/write 32-bit register that contains the starting address of the DMA transfer target.

Length/Count Register (LETH0=208, LETH1=218): LETH is a read/write 32-bit register that records the counts of current DMA transfer.

DMA Channel Mode Register (MODE0=20C, MODE1=21C): The MODE register specifies the operation mode of each channel.

The **Wait State Number** specifies the number of wait state needed for the particular DMA channel.

The **Recovery State Number** specifies the number of wait state needed for the recovery of the DMA channel.

The **channel terminal count flags** indicate that a DMA operation has stopped.

The **DMA channel enable bits** enable or suspend a DMA operation after a channel is set up. If a enable bit for a channel is cleared when a channel is active, the DMA will be suspended after pending requests for the channel are serviced. The DMA operation will resume normally when the bit is reset.

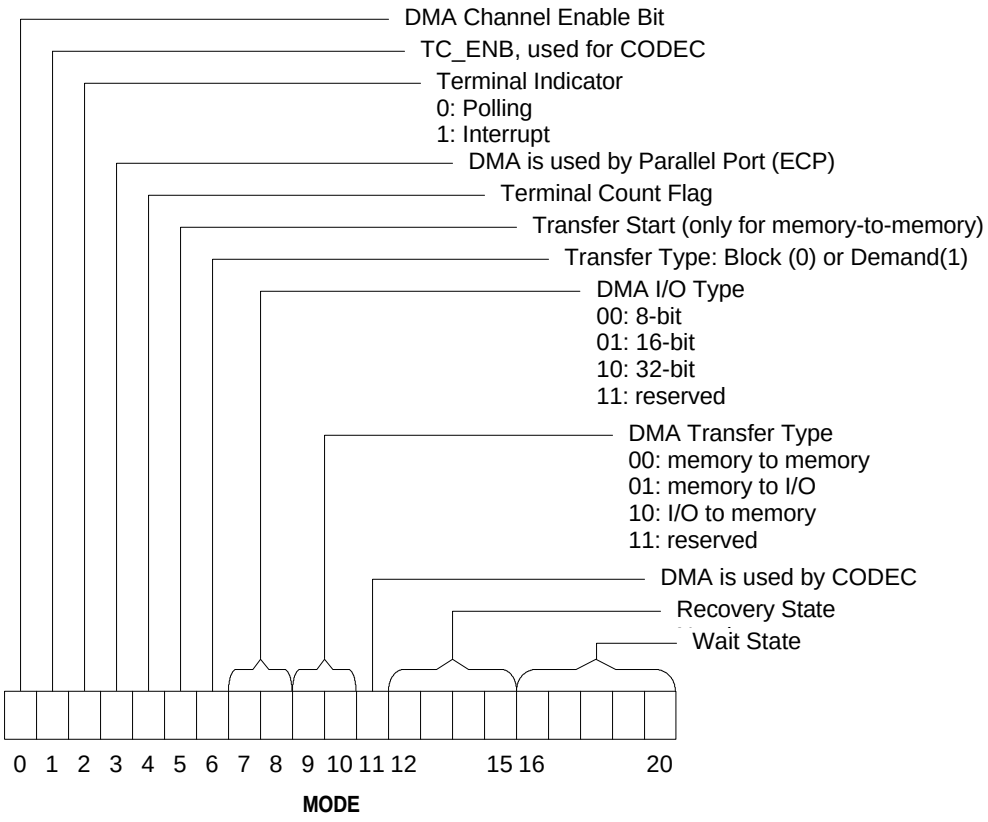
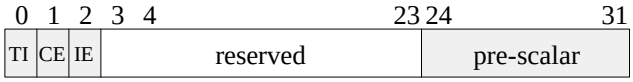


FIGURE 8.9 PROGRAMMING DMA CONTROLLER MODE REGISTER

8.4 Timer / Counter Registers

Each timer is controlled and initialized by two registers: a timer control register and an timer initial count register.

Timer Control register: TCR1 (40h), TCR2 (48h)



TCR

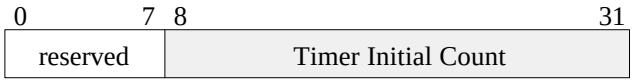
Pre-Scalar (PS): A pre-scalar value can be used to divide the input clock.

Interrupt Enable bit (IE): When IE is set to one and the counter decrements to zero, the timer asserts its interrupt signal to interrupt the CPU.

Counter Enable bit (CE): Setting the CE bit to one causes the timer to begin decrementing. Setting the CE bit to zero stops the timer.

Timer Interrupt bit (TI): The timer sets this bit to one to indicate that it has decrement to zero. This bit remain one until software sets it to zero.

Timer Initial Count Register: TICR1 (44h), TICR2(4ch)



TICR

A 24-bit read/write register for the initial counter value.

8.5 Serial I/O (UART) Register Definition

			Description
0	3F8, DLAB = 0	RBR[0:7]	- Receiver Buffer Register. - Read only. - bit 7 is LSB.
0	3F8, DLAB = 0	THR[0:7]	- Transmitter Holding Register. - Write only. - bit 7 is LSB.
1	3F9, DLAB = 0	IER[3:7]	- Interrupt Enable Register. * bit 7: Irpt_RDA enable (1/0- Enable/Disable). * bit 6: Irpt_THRE enable (1/0- Enable/Disable). * bit 5: Irpt_RLS enable (1/0- Enable/Disable). * bit 4: Irpt_MOS enable (1/0- Enable/Disable). - bit 3: Loop-back enable (1/0- Enable/Disable).
0	3F8, DLAB = 1	DLL[0:7]	* Divisor Latch Register (LS).
1	3F9, DLAB = 1	DLM[0:7]	* Divisor Latch Register (MS).
2	3FA	IIR[0:7]	- Interrupt Ident. Register. - Read only. * bit 7: No Irpt pending (1/0- True/False). * bit 6: Irpt ID bit (2). * bit 5: Irpt ID bit (1). * bit 4: Irpt ID bit (0). - bit 3: DMA mode select (1/0- Mode 1/Mode 0). - bit 2: RCVR trigger (LSB). - bit 1: RCVR trigger (MSB). - bit 0: FIFO mode enable (1/0- Enable/Disable).
2	3FA	FCR[0:7]	- FIFO Control Register. - Write only. * bit 7: FIFO mode enable (1/0- Enable/Disable). - bit 6: Reset RCVR FIFO. (self_clearing bit) - bit 5: Reset XMIT FIFO. (self_clearing bit) - bit 4: DMA mode select (1/0- Mode 1/Mode 0). - bit 3: (Reserve). - bit 2: (Reserve). * bit 1: RCVR trigger (LSB). * bit 0: RCVR trigger (MSB).
3	3FB	LCR[0:7]	- Line Control Register. * bit 7: Word length select (LSB). * bit 6: Word length select (MSB). - bit 5: Number of stop bit. - bit 4: Parity enable. (1/0- Enable/Disable) - bit 3: Even parity select. (1/0- Even/Odd parity) - bit 2: Stick parity enable. (1/0- Enable/Disable) - bit 1: Set break. - bit 0: Divisor Latch Access Bit (DLAB).

4	3FC	TOR[0:7]	- Time Out Register. - bit 7 ~ 1: Time out bit-count. - bit 0: Irpt_TOUT enable. (1/0- Enable/Disable)
5	3FD	LSR[0:7]	- Line Status Register. - Read only. - Write: Null operation. - bit 7: Data Ready (DR). - bit 6: Overrun Error (OE). - bit 5: Parity Error (PE). - bit 4: Framing Error (FE). - bit 3: Break Interrupt (BI). - bit 2: THR Empty (THRE). - bit 1: Transmitter Empty (TEMT). - bit 0: Error in RCVR FIFO (Err_RCVR).
6	3FE	MOS[0:7]	- MODEM Status Register: **non-exist** - Write: Null operation. - Read: Get 8'b0
7	3FF	SCR[0:7]	- Scratchpad Register. - Read/Write-able

TABLE 8.10 W90100 UART REGISTERS

Note: 1. Irpt_RDA: Received Data Available interrupt.
Irpt_THRE: Transmitter Holding Register Empty interrupt.
Irpt_RLS: Receiver Line Status Interrupt.
Irpt_MOS: MODEM Status Interrupt.
Irpt_TOUT: Receiver Time OUT Interrupt.

2. Baud rate = Frequency input / (16 * ({DLM, DLL} + 2))

3. Interrupt Identification:

IIR[4]	IIR[5]	IIR[6]	IIR[7]	**Priority**	**Irpt type**
-	-	-	1	-	None
0	0	0	0	4th	Irpt_MOS
0	0	1	0	3rd	Irpt_THRE
0	1	0	0	2nd	Irpt_RDA
1	1	0	0	2nd	Irpt_TOUT
0	1	1	0	1st	Irpt_RLS

* Irpt_RLS- caused by: Overrun Error or Parity Error or Framing Error or Break Interrupt.
- reset by: Reading LSR.
* Irpt_RDA- caused by: Received data >= RCVR trigger level.
- reset by: Reading RBR or RCVR FIFO drops below the trigger level.
* Irpt_TOUT- caused by: RCVR FIFO is non-empty and have not been accessed (Read/write) for the time >= TOUR[1:7].
- reset by: Reading RBR.
* Irpt_THRE- caused by: THRE has been set.
- reset by: Reading IIR (if source of INTR is Irpt_THRE) or writing THR.

* Irpt_MOS- MODEM Status interrupt: Non-implemented.

4. RCVR Interrupt trigger level programing:

FCR[0]	FCR[1]	**Trigger level**
0	0	1 bytes
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

5. FCR[7] is always 1. Write FCR[7] to 0 has no effect.

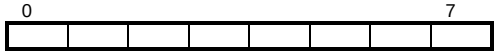
6. Transmitter/Receiver Character length programing:

LCR[6]	LCR[7]	**Character length**
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

8.6 IEEE 1284 Parallel Port

8.6.1 Parallel Port (Host Side) Register Definition

1. Data Register (offset 378) R/W



This is the standard parallel port data register. Writing to this register in Standard mode shall drive data to the parallel port data lines. In all other modes the drivers may be tri-stated by setting the direction bit in the dcr register. Read to this register return the value on the data lines.

Standard mode:

write data_reg: cpu_data[0:7]→ data_reg[0:7]→ PAD_ED[0:7]

read data_reg: data_reg[0:7]→ cpu_data

PS/2 mode, forward:

write data_reg: cpu_data→ data_reg → PAD_ED

read data_reg: data_reg→ cpu_data

PS/2 mode, reverse:

write data_reg: cpu_data→ data_reg

read data_reg: PAD_ED→ cpu_data

Centronix Peripheral mode:

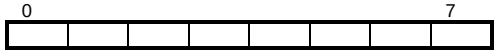
read data_reg: PAD_ED→ cpu_data

Other mode:

write data_reg: cpu_data[0:7]→ data_reg[0:7]

read data_reg: undefined

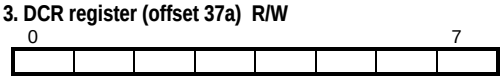
2. DSR register (offset 379) Read only



This read-only register reflects the inputs on the parallel port interface.

Bit [0]- nBusy: inverted parallel port **Busy** signal
Bit [1]- nAck: parallel port **nAck** signal
Bit [2]- PError: parallel port **PError** signal
Bit [3]- Select: parallel port **Select** signal
Bit [4]- nFault: parallel port **nFault** signal
Bit [5:7]- reserved

3. DCR register (offset 37a) R/W

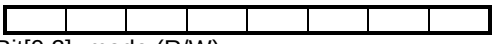


This register directly controls several output signals as well as enabling some functions. The drivers for nStrobe, nAutoFd, nInit, and nSelectIn are open-collector in standard mode.

Bit [0:1]- reserved
Bit [2]- Direction
0: forward (default)
Drivers are enabled.
1: reserved
In Standard mode or Parallel FIFO mode, this bit is forced to 0. The drivers are enabled, i.e. the data pins of the parallel port are always outputs. Otherwise, this bit tri-states the data output drivers, so that data will be read from the peripheral.
Bit [3]- ackIntEn
1: Enable an interrupt on the rising edge of nAck.
0: Disable the nAck interrupt (default)
Bit [4]- SelectIn; is inverted and then driven as parallel prot nSelectIn (default 1).
Bit [5]- nInit; is driven as parallel port nInit (default 1).
Bit [6]- autofd; is inverted and then driven as parallel port nAutoFd (default 0).
In centronic peripheral mode, when the nAck is active, the bit will be cleared by hardware.
Bit [7]- strobe; is inverted and then driven as parallel port nStrobe (default 0).

4. ECR register (offset 243) (R/W)

0 7



Bit[0:2]- mode (R/W)

000: Standard parallel port mode (default).
In this mode, FIFO is reset and common collector drivers are used on the control lines (nStrobe, nAutoFd, nInit, and nSelectIn). Direction bit is cleared to "0".

001: PS/2 parallel port mode
The direction could be forward or reverse. In reverse direction, reading the data register returns the value on the data lines not the value in the data register.

010: Parallel port FIFO mode
This is the same as Standard parallel port mode except that Pwords are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when the direction bit is 0.

011: ECP parallel port mode
In the forward direction, Pwords is placed into the FIFO and transmitted automatically to the peripheral using ECP protocol. In the reverse direction, bytes are moved from the ECP data port and packed into Pwords in the FIFO. All drivers have active pull-ups.

100: Centronic peripheral mode
In this mode, the parallel port acts as a reverse port in centronics mode and the direction bit is forced to 1. The nAutofd bit (DCR bit 6) is cleared, nAck is active until nAutofd bit (DCR bit 6) is set to 1 by software. And the parallel port data will be latched in the data register.

101: Reserved

110: Test mode
In this mode, the FIFO may be read or written, but the data will not be transmitted on the parallel port. Using this mode to test the depth of the FIFO, the write-threshold, and the read-threshold.

111: Configuration mode
In this mode, the CNFGA and CNFGB registers are accessible at addresses 244 and 246

Bit[3]- nErrIntrEn (R/W, Valid only in ECP mode)

1: Disable the interrupt generated on the asserting edge of nFault (default).

0: Enables an interrupt pulse on the high to low edge of nFault.

Note that an interrupt pulse will be generated if nFault is asserted and this bit is written from a "1" to a "0". This prevents interrupts from being lost in the time between the read of the ecr and the wrtie of the ecr.

Bit[4]- dmaEn (R/W)

1: Enables DMA, DMA starts when serviceIntr (bit 5) is 0.

0: Disables DMA unconditionally (default).

Bit[5]- serviceIntr (R/W)

1: Disables DMA and all of the service interrupts (default).

0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred, serviceIntr bit shall be set to a "1" by the hardware. Writing this bit to a "1" will not cause an interrupt.

case 1: dmaEn = 1
During DMA (this bit is set to a 1 when terminal count is reached)

case 2: dmaEn = 0, direction = 0
This bit shall be set to 1 whenever there are writeIntrThreshold or more Pwords free in the FIFO.

case 3: dmaEn = 0, direction = 1
This bit shall be set to 1 whenever there are readIntrThreshold or more valid Pwords to be read from FIFO.

Bit[6]- Full (Read only)

1: direction = 0 The FIFO cannot accept another Pword.

1: direction = 1 The FIFO is completely full.

0: direction = 0 The FIFO has at least 1 free Pword

0: direction = 1 The FIFO has at least 1 free byte.

Bit[7]- empty (Read only)

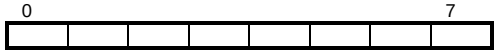
1: direction = 0 The FIFO is completely empty

1: direction = 1 The FIFO contains less than 1 Pword of data

0: direction = 0 The FIFO contains at least 1 byte of data

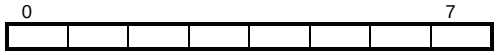
0: direction = 0 The FIFO contains at least 1 Pword of data

5. CONFIGA register (offset 244) (R/W only in configuration mode)



Bit [0]- Indicates if interrupts are pulsed or level (Read only)
0: pulse
1: level
Bit [1:3]- Pword size (R/W)
001: Pword size = 1 byte
010: Pword size = 4 byte
000 and 011 ~ 111: reserved
Bit [4]- reserved
Bit [5]- nByteInTransceiver (Read only)
0: When transmiting (at host recovery), there is one byte in the transceiver waiting to be transmitted that does not affect the FIFO full bit.
Bit [6:7]- Snapshot of the Pword
This field is not used for Pword size of 1 byte.
For host recovery situations these bits indicate what fraction of a Pword was not transmitted so that software can re-transmit the unsent bytes. If the Pword size is 4 bytes the value of these two bits is a snapshot of the last Pword being transmitted in mode 011 event 35 when the FIFO was reset (port was transitioned from mode 011 to mode 000 or 001)
00- the Pword at the head of the FIFO contained a complete Pword
01- the Pword at the head of the FIFO contained only 1 valid bytes.
10- the Pword at the head of the FIFO containeed 2 valid bytes.
11- the Pword at the head of the FIFO contained 3 valid bytes.

6. Reverse address register (offset 245) (Read only)



Bit [0:1]- Reserved
Bit [2]- Tag_all
1: To indicate the unread bytes of the FIFO storing the reverse data/ command that has at least one address bytes.
0: There is no address byte in the FIFO
Bit [3:6]- Tag0, Tag1, Tag2, Tag3
to check if there is one byte of the following read Pword = 4 bytes is the reverse address. Tag0, Tag1, Tag2 and Tag3 are individually for the byte0, byte1, byte2 and byte3 of the Pword
Bit [7]- Tag
to check if the byte of the following read Pword (1 byte) is the reverse address.

8.6.2 Parallel Port Interface controller (peripheral side)

(base : 0x370)

8	DL	- Data Lines.
		- Read/Write.
		- Exist only in BSTD mode.
		* bit [0:7] : Echo data line status.

Note : 1. Reading DL returns the value on the data-line but not the value in the data-register.

2. Writing DL drives the value directly into data-line.

9	DSRA	- Device Status Register A.
		- Read only.
		- bit 0 : Complement version of "nStrobe" pin.
		- bit 1 : Complement version of "nAutoFd" pin.
		- bit 2 : version of "nInit" pin.
		- bit 3 : Complement version of "nSelectIn" pin.
		- bit 4 : Device Fifo "full". (1/0 - True/False)
		- bit 5 : Device Fifo "empty". (1/0 - True/False)
		- bit [6:7] : reserved.
a	DCRA	- Device Control Register A.
		- Read/Write.
		- bit [0:1] : reserved.
		- bit 2 : Parallel Data port output enable. (1/0 - Enable/Disable)
		- bit 3 : state driving to "nFault" pin.
		- bit 4 : state driving to "Select" pin.
		- bit 5 : state driving to "PError" pin.
		- bit 6 : state driving to "nAck" pin.
		- bit 7 : inverted state driving to "Busy" pin.

Note : 1. The initial value of this register is 6'b1 which makes Busy pin = nAck pin = low.

2. Bit 2 : This bit has no effect in EPP mode.

b	DSRB	- Device Status Register B
		- Read only.
		- bit [0:4] : reserved.
		* bit [4:5] : Valid bytes in the Top PWord at the instanst of reverse "abort operation".
		* bit 6 : Device fifo over- or under-run. (1/0 - True/False)
		* bit 7 : ECP/EPP Command register pended. (1/0 - True/False)

Note : 1. Bit [4:5] = 00 : The TOP PWord contained a complete PWord.
01 : The TOP PWord contained 1 valid byte.
10 : The TOP PWord contained 2 valid byte.
11 : The TOP PWord contained 3 valid byte.

2. Bit 6 : This bit once be set, it will keep in set-state until the fifo is reseted.

2. Bit 7 : This bit once be set would prevent from the following parallel-port-interface access.
Read DSRB register would clear the bit.

c	DCRB	- Device Control Register B
		- Read/Write.
		* bit 0 : Dma mode enable (and request DMA). (1/0 - Enable/Disable)
		* bit 1 : Reset FIFO. (1/0 - Enable/Disable)
		* bit 2 : Reset Device. (1/0 - Enable/Disable)
		* bit [3:5] : Device mode select.
		* bit [6:7] : Fifo read-threshold.

Note : 1. Bit 0 : A low-to-high transistion in this bit will activate DREQ, and DREQ will be deasserted when DMAC reponses DACK. This bit will also be cleared by a DMA TC (terminal count).

2. Bit [1:2] : It is a self-clear bit. Writing a logical 1 will generate 1 SCLK period high "reset" signal.

3. Bit [3:5] = 000 : Bidirectional Standard Parallel Port Mode (SPP).
001 : Fast reverse Standard FIFO Mode (FSPP).
010 : ECP mode.
011 : EPP mode.
1xx : reserved

4. Bit [6:7] = 00 : Read Threshold = 16 byte
01 : Read Threshold = 12 byte
10 : Read Threshold = 8 byte
11 : Read Threshold = 1 byte (if PWord = 1 or 2 byte).
Read Threshold = 4 byte (if PWord = 4 byte).

d	DCRC	- Device Control Register C
		- Read/Write.
		* bit [0:1] : PWord size select.
		* bit 2 : "TC" interrupt enable. (1/0 - Enable/Disable)
		* bit 3 : "Address" interrupt enable. (1/0 - Enable/Disable)
		- bit 4 : "servIntr" interrupt enable. (1/0 - Enable/Disable)
		- bit 5 : "nSelectIn" interrupt enable. (1/0 - Enable/Disable)
		- bit 6 : "nInit" interrupt enable. (1/0 - Enable/Disable)
		- bit 7 : "nStrobe" interrupt enable. (1/0 - Enable/Disable)

Note : 1. Bit [0:1] = 00 : PWord = 8 bits.
01 : reserved (8 bits).
10 : PWord = 32 bits.
11 : reserved (8 bits).

---

e	IIR	- Interrupt Ident. Register.	
		- Read only .	
		* bit 2 : "TC" interrupt occurs.	(1/0 - True/False)
		* bit 3 : "Address" interrupt occurs.	(1/0 - True/False)
		* bit 4 : "servIntr" interrupt occurs.	(1/0 - True/False)
		* bit 5 : "nSelectIn" interrupt occurs.	(1/0 - True/False)
		* bit 6 : "nInit" interrupt occurs.	(1/0 - True/False)
		* bit 7 : "nStrobe" interrupt occurs.	(1/0 - True/False)

Note : 1. bit 2 : Irpt_TC will be set when TC is active, and will be clear when TC is reset (write a 0 into DMA mod_reg[4] will reset TC).

2. bit 3 : Irpt_Addr will happen only in receiver mode when PPI port receive Address(command) bytes.
And the interrupt will be cleared when CPU reads DSRB.

3. bit 4 : Irpt_SERV will occurs if DCRB[4]= 1 and
(1) if DCRA[2]=0 and Read-threshold is reached, under this condition, Irpt_SERV will keep high till the above condition is dismissed.
(2) if DCRA[2]=1 and the DFifo is from non-empty to empty status, a two system-clock-cycle Irpt_SERV will be issued.

4. bit 5 : Irpt_NSELI will occurs if DCRB[5]= 1 and a H-to-L or L-to-H transistion is activated on "nSelectIn".
And it will be cleared when CPU read DSRA.

5. bit 6 : Irpt_NINIT will occurs if DCRB[6]= 1 and a H-to-L or L-to-H transistion is activated on "nInit".
And it will be cleared when CPU read DSRA.

6. bit 7 : Irpt_NSTB will occurs if DCRB[7]= 1 and a H-to-L transistion is activated on "nStrobe".
And it will be cleared when CPU read DSRA.

---

f	DR	- Data Register.	
		- Read only. (optional)	
		* bit [0:7] : Data port input latch.	

Note : 1. Reading DR returns the value on the data-register but not the value in the data-line.
2. DR works only in forward transfer mode, and it latchs data-line's state

whenever "nStrobe" pin is from high-to-low.

0	DFifo	- Data Fifo. - Read/Write. - Host side's width is 8-bit and system side is PWord.
4	CMD	- Command register. - Write by PPI interface and Read by CPU. - bit [0:7] : Command code.
5	CNTR	- Device fifo counter. - Read only. (for test) - bit 0 : reserved. * bit 1 : Data Available (DA). (1/0 - True/False) * bit 2 : Space Available (SA). (1/0 - True/False) * bit [3:7] : Valid bytes in Dfifo.

Note : 1. Bit 1 : Device fifo contains at least 1 "PWord" data.

2. Bit 2 : Device fifo contains at least 1 "PWord" available space.

8.7 Frame Memory Reduction Module Registers

There are two control registers which must be loaded to operate any of the CODEC's: the Control Register and the Byte Count Register. Other registers are used depending on the compressor or decompressor selected. In addition, the DMA controller must be programmed to provide the input data, and to save the output data if the output is to be transferred to memory. If the output is to go to the Video Interface/RET, that module must be programmed as well.

The Control and Byte Count Registers are shown in Table 8.11. Both are Read/Write Registers.

NAME	OFFSET	FUNCTION			
CONTROL	1000	Unused	Reset	Destination	Select
SCAN LINE	1004	Unused	Scan Line Length		
BYTE COUNT	1008	Unused	Byte Count		

TABLE 8.11 CONTROL. SCAN LINE, AND BYTE COUNT REGISTERS

8.7.1 Control Register

8.7.1.1 Reset Bit

The Reset Bit is bit 27 in the Control Register. When set to ONE, the CODEC's are reset to their power on state (except for the Control Register.) This is intended to be used only to recover from a drastic error. For normal operation, this bit should always be ZERO.

8.7.1.2 Destination Bit

Bit 28 in the Control Register selects the destination of the CODEC output. When this bit is ZERO, output from the CODEC is transferred to memory. The DMA controller must be programmed for successful transfer. If this bit is ONE, the CODEC output goes to the Video Interface/RET; in this case the RET must be programmed for the desired function(s.)

8.7.1.3 Select Field

Bits 29 through 31 select the CODEC to be used as follows: (X = Don't Care)

SELECT FIELD	FUNCTION
0XX	None
100	Byte Compressor
101	Byte Decompressor
110	JBIG Compress/Decompress
111	Zero Compressor

When a CODEC completes its operation, it sets the proc_done signal and stops. In order to restart the same, or to start a different, CODEC, the CPU must first reset bit 29 of the Control Register, and secondly re-select a CODEC.

8.7.2 Byte Count Register

The Byte Count Register, shown in Table 8.11, is a 24-bit down-counter. It decrements as each byte is transferred from the CODEC to the FIFO. When the counter reaches ZERO, no more data is transferred to the FIFO. This counter must be loaded, before a CODEC is started, with a value at least as large as the number of output bytes.

When compressing data, the counter can be loaded with a large value. After compression, the counter can be read to determine the number of compressed bytes.

During decompression, the counter can be loaded with the expected number of output bytes to limit the output.

8.7.3 Scanline Length Register

The Scanline Length Register is required only for the CODEC. It contains 16 bits, and can be read or written by the CPU.

It should be loaded, before starting the CODEC, with the number of bytes on each line of the image, i.e., the number of pixels per line on the printed page. The value must be a multiple of 32 and must not be ZERO.

R	RW	BIT														
T		15	14	13	12	11	10	9	8	7	6	5	4	3	2	
	RW	Sdrst	Cx3Line	TpbOn	JStuff	JEncode	JDecode	ForceTx	JLimits		MSubX					
	RW	Reserved											CxClr	Resume	OutPort	
	RW	PixelsFld														
	RW	LinesFld														
	RW	StripeLinesFld														
	RW	Interval														
	RW	BaseLo														
	RW	BaseHi														
	RW	CodeSpace				FfStack										
	RW	Reserved				ZeroCnt										
	RW	Reserved								CodeBuf2						
	RW	RenShift				Line2	Line1	ZeroOvr	FfFmc	Dtauxh						
	R	Reserved										Error			Init	
	R	LpsInt														
	R	Reserve	MpsState							MpsSwt	LpsState					
	R	NewLinesFld														
FF	RW	State1							Mps1	State0						
FF	RW	RamData														

TABLE

8.7.4 JBIG Registers

The JBIG Registers are shown in Table 8.12. All registers contain 16-bits. Unused bits labeled "*reserved*" must be set to ZERO when written, and are indeterminate when read. Unless otherwise specified, all values are unsigned integers. Any restrictions on register values are noted below; violations of these restrictions result in undefined behavior, including lockup.

8.7.4.1 CtlJbig Register

MSubX: This field controls AT pixel movement during encoding and is ignored during decoding. If MSubX or ForceTx is ZERO, adaptive template pixel (AT) movement is disabled. Otherwise, the AT pixel will be positioned MSubX pixels to the left on the current line. MSubX corresponds to Mx in ISO IS 11544. The allowed values of MSubX depend on other fields as follows:

ForceTx	Cx3Line	MSubX
0	0	0
0	1	0
1	0	0, 5-127
1	1	0, 3-127

MSubX must be ZERO if encoder Speedmarks are being saved or restored and ForceTx = 0.

JLimits: This field limits the maximum allowed stacked 00 or FF bytes count during encoding. The limit field is encoded as follows:

JLimits Field	FF Limit
00	No Limit
01	127
10	15
11	1

If this limit is exceeded, then a sequence of 00 or FF bytes will be replaced in the output with a private FMC, which is the sequence of five bytes: FF, 01, 00 or FF, NN, NN, where NNNN is a two byte count. To create a valid JBIG coded output, these five bytes must be replaced with NNNN bytes of 00 or FF.

ForceTx: This field is used only during encoding. Setting ForceTx to ONE forces the AT pixel MSubX pixels to the left on the current line. The AT movement will be effected by output of the AT movement floating marker code (FMC) at the start of the image ' s first stripe, and no further movements will be allowed for the rest of the image. If ForceTx = 0, the AT pixel will move as described under the MSubX field.

JDecode: If this field is ONE, a decode operation is performed. The JDecode and JEncode must not both be ONE simultaneously.

JEncode: A ONE in this field enables an encode operation. The JDecode and JEncode must not both be ONE simultaneously.

JStuff: ISO IS 11544 requires that JBIG code streams place STUFF (00) bytes after any encoded image byte which is FF. Setting JStuff = 1 enables the addition of STUFF bytes during encoding, and removal of STUFF bytes during decoding. For JBIG coding, this field must be ONE.

TpbOn: Setting TpbOn = 1 enables the JBIG 'typical line prediction' feature. When enabled, an extra pseudo pixel is inserted at the start of each line to indicate if that line is identical to the previous line. The corresponds to the ISO IS 11544 variable TBPON.' This field must be the same when encoding and decoding to retrieve the original image.

Cx3Line: This field selects two (Cx3Line = 0) and three (Cx3Line = 1) line image templates for coding context generation. This field corresponds to the inverse of the ISO IS 11544 variable 'LRLTWO.' This field must be the same when encoding and decoding to retrieve the original image.

Sdrst: This field is used only during encoding. Setting this field to ONE causes the encoded stripes to be terminated with the SDRST sequence FF 03, and resets its coding state each stripe. Otherwise, stripes are terminated with FF 02 (SDNORM.)

8.7.4.2 CtlJbig2 Register

BmRest: This field must be ONE when restoring a Speedmark; otherwise it must be ZERO.

BmTake: This field must be ONE if a Speedmark will be taken after encoding; otherwise it must be ZERO.

OutPort: This field is unused.

Resume: Setting this field to ONE allows a decode operation to continue after taking a Speedmark.

CxClr: If this field is ONE, the encoder/decoder will clear CxRam to all ZERO's when it is enabled, before performing the operation. This requires about 512 clock cycles. This is required for any JBIG coding operation unless CxRam is initialized by the CPU.

8.7.4.3 Pixels Register

This register must be loaded with the number of pixels on an image line before a coding operation is initiated. It must not be ZERO. The maximum value is determined by the amount of external SRAM available, but cannot exceed 65535 bytes in any case.

8.7.4.4 Lines Register

This register must be loaded with the total number of lines in the image before a coding operation is initiated. It must not be ZERO. If a NEWLEN FMC has been received within a JBIG stream (as indicated by StatusJ6 register bit NewLen), then Lines will be reloaded with the FMC value, unless CtlJbig2-BmTake or CtlJbig2-BmRest is ONE.

8.7.4.5 NewLines Register

This register is valid only if StatusJ7-NewLen = 1. It is the number of lines from the NEWLEN FMC. This value should be used to replace the value found in the JBIG header.

8.7.4.6 StripeLines Register

This is the number of lines per JBIG stripe. If the number of image lines is not evenly divisible by StripeLines (including the case where one stripe is larger than the entire image), then the last stripe will contain less than StripeLine lines. This field corresponds to the ISO IS 11544 variable L0.

8.7.4.7 StatusJ0 Register

Interval: This is the ONE's complement of the JBIG interval register (ISO IS 11544 parameter A.) This is used for Speedmarks.

8.7.4.8 StatusJ1 Register

BaseLo: This is the ONE's complement of the lower 16 bits of the JBIG base register (unrenormalized version of ISO IS 11544 parameter CLOW.) This is used for Speedmarks.

8.7.4.9 StatusJ2 Register

BaseHi: This is the ONE's complement of the high order 16 bits of the JBIG base register (unrenormalized version of ISO IS 11544 parameter CHIGH.) This is used for Speedmarks.

8.7.4.10 StatusJ3 Register

FFStack: This is the ONE's complement of the JBIG FF stack counter (IOS IS 11544 parameter SC.) This is used for Speedmarks.

CodeSpace: This state is used for Speedmarks.

8.7.4.11 StatusJ4 Register

ZeroCnt: This is the ONE's complement of the JBIG 00 stack counter. This state is used for Speedmarks.

8.7.4.12 StatusJ5 Register

Codebuf2: This is the last code byte (not yet output) in the JBIG encoder pipeline. This is used for Speedmarks.

8.7.4.13 StatusJ6 Register

This register is provides status information after a coding operation for error checking and for Speedmarks.

TpLine: This field indicates the typical line status of the decoder. It is also used for Speedmarks.

Dtauxh: This field gives the AT pixel position during decode. It is also used for Speedmarks.

FFFmc: This field is set to ONE if a private FMC was inserted into the code during encoding. This feature is controlled by CtlJbig-JLimits (q.v..)

ZeroOver: This bit indicates an internal coder error.

Line1: This bit is set to ONE if the coder is coding the first image line. It is required for Speedmarks.

Line2: This bit is set to ONE if the coder is coding the first or second image line. It is required for Speedmarks.

RenShift: This field indicates the renormalization status of the JBIG base and interval registers. It is required for Speedmarks.

8.7.4.14 StatusJ7 Register

This read-only register is useful for testing, determining the status of operation on the current image, and for Speedmarks.

Done: This bit is set when the current operation is complete or has been terminated by an error. It is cleared when the JBIG coder is not selected.

NewLen: This bit is set if a NEWLEN FMC was received. If it is set, the Lines parameter may have been changed to give the new image length. If it is ZERO, the image size is left as programmed.

Init: This bit is set while CxRam is being initialized, and ZERO thereafter. CxRam access is prohibited when Init = 1.

Error: If DONE = 1 and this field is not ZERO, an error has occurred during processing. The possible error values are as follows:

ERROR	INTERPRETATION
0	No error
1	Private FMC
1	Invalid Escape Code
1	ABORT FMC
2	Non-zero AT FMC yAT
3	AT FMC Tx < 0
4	Non-zero AT FMC Ty
5	NEWLEN FMC Yd > 64K
6	Comment Ld > 64K
7	Missing End-of-Stripe

8.7.4.15 JRomHi Register

A state transition ROM is used to determine the information associated with a given coding state. This ROM data is made accessible for testing purposes via the registers JRomHi and JRomLo. Access to this data involves the following steps:

1. The CODEC must be deselected; see Section 8.7.1.3.

2. Either the JDecode or the JEncode bit, but not both, should be set in CtlJbig.

3. The State0 field in CxRam is must be loaded with the desired ROM address. The allowed addresses are 0-112 decimal.

4. Finally, the register is read to get the data.

LpsInt: This number is the next interval value when the less probable symbol is received. It corresponds to the ISO IS 115454 variable LSZ.

8.7.4.16 JRomLo Register

See section 8.5.7.15 on how to read this register.

LpsState: This field gives the next context state for renormalizations when the less probable symbol is received.

MpsSwitch: If this field is ONE, then the more probable symbol for a context is inverted if the less probable symbol is received. Otherwise, the more probable symbol remains unchanged.

MpsState: This is the next context state for renormalizations when the more probable symbol is received.

8.7.4.17 CxRam Register

The JBIG state context RAM contains 1024 bytes, one per context, organized as 512 16-bit words. Access to this RAM aids testing and Speedmarking.

Mps0: This field gives the more probable symbol for the given context.

State0: This identifies which of the 113 JBIG coding states is associated with the given context.

Mps1: This field gives the more probable symbol for the given context.

State1: This identifies which of the 113 JBIG coding states is associated with the given context.

8.7.4.18 ExtRam Register

The external SRAM can be read or written through these registers. The maximum SRAM size is 65,536 bytes. The SRAM can be accessed only when the JBIG module is selected (see Section 8.7.1.3).

RamData: This is the data at the currently addresses SRAM location.

8.8 Image Enhancement Module Registers

Control Registers for RET module. Address starting from 0xF0100000

8.8.1 Memory Map for RET module

Memory Map	From (PA15:0)	To (PA15:0)
Internal LUT (256 x 8)	0000	01FF(03FF)
Control Registers (5 x 16)	0400	040F(04FF)
Line Store Memory (4K x 16)	4000	5FFF(7FFF)

8.8.2 Control Register A (address = 0400)

15 (MSB)	cpu2lsm	To enable CPU to access the line store memory
14	reserved	
13	cpu2ilut	To enable CPU to access the internal LUT
12	*reserved*	!c_adj_lb, should be 0
11	*reserved*	!w_adj_lb, should be 0
10	fsync_en	The top of page detection is controlled by fsync_en and fsync. fsync_en goes high by software to tell us to look for the fsync from the engine. Must go low after a page to reset circuit that looks for page start.
9	vidpol	video polarity, connected to modulator/video_pol
8	bdedge	bd edge sensitiviity, connected to modulator/bdedge or BD_pol_sel
7	vidkill	video kill, connedted to modulator/video_kill or viden
6	black	
5	force	
4	*reserved*	
3	mode control bit 3	
2	mode control bit 2	
1	mode control bit 1	
0 (LSB)	mode control bit 0	

TABLE 8.11 RET CONTROL REGISTER A

Unused bits labeled"***reserved***" must be set to**ZERO** when written.

Mode	Mode control bits [3:0]	Description
m600x1e	0000	Mode 600x1 edge enhancement
m600x1t	0001	Mode 600x1 test
m600x1eg	0010	Mode 600x1 edge enhancement & 1-bit grayscale
m600x1tg	0011	Mode 600x1 1-bit grayscale
m300x1e	0100	Mode 300x1 edge enhancement
m300x1t	0101	Mode 300x1 test
m200x1e	0110	Mode 200x1 edge enhancement
m200x1t	0111	Mode 200x1 test
m100x1e	1000	Mode 100x1 edge enhancement
m100x1t	1001	Mode 100x1 test
m1200x1	1010	Mode 1200
m600x8	1011	Mode 600x8
m300x8	1100	Mode 300x8

TABLE 8.12 RET MODE CONTROL BITS

8.8.3 Control Register B (address = 0402)

15 - 0	Reserved	

TABLE 8.13 RET CONTROL REGISTER B

8.8.4 Control Register C (address = 0404)

15 - 11	Unused	
10 - 0	HMargin	Horizontal Margin, count of engine clocks to delay the start of the line

TABLE 8.14 RET CONTROL REGISTER C

8.8.5 Control Register D (address = 0406)

15 - 12	Unused	
11 - 0	LineLength	Line Length Count, number of source pixel in a line

TABLE 8.15 RET CONTROL REGISTER D

8.8.6 Control Register E (address = 0408)

15 - 0	VMarginTop	Vertical Top Margin, in lines

TABLE 8.16 RET CONTROL REGISTER E

8.8.7 Control Register F (address = 040A)

15 - 0	VMarginBottom	Vertical Bottom Margin, in lines

TABLE 8.17 RET CONTROL REGISTER F

8.8.8 Control Register G (address = 040C)

15 - 0	C_Adj	Reserved for C Adjustment value of modulaltor

TABLE 8.18 RET CONTROL REGISTER G

8.8.9 Control Register H (address = 040E)

15 - 0	W_Adj	Reserved for W Adjustment vaule ofmodulator

TABLE 8.19 RET CONTROL REGISTER H

8.9 Video Interface Command/Status Registers

8.9.1 Control Register IO1 (offset = 0300)

0 (MSB)	FSYNC_POL	FSYNC_ polarity control. 0: low active. 1: high active, or reverse the polarity of the FSYNC_ input.
1	FSYNC_SEL	FSYNC_ input/output control. 0: input. 1: output.
2	LSYNC_POL	LSYNC_ polarity control. 0: no reverse 1: reverse the polarity of the LSYNC_ input.
3	SRDY_SEL	CCLK_/SRDY_ select. 0: select CCLK_ for NEC or CANNON engine. 1: select SRDY_ for SHARP engine.
4	CBSY_SEL	CBSY_ select. 0: CBSY_ output for NEC engine. 1: CBSY_ output for SHARP engine.
5	PRINT_POL	PRNT_ polarity control. 0: low active. 1: high active.
6	CMD_DIR	CMD/STS i/o signal direction control. When CMD/STS is programmed as bidirectional I/O, the direction is controlled by CBSY_ and SBSY_. 0: bidirectional I/O. 1: output.
7(LSB)	CCLK_DIR	CCLK_ command clock direction control. 0: bidirectional. 1: output.

TABLE 8.20 VIDEO INTERFACE CONTROL REGISTER IO1

8.9.2 Control Register IO2 (offset = 0301)

0(MSB)	reserved	
1	reserved	
2	reserved	
3	reserved	
4	reserved	
5	reserved	
6	CS_IEN	CMD/STS completion interrupt enable bit. 0: disable. 1: enable.
7(LSB)	Eng_IEN	Engine NOT ready interrupt enable bit. 0: disable. 1: enable.

TABLE 8.21 VIDEO INTERFACE CONTROL REGISTER IO2

8.9.3 Engine Command Register (offset = 0304)

0-7	ECM	Command to printer engine

TABLE 8.22 ENGINE COMMAND REGISTER

8.9.4 Engine Status Register (offset = 0305)

0-7	EST	Status from printer engine

TABLE 8.23 ENGINE STATUS REGISTER

8.9.5 Control Register IO6 (offset = 0307)

0-3	reserved	

4	CS_TYPE	select Mita or NEC command/status protocol 0: NEC. 1: Mita.
5	RDY_POL	Engine RDY_ polarity. 0: low for engine ready. 1: high for engine ready.
6-7	CCLK_DIV	CCLK_ output clock select. 00: PCLK/128. 01: PCLK/64. 10: PCLK/32. 11: PCLK/16.

TABLE 8.24 CONTROL REGISTER IO6

8.9.6 Control Register IO7 (offset = 0308)

0-6	reserved	
7	PRNT_	Set this bit will generate PRNT_ for NEC and CANNON egines, or PAGE_ for SHARP engine

TABLE 8.25 CONTROL REGISTER IO7

8.9.7 Control Register IO8 (offset = 0309)

0-3	reserved	
4	RDY_FLAG	Engine ready flag (read only) 0: engine ready. 1: engine not ready.
5	SBSY_/CRDY_	SBSY_/CRDY_. SBSY_: used by NEC or CANNON engines, 0: active low for receiving engine status. CRDY_: used by SHARP engine; 0: ready for receiving command from controller
6	CMD_COMP	command completion flag.
7	STS_COMP	status completion flag

TABLE 8.26 CONTROL REGISTER IO8

8.9.8 Control Register IO9 (offset = 030a)

0-5	reserved	
6	SRDY_	SRDY_ for SHARP engine
7	CBSY_	CBSY_ for SHARP engine

TABLE 8.27 CONTROL REGISTER IO9

8.10 Parallel I/O Interface

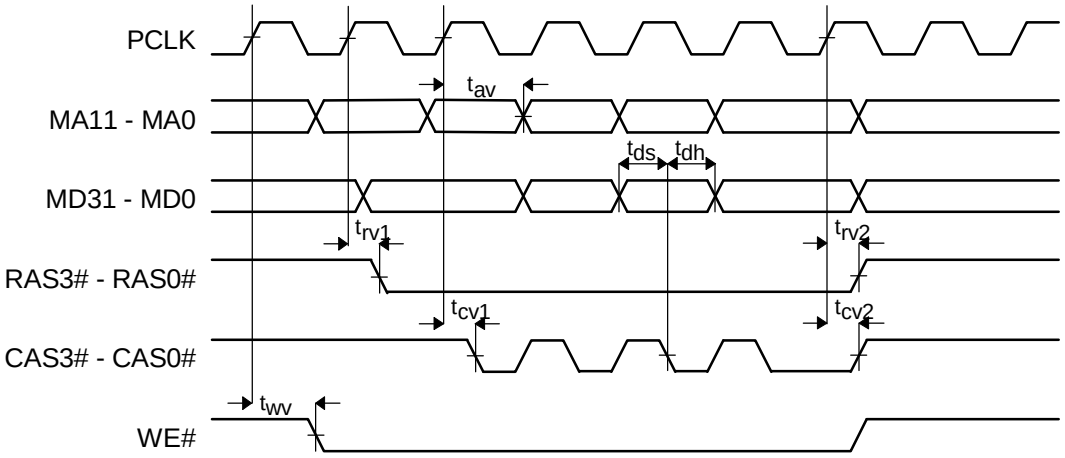
There are four registers in the PIO megacell.

Name	I/O Address	Description
PINV	F0000050	PIO polarity control register PINV[0:7] control the input/output polarity of each bit in PIO[0:7]. 0:non-inverted; 1:inverted.
PIN	F0000054	PIO input register
POUT	F0000058	PIO output register
POEN	F000005C	PIO output enable register POEN[0:7] specify the I/O direction of each PIO bit individually. 0:input; 1:output.

Due to the endian difference between the CPU core and the PIO megacell, the PIO megacell must be accessed in WORD (32-bit) mode.

9. Timing Diagram

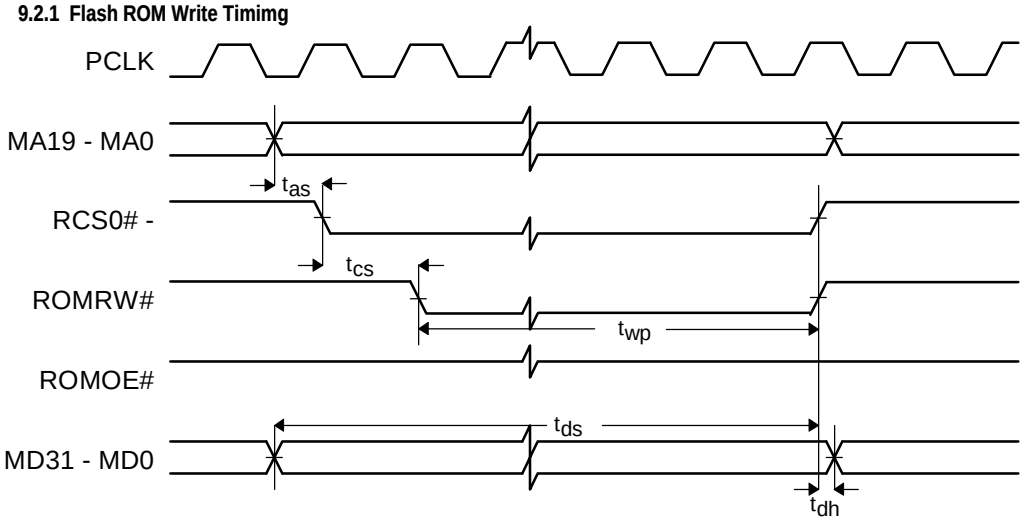
9.1 DRAM AC Timimg



Symbol	Parameter	Min	Max	Unit
t_{rv1}	RAS# valid delay ref. to PCLK rising			ns
t_{rv2}	RAS# valid delay ref. to PCLK rising			ns
t_{cv1}	CAS# valid delay ref. to PCLK rising			ns
t_{cv2}	RAS# valid delay ref. to PCLK rising			ns
t_{wv}	WE# valid delay ref. to PCLK rising			ns
t_{ds}	Memory data setup time			ns
t_{dh}	Memory data hold time			ns
t_{av}	Memory address valid delay			ns

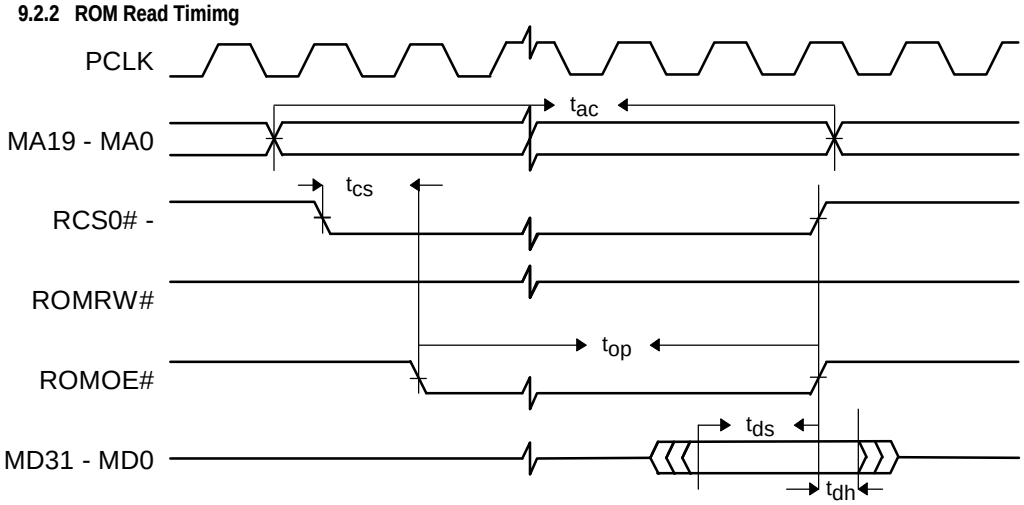
9.2 ROM AC Timimg

9.2.1 Flash ROM Write Timimg



Symbol	Parameter	Min	Max	Unit
t_{as}	Address setup time			ns
t_{cs}	Chip select setup time			ns
t_{ds}	Data setup time			ns
t_{dh}	Data hold time			ns
t_{wp}	Flash ROM write pulse width		7	PCLK

9.2.2 ROM Read Timimg

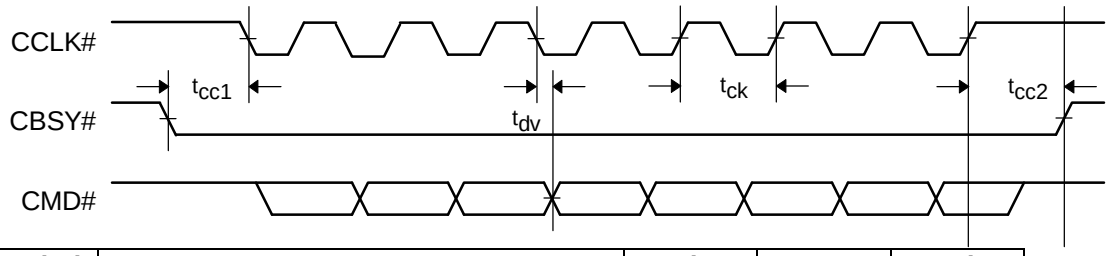


Symbol	Parameter	Min	Max	Unit
t_{ac}	Access time	3		PCLK
t_{cs}	Chip select setup tome			ns
t_{op}	Output enable pulse			ns
t_{ds}	Data setup tome			ns

t_{dh}	Data hold time			ns

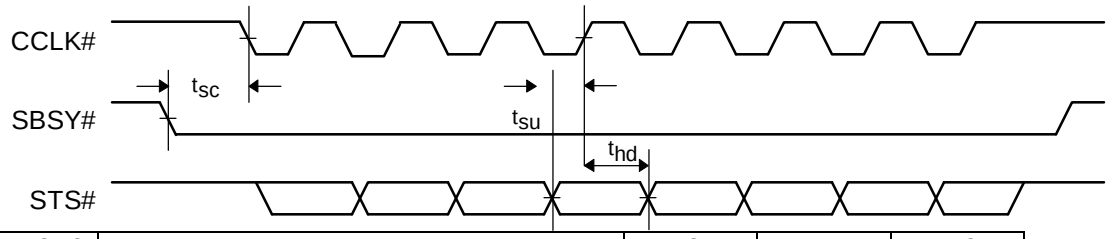
9.3 Print Engine AC Timing

9.3.1 Engine Command AC Timing



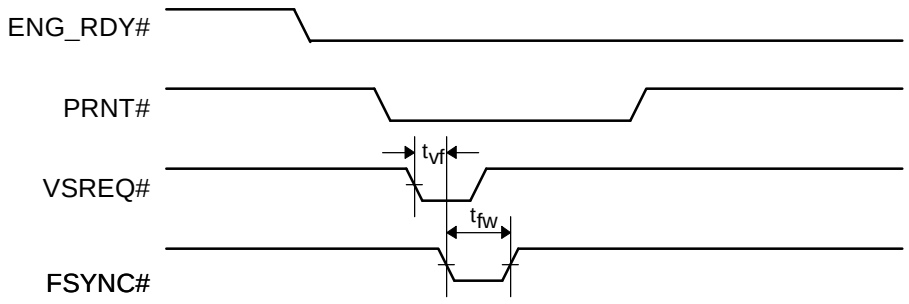
Symbol	Parameter	Min	Max	Unit
t_{ck}	CCLK# period	32	4096	PCLK
t_{cc1}	CCLK# asserted ref. to CBSY# falling	1	5	CCLK#
t_{cc2}	CBSY# deasserted ref. to last CCLK# rising	1	5	CCLK#
t_{dv}	CMD# valid delay ref. to CCLK# falling			ns

9.3.2 Engine Status AC Timing



Symbol	Parameter	Min	Max	Unit
t_{sc}	CCLK# asserted ref. to SBSY# falling	1	6	CCLK#
t_{su}	STS# setup time ref. to CCLK# rising			ns
t_{hd}	STS# hold time ref. to CCLK# rising			ns

9.4 Video Interface AC Timing



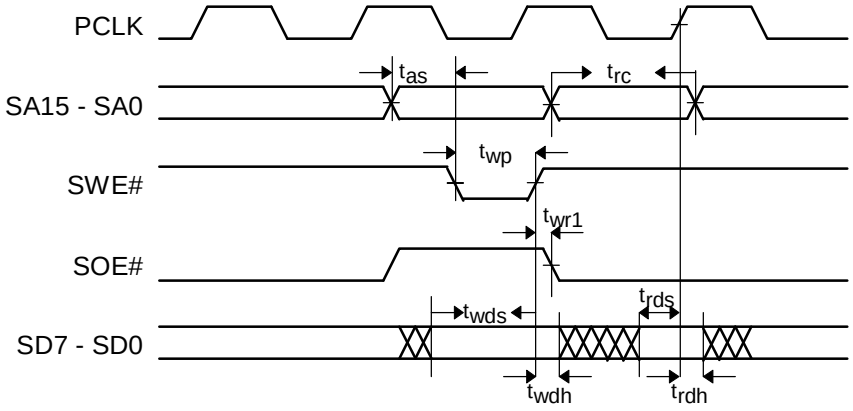
Note: Set FSYNC# as output

Symbol	Parameter	Min	Max	Unit

t_{vf}	assert FSYNC# ref. to VSREQ# falling		1	LSYNC#
t_{fw}	FSYNC# active period		1	LSYNC#

9.5 Sram AC Timing

9.5.1 Sram Write Timing



Symbol	Parameter	Min	Max	Unit
t_{as}	Address setup time			ns
t_{wp}	Write pulse width		1/2	PCLK
t_{rc}	Read Cycle Time		1	PCLK
t_{wds}	Write data setup tome			ns
t_{wdh}	Write data hold time			ns
t_{rds}	Read data setup time ref. to PCLK			ns
t_{rdh}	Read data hold time ref. to PCLK			ns
t_{wr1}	Write recovery time			ns

CORPORATE HEADQUARTERS:

NO. 4, Creation Rd. III

Science-Based Industrial Park

Hsinchu, Taiwan, R.O.C.

TEL: 886-35-770066

FAX: 886-35-789467

INFORMATION CONTACTS:

Rongken Yang

Special Product Design Dept. I

TEL: 886-35-792632

E-mail: rkyang@winbond.com.tw

Note: All data and specifications are subject to change without notice.