

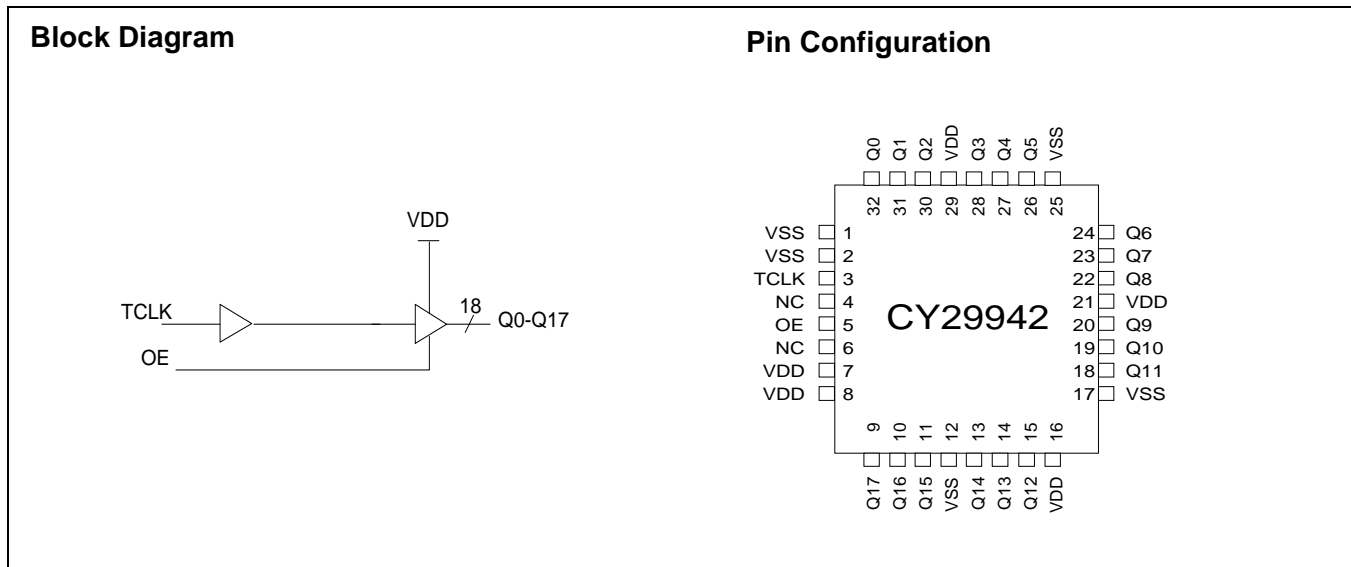


#### Features

- 200-MHz clock support
- 2.5V or 3.3V operation
- LVC MOS/LVTTL clock input
- LVC MOS-/LVTTL-compatible inputs
- 18 clock outputs: drive up to 36 clock lines
- 200 ps max. output-to-output skew
- Output Enable control
- Pin compatible with MPC942C
- Available in Industrial and Commercial
- 32-pin LQFP package

#### Description

The CY29942 is a low-voltage 200-MHz clock distribution buffer with an LVC MOS or LVTTL compatible input clock. All other control inputs are LVC MOS/LVTTL compatible. The eighteen outputs are 2.5V or 3.3V LVC MOS or LVTTL compatible and can drive 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the devices an effective fanout of 1:36. Low output-to-output skews make the CY29942 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.



**Pin Description<sup>[1]</sup>**

Pin	Name	PWR	I/O	Description
3	TCLK		I, PD	<b>External Reference/Test Clock Input</b>
5	OE		I, PU	<b>Output Enable.</b> When HIGH, all the outputs are enabled. When set LOW, the outputs are at high impedance.
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDD	O	<b>Clock Outputs</b>
7, 8, 16, 21, 29	VDD			<b>3.3V or 2.5V Power Supply</b>
1, 2, 12, 17, 25	VSS			<b>Common Ground</b>
4, 6	NC			<b>No Connection</b>

**Note:**

1. PD = Internal Pull-Down, PU = Internal Pull-up.

**Maximum Ratings<sup>[2]</sup>**

Maximum Input Voltage Relative to  $V_{SS}$ : .....  $V_{SS} - 0.3V$   
 Maximum Input Voltage Relative to  $V_{DD}$ : .....  $V_{DD} + 0.3V$   
 Storage Temperature: .....  $-65^{\circ}C$  to  $+150^{\circ}C$   
 Operating Temperature: .....  $-40^{\circ}C$  to  $+85^{\circ}C$   
 Maximum ESD protection ..... 2 kV  
 Maximum Power Supply: ..... 5.5V  
 Maximum Input Current: .....  $\pm 20$  mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either  $V_{SS}$  or  $V_{DD}$ ).

**DC Parameters:**  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ , Over the specified temperature range.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input Low Voltage		$V_{SS}$		0.8	V
$V_{IH}$	Input High Voltage		2.0		$V_{DD}$	V
$I_{IL}$	Input Low Current <sup>[3]</sup>				-200	$\mu A$
$I_{IH}$	Input High Current <sup>[3]</sup>				200	$\mu A$
$V_{OL}$	Output Low Voltage <sup>[4]</sup>	$I_{OL} = 20$ mA			0.5	V
$V_{OH}$	Output High Voltage <sup>[4]</sup>	$I_{OH} = -20$ mA, $V_{DDC} = 3.3V$	2.4			V
		$I_{OH} = -16$ mA, $V_{DDC} = 2.5V$	2.0			
$I_{DDQ}$	Quiescent Supply Current			5	7	mA
$I_{DD}$	Dynamic Supply Current	$V_{DD} = 3.3V$ , Outputs @ 150 MHz, $CL = 15$ pF		285		mA
		$V_{DD} = 3.3V$ , Outputs @ 200 MHz, $CL = 15$ pF		335		
		$V_{DD} = 2.5V$ , Outputs @ 150 MHz, $CL = 15$ pF		200		
		$V_{DD} = 2.5V$ , Outputs @ 200 MHz, $CL = 15$ pF		240		
$Z_{out}$	Output Impedance	$V_{DD} = 3.3V$	8	12	16	$\Omega$
		$V_{DD} = 2.5V$	10	15	20	
$C_{in}$	Input Capacitance			4		pF

**Notes:**

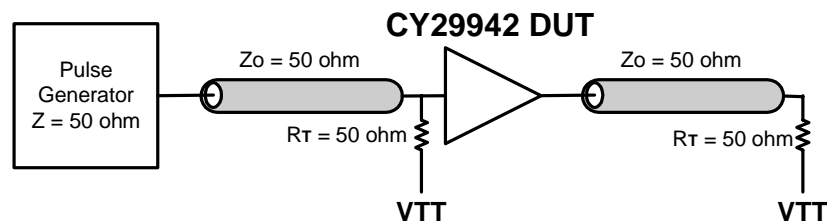
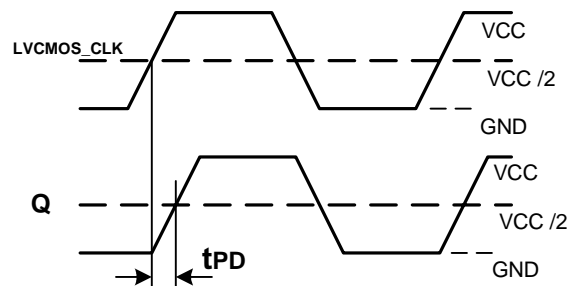
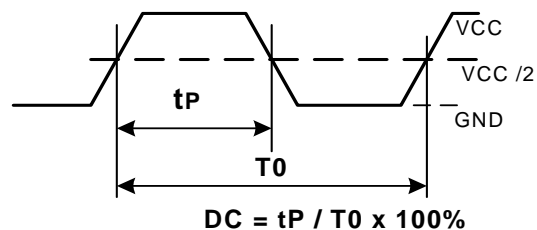
- Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- Inputs have pull-up/pull-down resistors that effect input current.
- Driving series or parallel terminated 50 $\Omega$  (or 50 $\Omega$  to  $V_{DD}/2$ ) transmission lines.

**AC Parameters**<sup>[5]</sup>:  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DCC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ , Over the specified temperature range

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Fmax	Input Frequency				200	MHz
Tpd	TTL_CLK to Q Delay <sup>[6, 7]</sup>	$V_{DD} = 3.3V$	1.8	3.3	3.8	ns
		$V_{DD} = 2.5V$	2.3	3.8	4.4	
FoutDC	Output Duty Cycle <sup>[6, 7, 8]</sup>	Measured at $V_{DD}/2$	45		55	%
Tskew	Output-to-Output Skew <sup>[6, 7]</sup>				200	ps
Tskew(pp)	Part-to-Part Skew <sup>[9]</sup>	$V_{DD} = 3.3V$			1.0	ns
		$V_{DD} = 2.5V$			1.3	
Tskew(pp)	Part-to-Part Skew <sup>[10]</sup>				600	ps
Tr/Tf	Output Clocks Rise/Fall Time <sup>[6, 7]</sup>	0.8V to 2.0V, $V_{DD} = 3.3V$	0.2		1.1	ns
		0.5V to 1.8V, $V_{DD} = 2.5V$				

**Notes:**

5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving 50Ω transmission lines.
7. See Figure 1.
8. 50% input duty cycle.
9. Across temperature and voltage range, includes output skew.
10. For a specific temperature and voltage, includes output skew.


**Figure 1. LVC MOS\_CLK CY29942 Test Reference for  $V_{CC} = 3.3V$  and  $V_{CC} = 2.5V$** 

**Figure 2. LVC MOS Propagation Delay (TPD) Test Reference**

**Figure 3. Output Duty Cycle (FoutDC)**

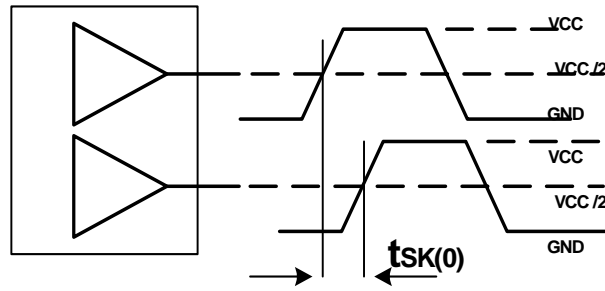
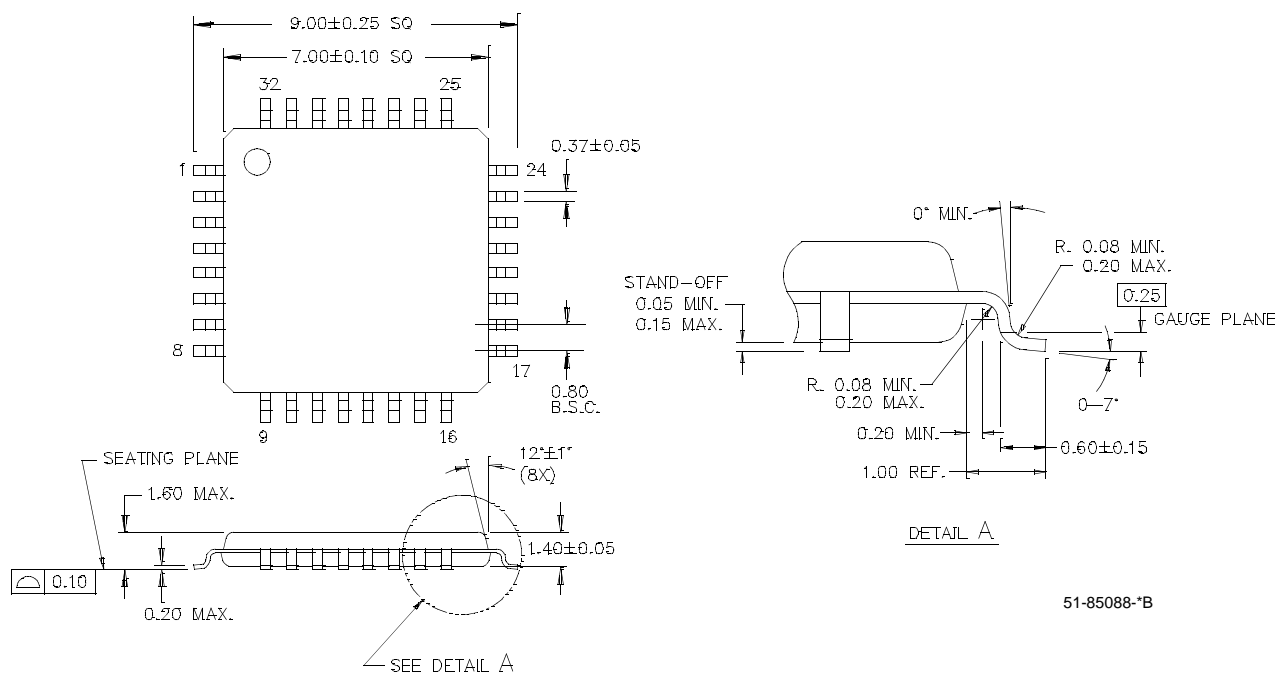


Figure 4. Output-to-Output Skew  $t_{SK}(0)$

**Ordering Information**

Part Number	Package Type	Production Flow
CY29942AI	32 Pin LQFP	Industrial, -40°C to +85°C
CY29942AIT	32 Pin LQFP - Tape and Reel	Industrial, -40°C to +85°C
CY29942AC	32 Pin LQFP	Commercial, 0°C to +70°C
CY29942ACT	32 Pin LQFP - Tape and Reel	Commercial, 0°C to +70°C

**Package Drawing and Dimensions**
**32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14**


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**Revision History**

<b>Document Title: CY29942 2.5V or 3.3V, 200-MHz, 1:18 Clock Distribution Buffer</b>				
<b>Document Number: 38-07284</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	111095	02/07/02	BRK	New data sheet
*A	116777	08/14/02	HWT	Added a Commercial Temp. Range in the Ordering Information
*B	122876	12/21/02	RBI	Add power up requirements to maximum rating information.