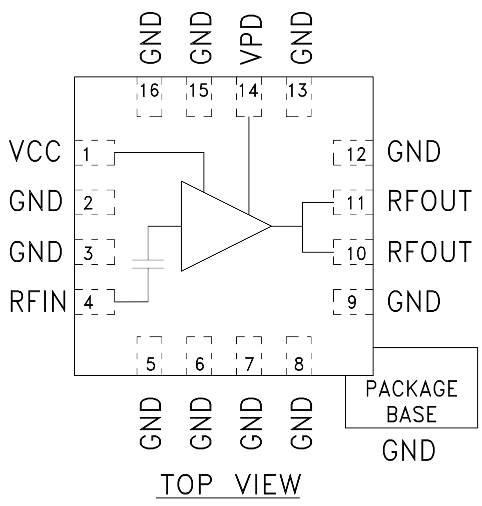
GaAs InGaP HBT MMIC POWER AMPLIFIER, 4.9 - 5.9 GHz

Typical Applications

This amplifier is ideal for use as a power amplifier for 4.9 - 5.9 GHz applications:

- 802.11a WLAN
- HiperLAN WLAN
- Access Points
- UNII & ISM Radios

Functional Diagram



Features

Gain: 20 dB

34% PAE @ Psat = +26 dBm

3.7% EVM @ Pout = +15 dBm
with 54 Mbps OFDM Signal

Supply Voltage: +3.0 V

Power Down Capability

Low External Part Count

General Description

The HMC415LP3 is a high efficiency GaAs InGaP Heterojunction Bipolar Transistor (HBT) MMIC Power amplifier which operates between 4.9 and 5.9 GHz. The amplifier is packaged in a low cost, leadless surface mount package with an exposed base for improved RF and thermal performance. With a minimum of external components, the amplifier provides 20 dB of gain, +26 dBm of saturated power, and 34% PAE from a +3.0V supply voltage. Vpd can be used for full power down or RF output power/current control. For +15 dBm OFDM output power (64 QAM, 54 Mbps), the HMC415LP3 achieves an error vector magnitude (EVM) of 3.7% meeting 802.11a linearity requirements.

Electrical Specifications, T_A = +25° C, Vs = 3V, Vpd = 3V

Parameter		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range			4.9 - 5.1			5.1 - 5.4			5.4 - 5.9		GHz
Gain		18	20		18.5	20.5		16	19		dB
Gain Variation Over Temperature			0.04	0.05		0.04	0.05		0.04	0.05	dB / °C
Input Return Loss			10			9			8		dB
Output Return Loss			10			12			8		dB
Output Power for 1dB Compression (P1dB)	Icq = 285 mA Icq = 200 mA	20	22.5 22.0		20.5	23.0 22.5		18	21.5 21.0		dBm
Saturated Output Power (Psat)			25.5			26			24		dBm
Output Third Order Intercept (IP3)		28	31		29	32		27	30		dBm
Error Vector Magnitude (54 Mbps OFDM Signal @ +15 dBm Pout)	Icq = 200 mA					3.7					%
Noise Figure			6			6			6		dB
Supply Current (Icq)	Vpd = 0V/3V		0.002 / 285			0.002 / 285			0.002 / 285		mA
Control Current (Ipd)	Vpd = 3V		7			7			7		mA
Switching Speed	tOn, tOff		45			45			45		ns

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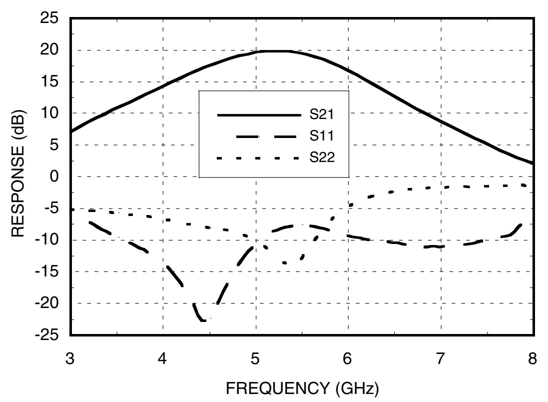
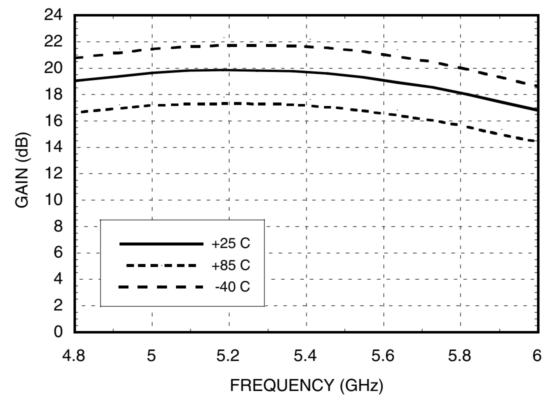
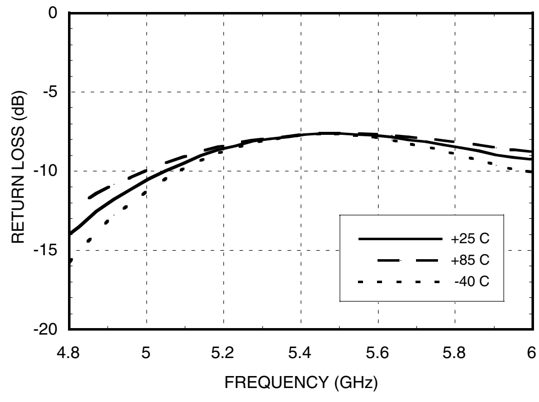
Broadband Gain & Return Loss



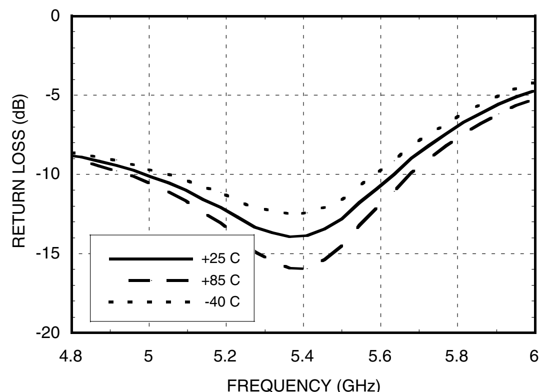
Gain vs. Temperature



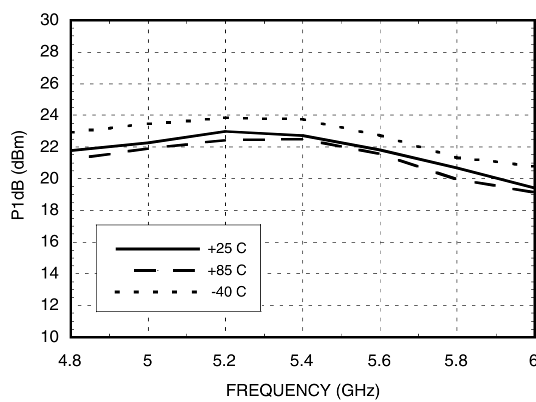
Input Return Loss vs. Temperature



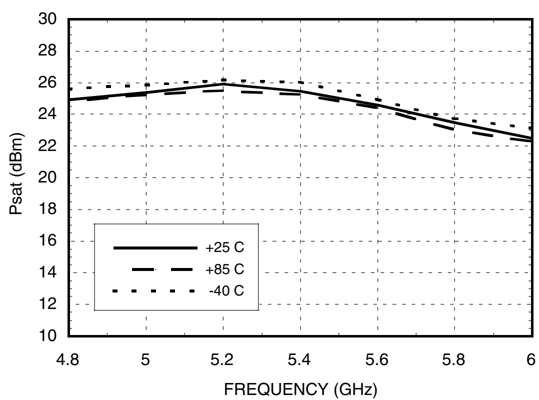
Output Return Loss vs. Temperature



P1dB vs. Temperature



Psat vs. Temperature



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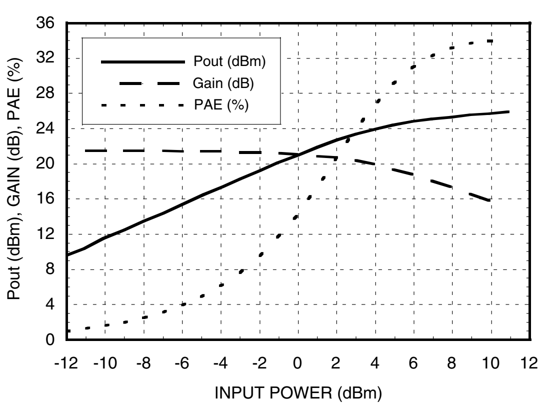
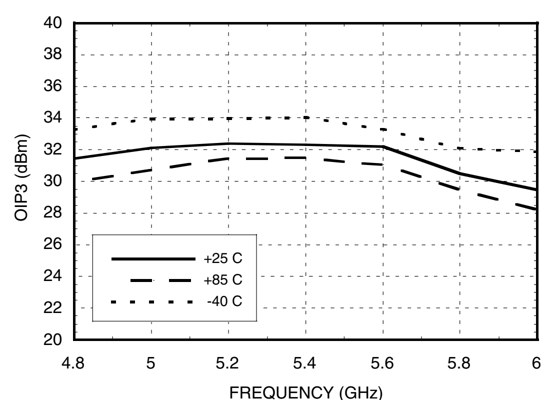
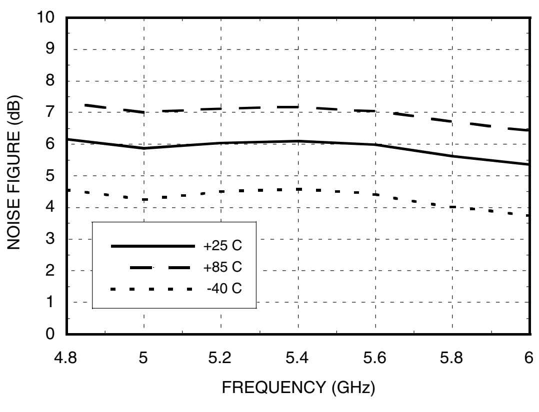
Power Compression @ 5.2 GHz



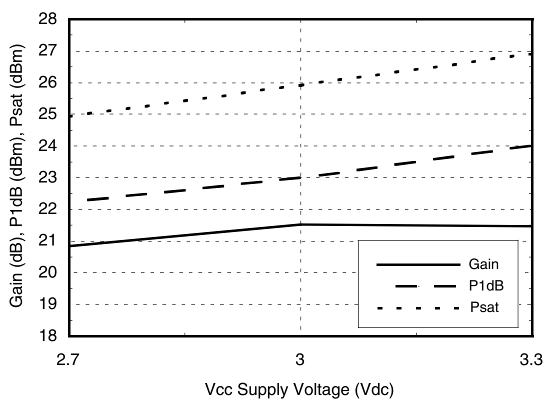
Output IP3 vs. Temperature



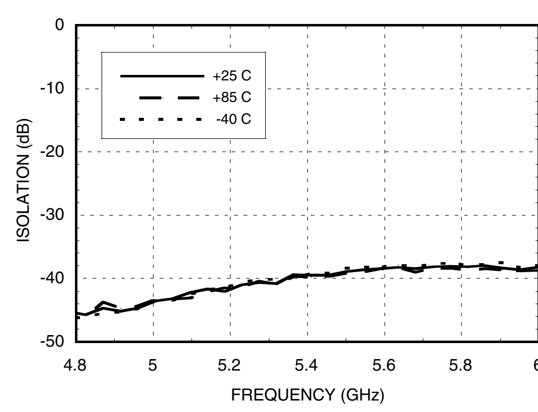
Noise Figure vs. Temperature



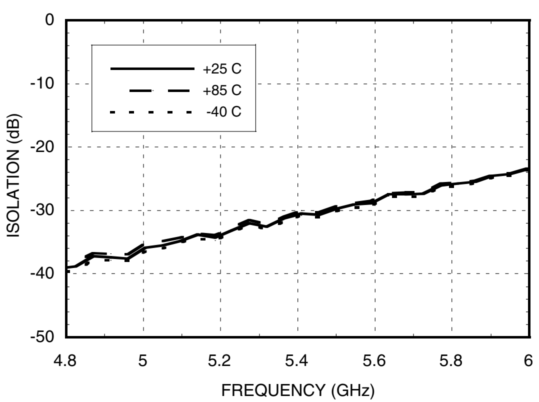
Gain & Power vs. Supply Voltage



Reverse Isolation vs. Temperature



Power Down Isolation vs. Temperature



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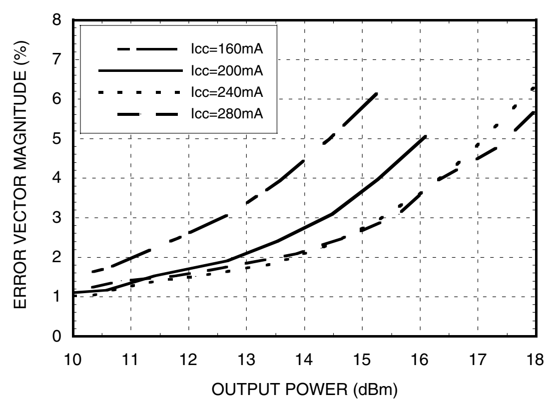
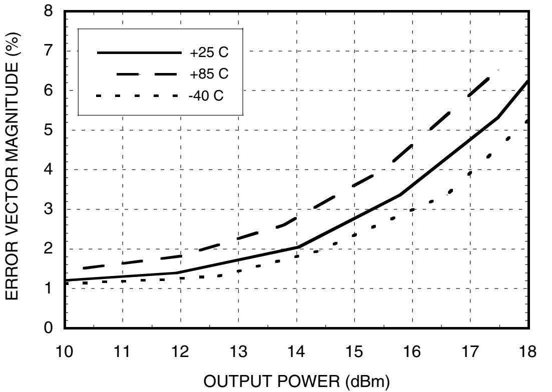
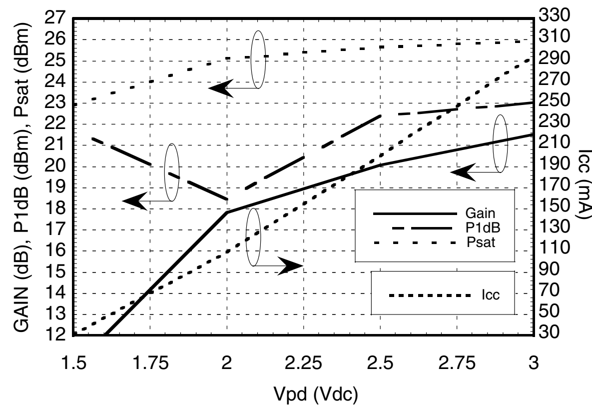
EVM vs. Supply Current, F = 5.2 GHz



EVM vs. Temperature, Icc = 240 mA, F = 5.2 GHz



Gain, Power & Quiescent Supply Current vs. Vpd @ 5.2 GHz



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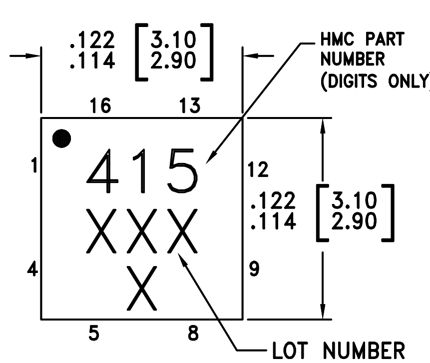
Absolute Maximum Ratings

Collector Bias Voltage (Vcc)	+5.0 Vdc
Control Voltage (Vpd)	+3.5 Vdc
RF Input Power (RFin)(Vs = Vpd = +3.0 Vdc)	+20 dBm
Junction Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	1.105 W
Thermal Resistance (junction to ground paddle)	59 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Outline Drawing



BOTTOM VIEW

PIN 16

.016 [0.40] REF
.008 [0.20] MIN

.012 [0.30]
.007 [0.18]

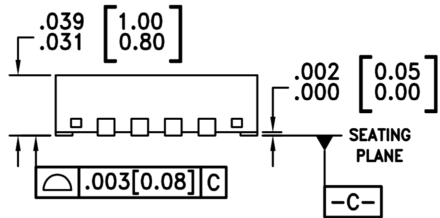
PIN 1

.061 [1.56]
.057 [1.44]

.022 [0.56]
.017 [0.44]

.077 [1.95]
.059 [1.50]
SQUARE

EXPOSED GROUND PADDLE MUST BE CONNECTED TO RF/DC GROUND



NOTES:
1. MATERIAL PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
6. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

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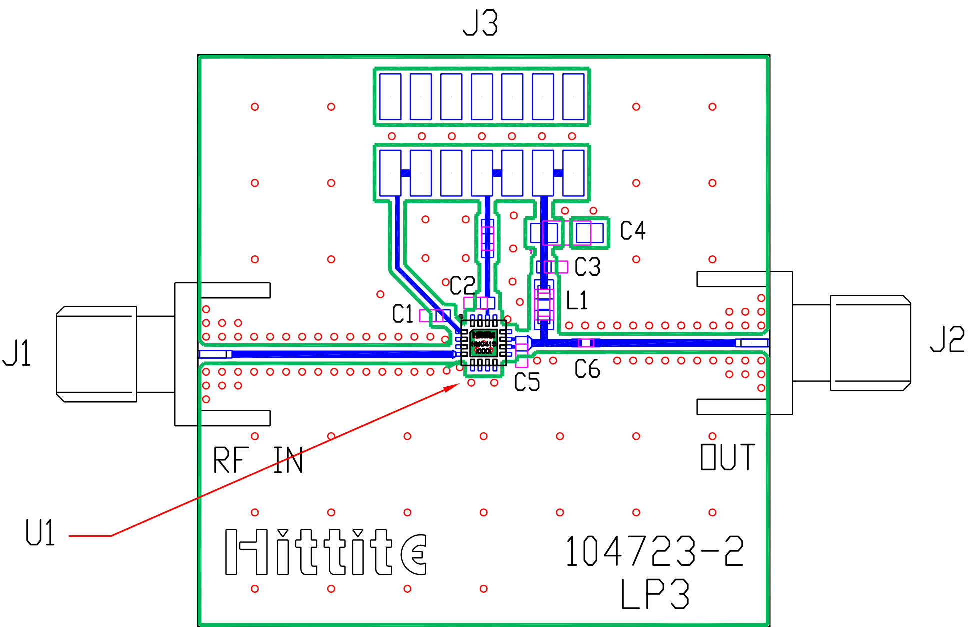
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vcc	Power supply voltage for the first amplifier stage. An external bypass capacitor of 330 pF is required as shown in the application schematic.	
2, 3, 5, 6, 7, 8, 9, 12, 13, 15, 16	GND	Ground: Backside of package has exposed metal ground slug that must be connected to ground thru a short path. Vias under the device are required.	
4	RF IN	This pin is AC coupled and matched to 50 Ohms from 5.0 to 6.0 GHz.	
10, 11	RF OUT	RF output and DC bias for the output stage.	
14	Vpd	Power control pin. For maximum power, this pin should be connected to 3.0V. A higher voltage is not recommemded. For lower idle current, this voltage can be reduced.	

Evaluation PCB



List of Material

Item	Description
J1 - J2	PC Mount SMA RF Connector
J3	2 mm DC Header
C1 - C3	330 pF Capacitor, 0603 Pkg.
C4	2.2 µF Capacitor, Tantalum
C5	0.5 pF Capacitor, 0603 Pkg.
C6	7.0 pF Capacitor, 0402 Pkg.
L1	3.0 nH Inductor, 0805 Pkg.
U1	HMC415LP3 Amplifier
PCB*	104723 Eval Board
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

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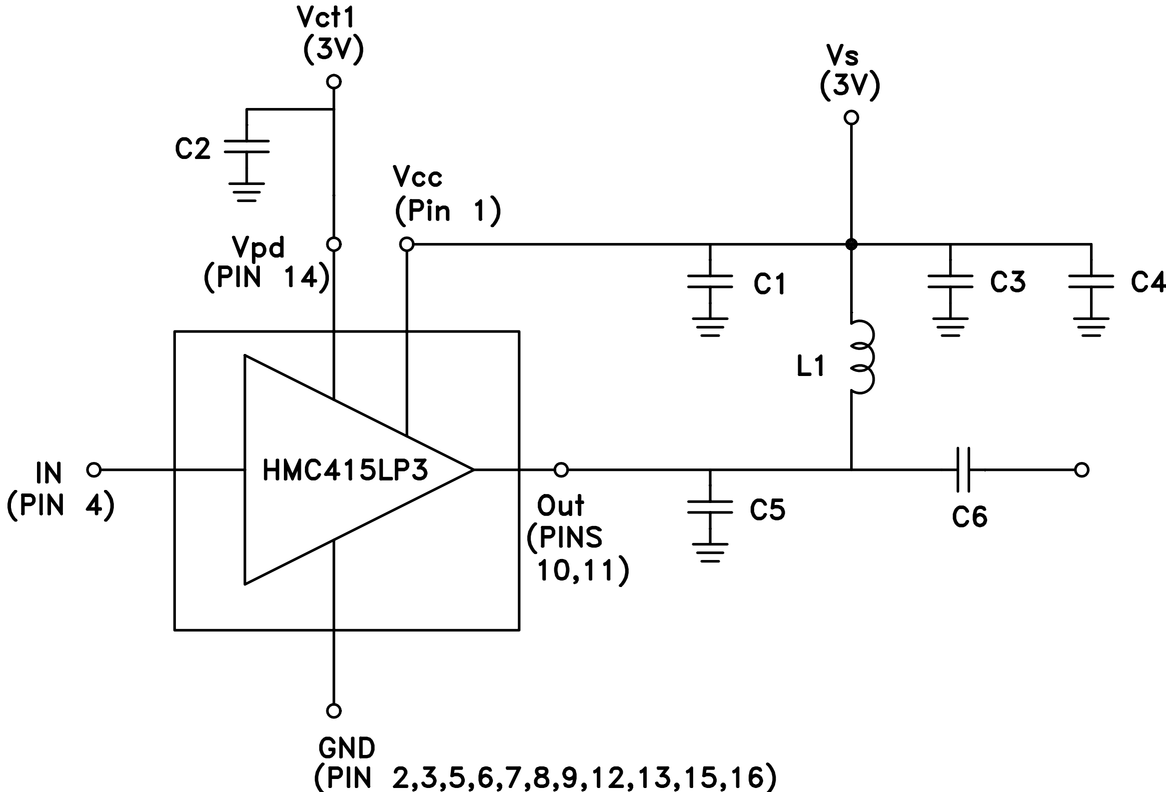
Application Circuit



Recommended Component Values	
L1	3.0 nH
C1, C2, C3	330 pF
C4	2.2 µF
C5	0.5 pF
C6	7.0 pF

Note 1: C1 should be located < 0.1” (2.54mm) from Pin 1 (Vcc)
Note 2: C3 should be located < 0.1” (2.54mm) from L1.