Advance Information

Full Bridge Driver

MC33253

55 VOLT
FULL BRIDGE DRIVER

The MC33253 is a full bridge driver including integrated charge pump, two independent high and low side driver channels.

The high and low side drivers include a cross conduction suppression circuit, which, if enabled, prevents the external power FETs from being on at the same time.

The drive outputs are capable to source and sink 1 A pulse peak current.

The low side channel is referenced to ground, the high side channel is floating above ground.

A linear regulator provides a maximum of 15.5V to supply the low side gate driver stages. The high side driver stages are supplied with a 10V charge pump voltage. Such built–in feature, associated to external capacitor provides a full floating high side drive.

A under– and over–voltage protection prevents erratic system operation at abnormal supply voltages. Under fault, these functions force the driver stages into off state.

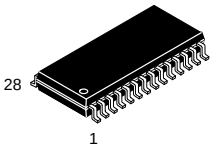
The logic inputs are compatible with standard CMOS or LSTTL outputs. The input hysteresis makes the output switching time independent of the input transition time.

The global enable logic signal can be used to disable the charge pump and all the bias circuit. The net advantage is the reducuction of the quiescent supply current to under 10µA. To wake up the circuit, 5 V has to be provided at G_EN.

A built–in single supply operational amplifier could be used to feedback information from the output load to the external MCU.

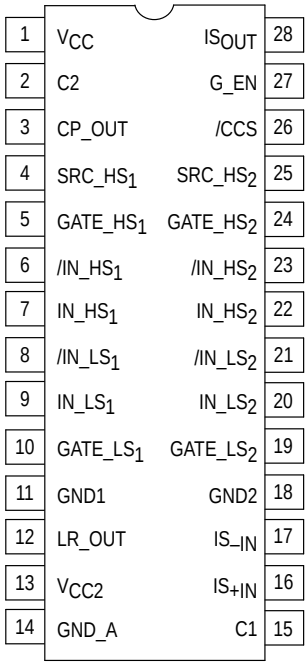
Features:

- V_{CC} Operating Voltage Range from 5.5 V up to 55 V
- V_{CC2} Operating Voltage Range from 5.5 V up to 28 V
- Automotive Temperature Range –40°C to 125°C
- 1A Pulse Current Output Driver
- Fast PWM Capability
- Built–In Charge Pump
- Cross Conduction Supression Circuit



DW SUFFIX
PLASTIC PACKAGE
CASE 751F–05
(SO–28)

PIN CONNECTIONS
(TOP VIEW)
CASE 751F–05
(28 SOIC)



MC33253

ORDERING INFORMATION

Device	Temperature Range	Package
MC33253DW	T_A = – 40°C to +125°C	Plastic SOIC28

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SIMPLIFIED BLOCK DIAGRAM

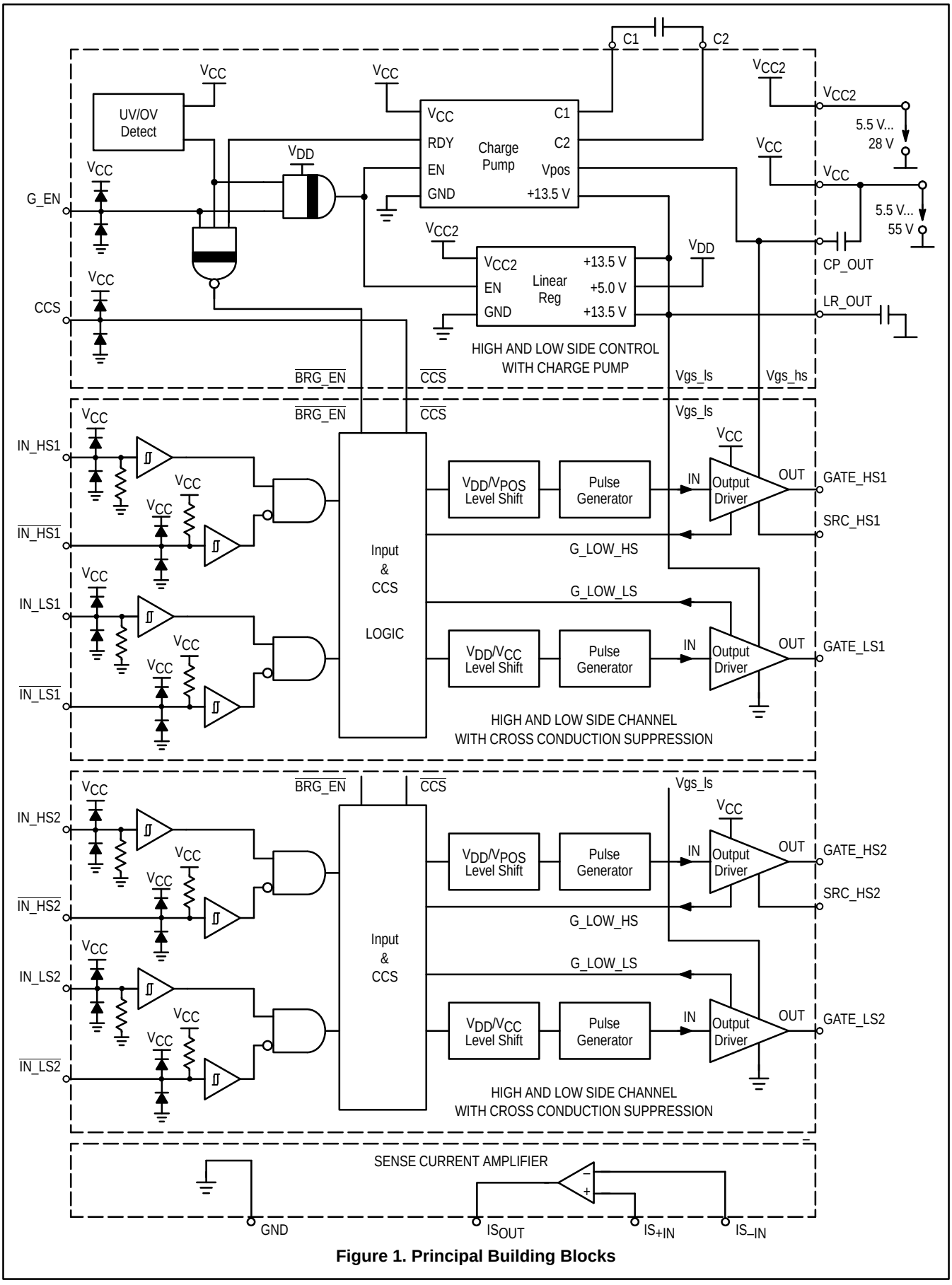


Figure 1. Principal Building Blocks

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to GND.

Rating	Symbol	Min	Max	Unit
Supply Voltage 1	V_{CC}	–0.3	60	V_{DC}
Supply Voltage 2	V_{CC2}	–0.3	28	V_{DC}
Linear Regulator Output Voltage	V_{LR_out}	–0.3	16	V_{DC}
High Side Floating Supply Absolute Voltage	V_{CP_OUT}	–0.3	65	V_{DC}
High Side Floating Supply Offset Voltage	V_{SRCHS}	–0.3	65	V_{DC}
High Side Floating Output Voltage	V_{GATEHS}	–0.3	65	V_{DC}
Low Side Output Voltage	V_{GATELS}	–0.3	16	V_{DC}
Logic Input Voltage	V_{IN}	–0.3	10	V_{DC}
Max V_{POSHS} Slew Rate	dV/dt	—	5.0	V/ns
Power Dissipation and Thermal Characteristics				
Maximum Power Dissipation	P_D			W
Thermal Resistance Junction–to–Air	$R_{\theta JA}$			°C/W
Operating Junction Temperature	T_J	–40	+150	°C
Storage Temperature	T_{stg}	–65	+150	°C

OPERATING CONDITIONS

(Typical values for T_A = 25°C, Min/Max values for T_A = –40°C to +125°C)

Rating	Symbol	Min	Max	Unit
Supply Voltage (VPower)	V_{CC}	5.5	55	V
Supply Voltage 2 (VBATT)	V_{CC2}	5.5	28	V
High Side Floating Supply Absolute Voltage	V_{CP_OUT}	V_{CC}+4	V_{CC}+11 but <65	V
Logic Input Voltage	V_{IN}	0	10	V
Ambient Temperature Range	T_A	–40	+125	°C

STATIC ELECTRICAL CHARACTERISTICS V_{CC} = 12 V, V_{CC2} = 12 V, C_{CP} = 33 nF, G_EN = 4.5 V unless otherwise specified. (Typical values for T_A = 25°C, Min/Max values for T_A = –40°C to +125°C, unless otherwise specified)

Characteristic	Pin #	Symbol	Min	Typ	Max	Unit
LOGIC SECTION						
Logic “1” Input Voltage (IN_LS & IN_HS)		V_{IH}	2.0	–	10	V
Logic “0” Input Voltage (IN_LS & IN_HS)		V_{IL}	–	–	0.8	V
Wake Up Input Voltage (G_EN)	27	V_{G_EN}	4.5	5.0 V	V_{CC2}	V
Wake Up Current (G_EN) VG_EN = 14 V	27	I_{G_EN}	–	250	500	μA
LINEAR REGULATOR SECTION						
Linear Regulator V_{Irout} @ V_{CC2} = 28 V	12	V_{Irout}	13.5	–	15.5	V
V_{Irout} @ $V_{CC2} \leq$ 12 V	12		V_{CC2} – 1	–	12	
CHARGE PUMP SECTION						
Charge Pump Output Voltage, I_{LOAD} = 0 mA	3	V_{CP_OUT}	V_{CC} + 8	V_{CC} + 9	V_{CC} + 11	V
Charge Pump Output Voltage, I_{LOAD} = 7 mA	3	V_{CP_OUT}	V_{CC} + 8	V_{CC} + 9	V_{CC} + 11	V
UNDER/OVERVOLTAGE SECTION						
Under Voltage Shutdown V_{CC2}	13	UV2	4.6	5.1	5.5	V
Under Voltage Shutdown V_{CC}	1	UV	4.6	5.1	5.5	V
Over Voltage Shutdown V_{CC}	1	OV	56	64	70	V
Over Voltage Shutdown V_{CC2}	13	OV2	28	31	34	V
OUTPUT SECTION						
Output Sink Resistor (turned off) V_{GS} = 1.0 V	5, 10 19, 24	R_{DS}	–	–	5.0	Ω
Output Source Resistor (turned on) ΔV_{GS} = 0, 1V		R_{DS}	–	–	5.0	Ω
High Side Gate Voltage ON State	5, 10 19, 24	V_{GS_HS}	–	–	V_{CC}+11	V
High Side Gate Voltage OFF State (Reference to SRC_HS)		V_{GS_HS}	–	–	0.5	V
Low Side Gate Voltage ON State		V_{GS_LS}	–	–	15.5	V
Low Side Gate Voltage OFF State		V_{GS_LS}	–	–	0.5	V
SENSE CURRENT AMPLIFIER SECTION (Internal V_{CC} supply @ 7V)						
Output Dynamic Range ($I_{sink/source}$ = 200μA)	28	V_{OH} V_{OL}	4.7 –	5.0 –	– 300	V mV
Open Loop Gain (at 25°C) (Note 2)		A	–	50	–	dB
Input Bias Current	16, 17	I_{IB}	–	–	1.0	μA
Input Offset Voltage (at 25°C)	16, 17	V_{io}	–	2.0	5.0	mV
Input Common Mode Range		V_{ICR}	–	–	3.0	V
Sink Capability (V_O > 1.1V) (Note 3)	28	I_{sink}	2.0	3.0	–	mA
Source Capability (V_O < 5V) (Note 3)	28	I_{source}	2.0	3.0	–	mA
Gain Bandwidth Product		GBW	–	1.8	–	MHz

NOTE 1 Rise time is given by time needed to charge the gate from 1.0 V to 10 V (vice versa for fall time)
NOTE 2 Characterization only
NOTE 3 Input Overdrive 1V

SUPPLY SECTION

Quiescent Supply Current V_{CC2} (G_EN = 0)	13	I_{QSD}	–	–	10	μA
Quiescent Supply Current V_{CC} (G_EN = 0)	1	I_{QSD}	–	–	10	μA
Supply Current V_{CC}	1	I_{OP}	–	0.5	3.0	mA
Supply Current V_{CC2}	13	I_{OP}	–	5.0	8.0	mA

DYNAMIC ELECTRICAL CHARACTERISTICS (Typical values for T_A = 25°C, Min/Max values for T_A = –40°C to +125°C)

Prop. Delay HS and LS between 50% input to 50% output, C_l = 5.0 nF		T_{PD}	–	200	300	ns
HS/LS Rise Time @ C_l = 5.0 nF, 10% to 90%		T_{RISE}	–	80	180	ns
HS/LS Fall Time @ C_l = 5.0 nF, 90% to 10%		T_{FALL}	–	80	180	ns

NOTE 1 Rise time is given by time needed to charge the gate from 1.0 V to 10 V (vice versa for fall time)
NOTE 2 Characterization only
NOTE 3 Input Overdrive 1V

Driver Characteristics

Turn–On:

For turn–on the current required to charge the gate source capacitor C_{iss} in the specified time can be calculated as follows:

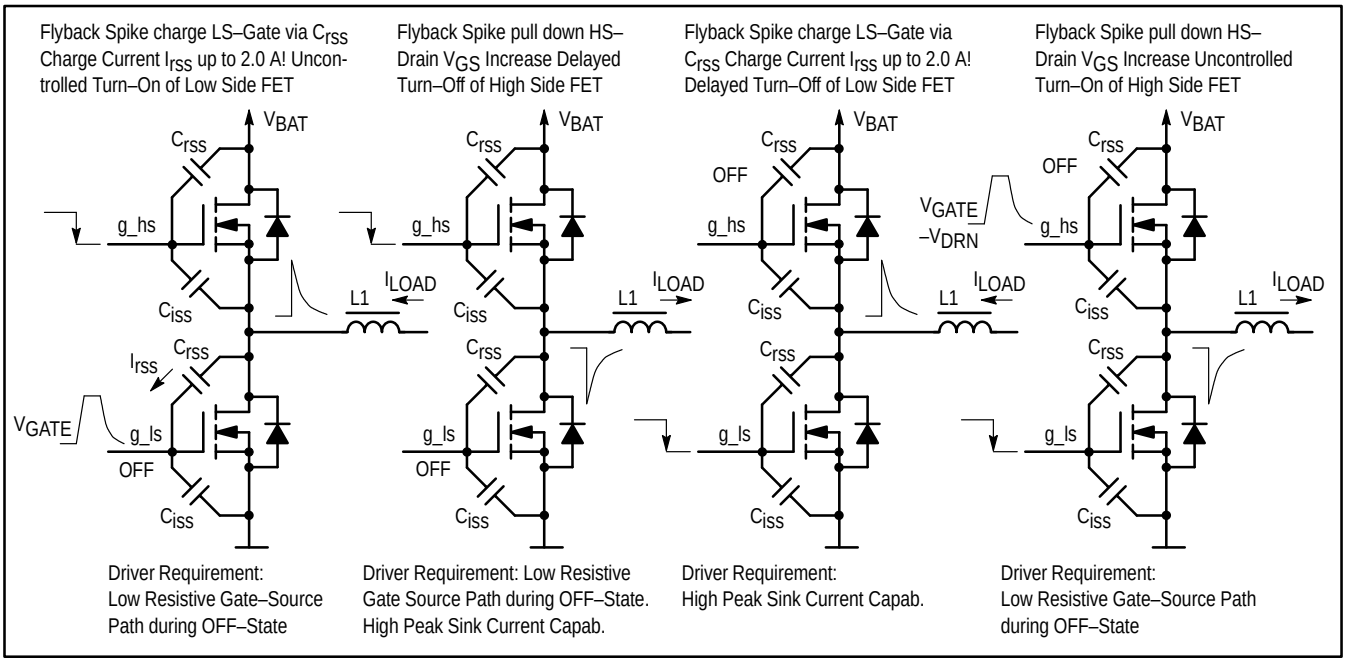
Peak Current for Rise/Fall Time (tr) and a typical PowerMosFET Gate Charge Q_g

$I_P = Q_g/tr = 75\ nC/80\ ns \approx 1.0\ A$

Turn–Off:

The peak current for turn–off can be obtained in the same way as for turn–on.

In addition to the dynamically current, required to turn–off or turn–on the FET, various application related switching scenarios have to be considered:



The output driver sources a peak current of up to 1A for 200 ns to turn on the gate. After 200 ns 100 mA are provided continuously to maintain the gate charged.

The output driver sinks a peak current of up to 1A for 200 ns to turn off the gate. After 200 ns 100 mA are sinked continuously to maintain the gate discharged.

In order to withstand high dV/dt spikes (up to 10 V/ns) a low resistive path between gate and source is implemented during the off state.

Driver Supply

The High Side Driver is supplied from the internal charge pump buffered at CP_OUT.

The low–drop regulator provides approx. 3.5 mA (f_{PWM} = 50kHz) per gate. In case of the full bridge that means approx. 14 mA, 7.0 mA for the high side and 7.0 mA for the low side.

(Note: The average current required to switch a gate with a frequency of 100 kHz is:

Average Current (Charge Pump) for PWM Frq. (f_{PWM})

$I_{CP} = Q_g * f_{PWM} = 75\ nC * 100\ kHz = 7{,}5\ mA$

A full bridge application switch only one high side and one low side at the same time.)

External capacitors on Charge Pump and on Linear Regulator are necessary to supply high peak current absorbed during switching.

The Low Side Driver is supplied from built in low drop regulator.

Gate Protection

The low side gate is protected by the internal linear regulator, which guarantees that V_{GATE_LS} does not exceed the maximum V_{GS}.

Especially when working with the charge pump the voltage at POS_HS can be up to 65 V!. The high side gate is clamped internally, in order to avoid a V_{GS} exceeding 14 V.

The Gate protection does not include a Flyback Voltage Clamp that protects the driver and the external FET from a Flyback voltage that can appear when driving inductive load. This Flyback voltage can reach high negative voltage values and needs to be clamped externally.

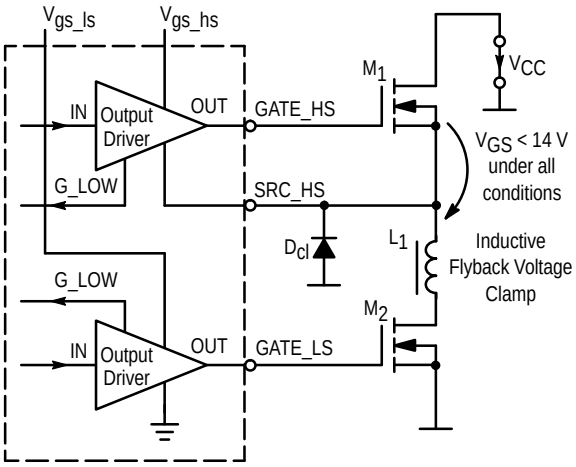


Figure 2. Gate Protection and Flyback Voltage Clamp

TMOS Failure Protection

All output driver stages are protected against TMOS failure conditions.

If one of the external power FETs is destroyed (Gate = V_{CC}, or Gate = Gnd) the function of the remaining output driver stages is not affected.

All output drivers are short circuit protected against short circuits to ground.

Cross Conduction Suppression

The purpose of the cross conduction suppression is to avoid that high and low side FET are turned on at the same time, which prevents the half bridge power FETs of a shoot–through condition.

The CCS can be disabled / enabled by an external signal (/CCS).

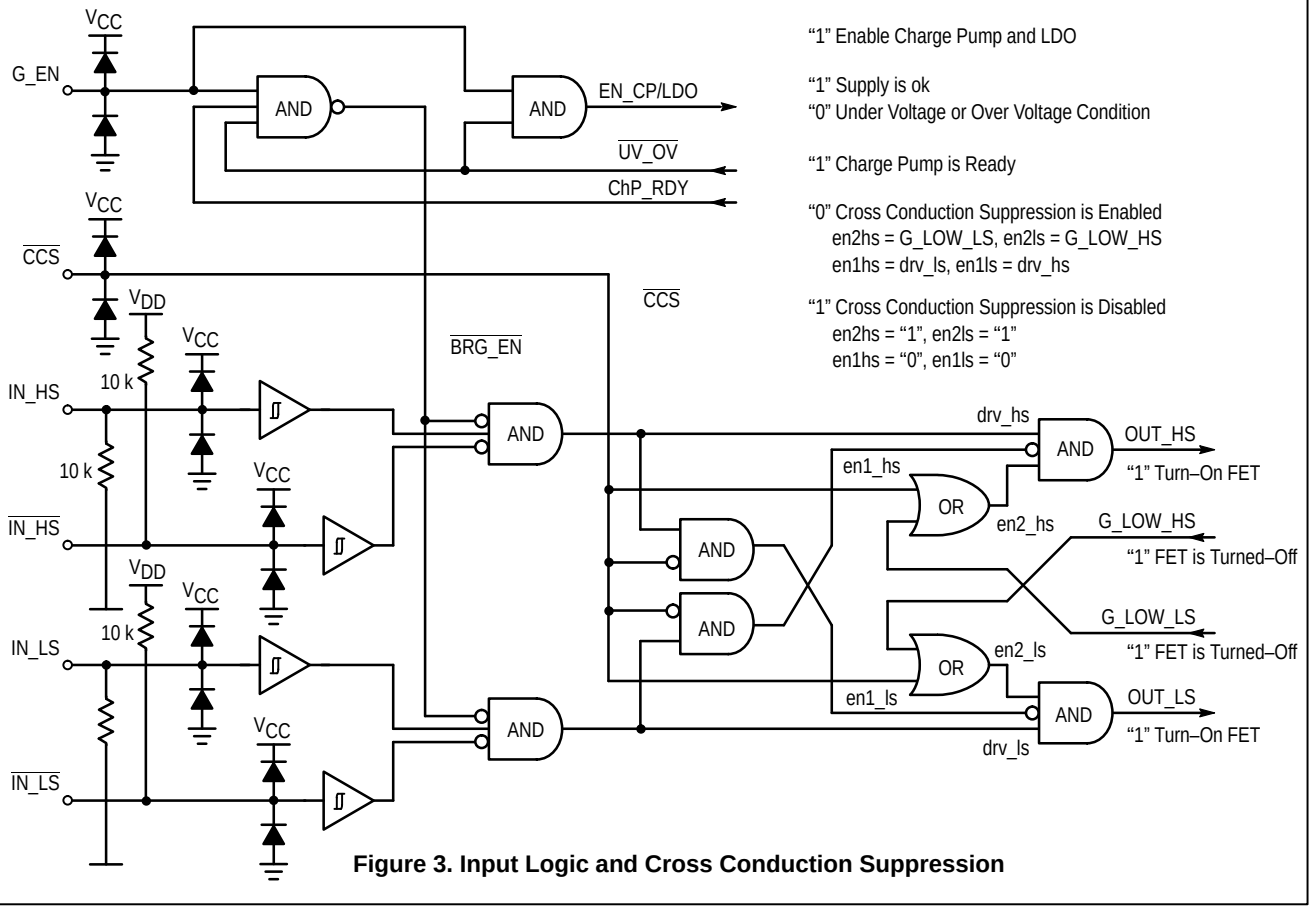


Figure 3. Input Logic and Cross Conduction Suppression

Logic Inputs

Logic Input Voltage Range:
(Max. Operating)
–0.3 V ... 10 V
Wake Up Function:
(G_EN)
4.5 V ... V_{CC2}

During Wake–Up the logic is supplied from the G_EN pin.

Low Drop Linear Regulator

The low drop linear regulator provides the 5.0 V for the logic section of the driver, the V_{gs_ls} buffered at LR_OUT and the +13.5 V for the charge pump, which generates the V_{gs_hs}.

The low drop linear regulator provides 3.5 mA average current per driver stage. If V_{CC2} exceeds 14 V the output is limited to 14.5 V.

Charge Pump

The charge pump generates the high side driver supply voltage (V_{gs_hs}), buffered at CP_OUT.
$V_{gs\_hs} = V_{CC} + V_{CC2} – 1.2$ V.

The average output current is I_{CP} = 3.5 mA (f_{PWM} = 50 kHz) per output driver.

The charge pump charges an external storage capacitor, which provides the peak switching current to the high side output drivers.

Sense Current OP–Amp

Typically shunt resistivity is dimensioned as low as possible (50 mOhm/10 A). The typical voltage generated by sensing the current is in the range of 500 mV. The A/D input of typical micro controller is in the range of 5.0 V. That requires a voltage gain of 10.

Over / Under Voltage Shutdown

The under voltage protection becomes active at V_{CC} below 5.5 V and the overvoltage protection is activated at V_{CC} above 55 V or at V_{CC2} above 28 V.

If the OUV protection is activated the outputs are driven low, in order to switch off the FETs.

Protection

A protection against double battery and load dump spikes up to 55 V is given by V_{CC} = 55 V.

A protection against reverse polarity is given by the external power FET with the free wheeling diodes, forming a conducting pass from ground to V_{CC}. An additional protection is not provided within the circuit.

There is a temperature shut down protector per each half bridge. It protects the circuitry against temperature damage by blocking the output drives.

APPLICATION DIAGRAM

Both applications utilize the internal charge pump to provide the high side floating voltage. This voltage can be provided by an external source also.

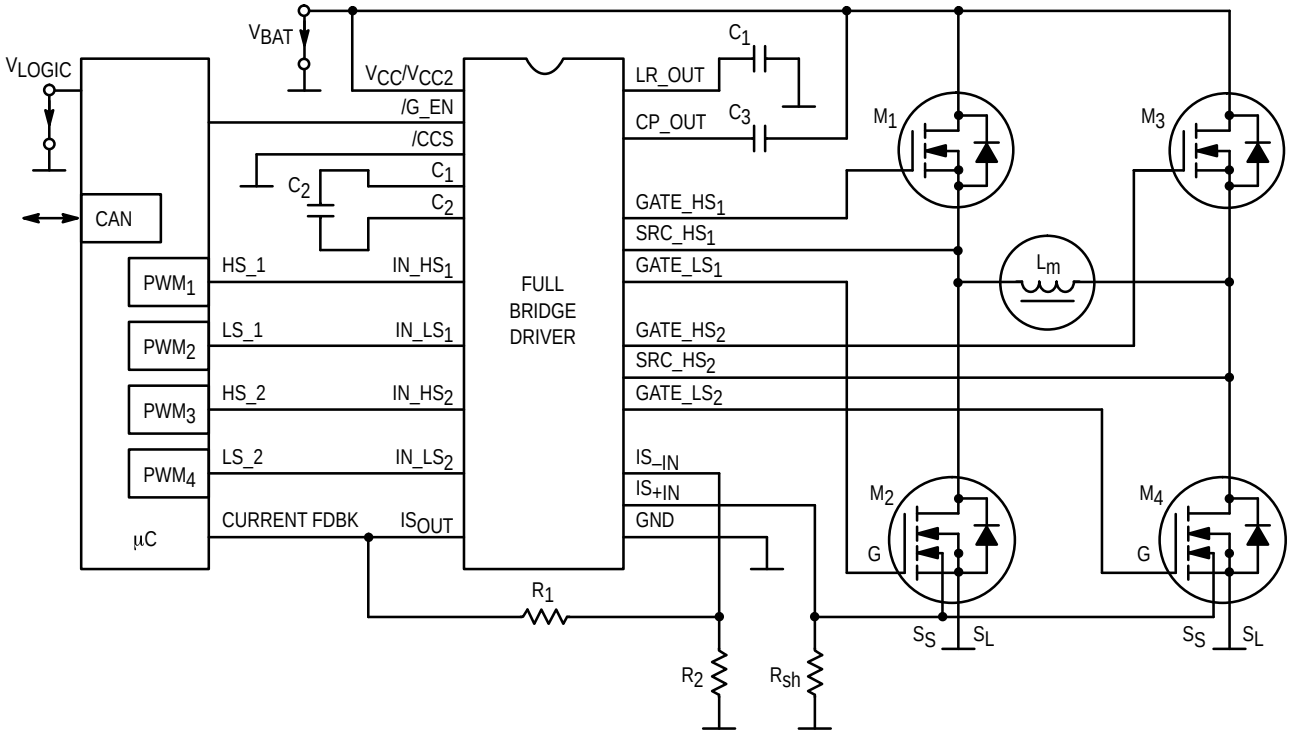


Figure 4. DC Motor Control with Micro Controller

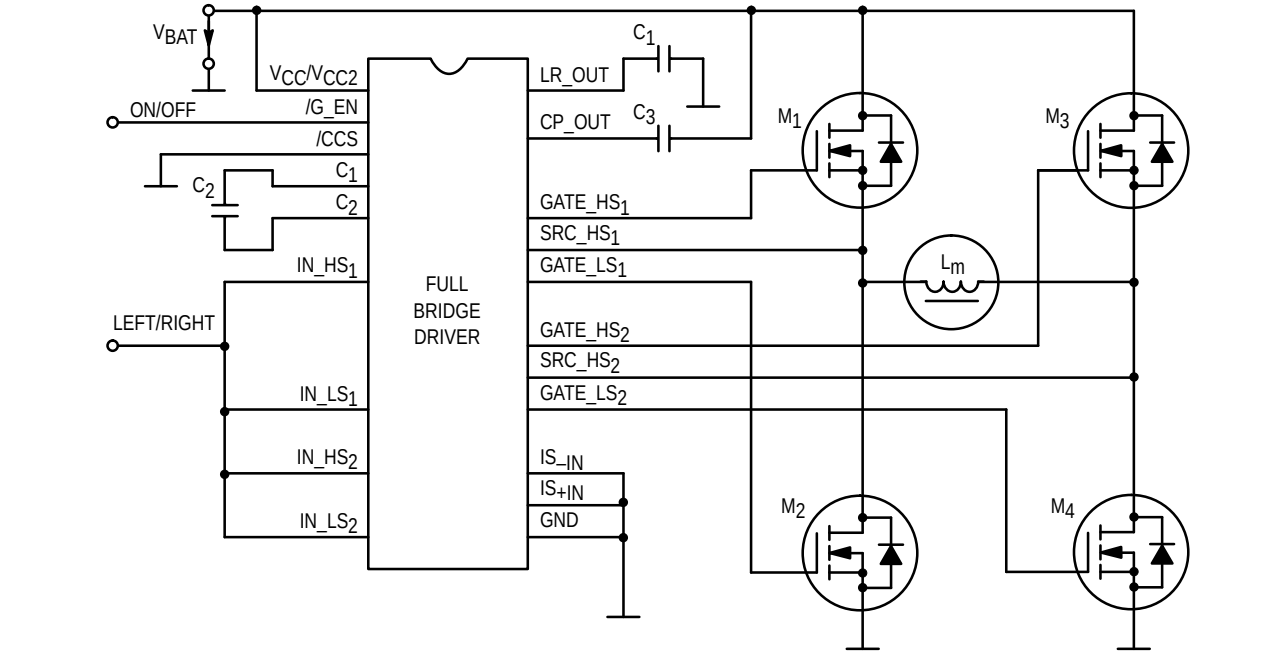
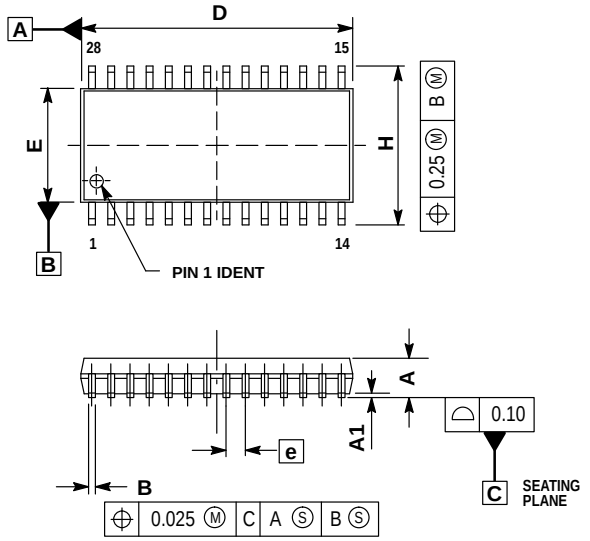


Figure 5. DC Motor Control (low cost)

PIN DEFINITIONS

Pin	Symbol	Pin Description
1	V_{CC}	Supply 1
2	C2	Charge Pump Capacitor
3	CP_OUT	Charge Pump Out
4	SRC_HS1	Source 1 Output High Side
5	GATE_HS1	Gate 1 Output High Side
6	/IN_HS1	Neg. Input High Side 1
7	IN_HS1	Pos. Input High Side 1
8	/IN_LS1	Neg. Input Low Side 1
9	IN_LS1	Pos. Input Low Side 1
10	GATE_LS1	Gate 1 Output Low Side
11	GND1	Ground
12	LR_OUT	Linear Regulator Output
13	V_{CC2}	Supply 2
14	GND_A	Analog Ground
15	C1	Charge Pump Capacitor
16	IS+	Sense OpAmp Pos. Input
17	IS–	Sense OpAmp Neg. Input
18	GND2	Ground 2
19	GATE_LS2	Gate 2 Output Low Side
20	IN_LS2	Pos. Input Low Side 2
21	/IN_LS2	Neg. Input Low Side 2
22	IN_HS2	Pos. Input High Side 2
23	/IN_HS2	Neg. Input High Side 2
24	GATE_HS2	Gate 2 Output High Side
25	SRC_HS2	Source 2 Output High Side
26	/CCS	Enable Cross Conduction Supression
27	G_EN	Global Enable
28	IS_OUT	Sense Current OpAmp Output

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0 °	8 °

CASE 751F–05
ISSUE F

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