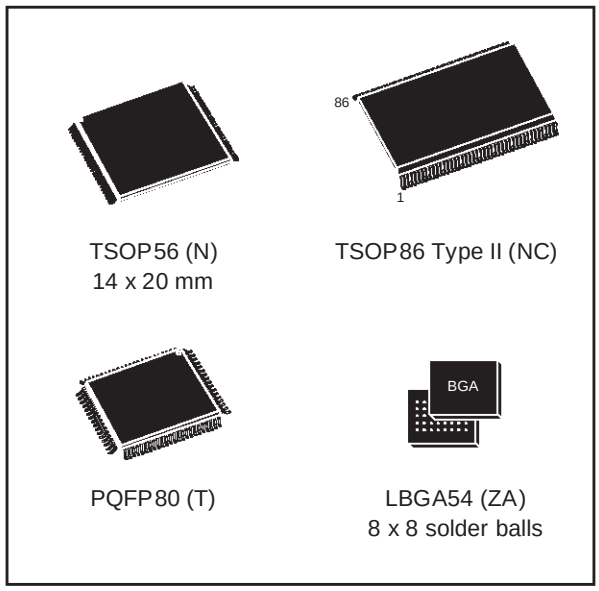
M58LW064A
M58LW064B

64 Mbit (4Mb x16 or 2Mb x32, Uniform Block) 3V Supply Flash Memories

PRELIMINARY DATA

- WIDE x16/x32 DATA BUS for HIGH BANDWIDTH
  - M58LW064A x16 DATA BITS
  - M58LW064B x16/x32 DATA BITS
- SUPPLY VOLTAGE
  - V_{CC} = 2.7V to 3.6V Supply Voltage
  - V_{CCQ} = 1.8V to 3.6V Input/Output Supply Voltage
- SYNCHRONOUS/ASYNCHRONOUS READ
  - Synchronous Burst read
  - Asynchronous Random Read
  - Address Latch Configurable
  - Page Read
- PIPELINED SYNCHRONOUS BURST INTERFACE
- ACCESS TIME
  - Synchronous Burst Read up to 66MHz
  - Asynchronous Page Mode Read 150/25ns
  - Random Read 150ns
- PROGRAMMING TIME
  - 16 Word or 8 Double-Word Write Buffer
  - 12µs Word effective programming time
- 64 UNIFORM 64 KWord MEMORY BLOCKS
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code M58LW064A: 17h
  - Device Code M58LW064B: 14h



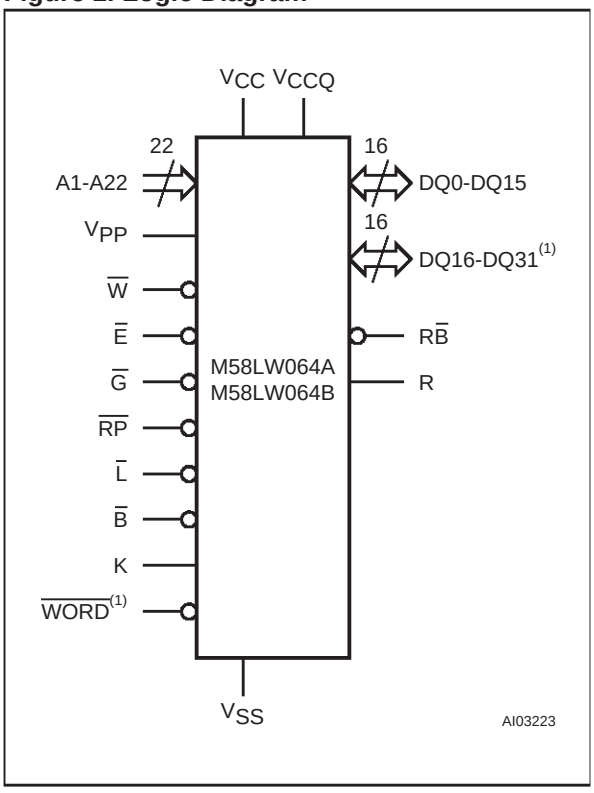
TSOP56 (N)
14 x 20 mm

TSOP86 Type II (NC)

PQFP80 (T)

LBGA54 (ZA)
8 x 8 solder balls

Figure 1. Logic Diagram



Note: 1. M58LW064B only.

Table 1. Signal Names

A1-A22	Address Inputs x16 Organization
A2-A22	Address inputs x32 Organization
DQ0-DQ7	Data Input/Output x16 and x32 Organization Command Input, Electronic Signature Output, Block Protection Status Output, Status Register Output
DQ8-DQ15	Data Input/Output x16 and x32 Organization
DQ16-DQ31	Data Input/Output x32 Organization
$\overline{B}$	Burst Address Advance
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
K	Burst Clock
$\overline{L}$	Latch Enable
R	Valid Data Ready (open drain output)
$R\overline{B}$	Ready/Busy (open drain output)
$\overline{RP}$	Reset/Power-down
V_{PP}	Program/Erase Enable
$\overline{W}$	Write Enable
$\overline{WORD}$	Word Organization (M58LW064B only)
V_{CC}	Supply Voltage
V_{CCQ}	Input/Output Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

DESCRIPTION

The M58LW064 is a non-volatile Flash memory that may be erased electrically at the block level and programmed in-system on a 16 Word or 8 Double-Word basis using a 2.7V to 3.6V supply for the core and a supply down to 1.8V for the Input and Output buffers. The M58LW064A is organized as 4Mb x16. The M58LW064B is organized as 4Mb x16 or 2Mb x32 bit organization selectable by the Word Organization input, $\overline{WORD}$. Both memories are internally configured as 64 blocks of 1 Mbit each. The memories support Asynchronous Random and Latch Enable Controlled Read with Page mode as well as Synchronous Burst Read with a configurable burst. They also support pipelined synchronous Burst Read. Writing is Asynchronous or Asynchronous Latch Enable Controlled.

The configurable synchronous burst read interface allows a high data transfer rate controlled by the Burst Clock signal, K. The interface is capable of bursting fixed or unlimited lengths of data. The burst type, latency and length are configurable and can be easily adapted to a large variety of system clock frequencies and microprocessors. A 16 Word or 8 Double-Word Write Buffer improves effective programming speed by up to 20 times when data is programmed in full buffer increments. Effective Word programming takes typically 12µs. The array matrix organization allows each block to be erased and reprogrammed without affecting other blocks. Program and Erase operations can be suspended in order to perform Read operations in any other block and then resumed; suspended Erase operations also allow Program operations to be performed in other blocks. All blocks are protected against spurious programming and erase cycles at power-up. Any block can be separately protected at any time. The block protection bits can also be reset, this is executed as one sequence for all blocks simultaneously. Block protection can be temporarily disabled. Each block can be programmed and erased over 100,000 times. Block erase is performed in typically 1 second.

An internal Command Interface (C.I.) decodes Instructions to access/modify the memory content. The Program/Erase Controller (P/E.C.) automatically executes the algorithms taking care of the timings required by the program and erase operations. Verification is internally performed and a Status Register tracks the status of the operations. The Ready/Busy output, $R\overline{B}$, indicates the completion of operations.

Instructions are written to the memory through the Command Interface (C.I.) using standard microprocessor write timings. The memory supports the Common Flash Interface (CFI) command set definition.

A Reset/Power-down mode is entered when the $\overline{RP}$ input is Low. In this mode the power consumption is lower than in the normal standby mode, the memory is write protected and both the Status and the Burst Configuration Registers are cleared. A recovery time is required when the $\overline{RP}$ input goes High.

The memory is offered in various packages. The M58LW064A is available in TSOP56 (14 x 20 mm) and LBGA54 1 mm ball pitch. The M58LW064B is available in PQFP80 and TSOP56 Type II.

Figure 2. TSOP56 Connections

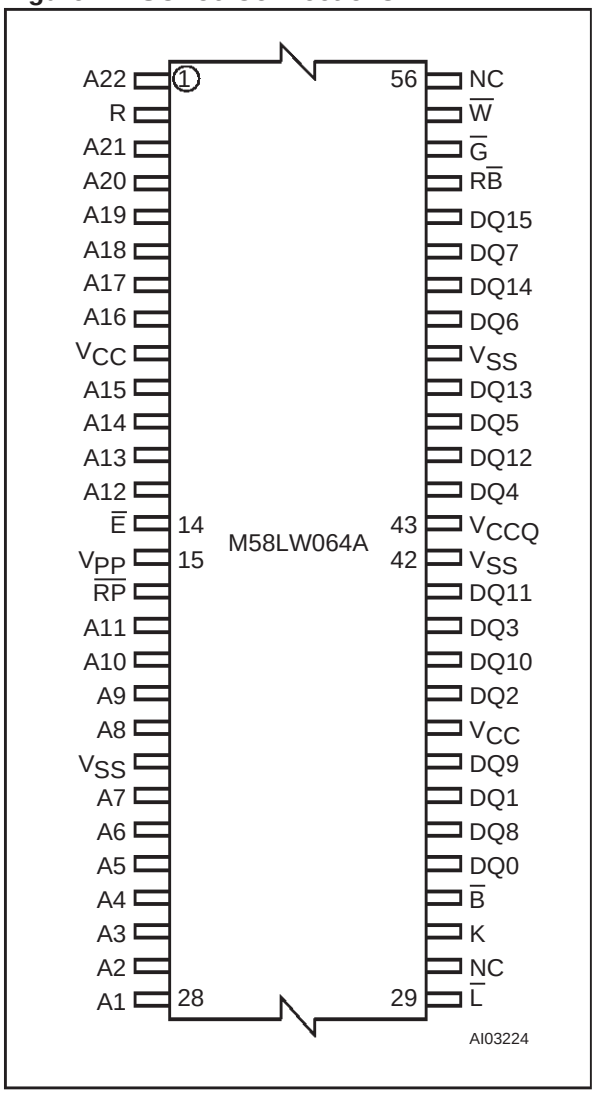


Figure 3. TSOP86 Type II Connections

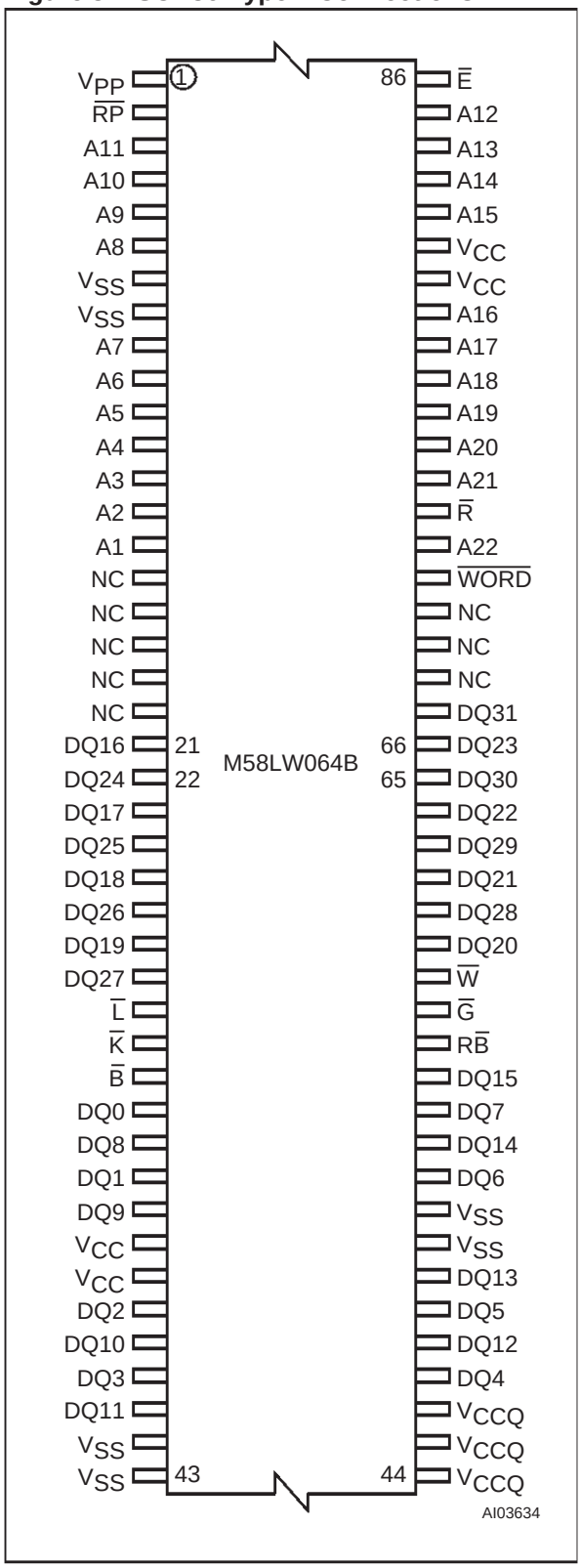


Figure 4. LBGA Connections for M58LW064A (Top view through package)

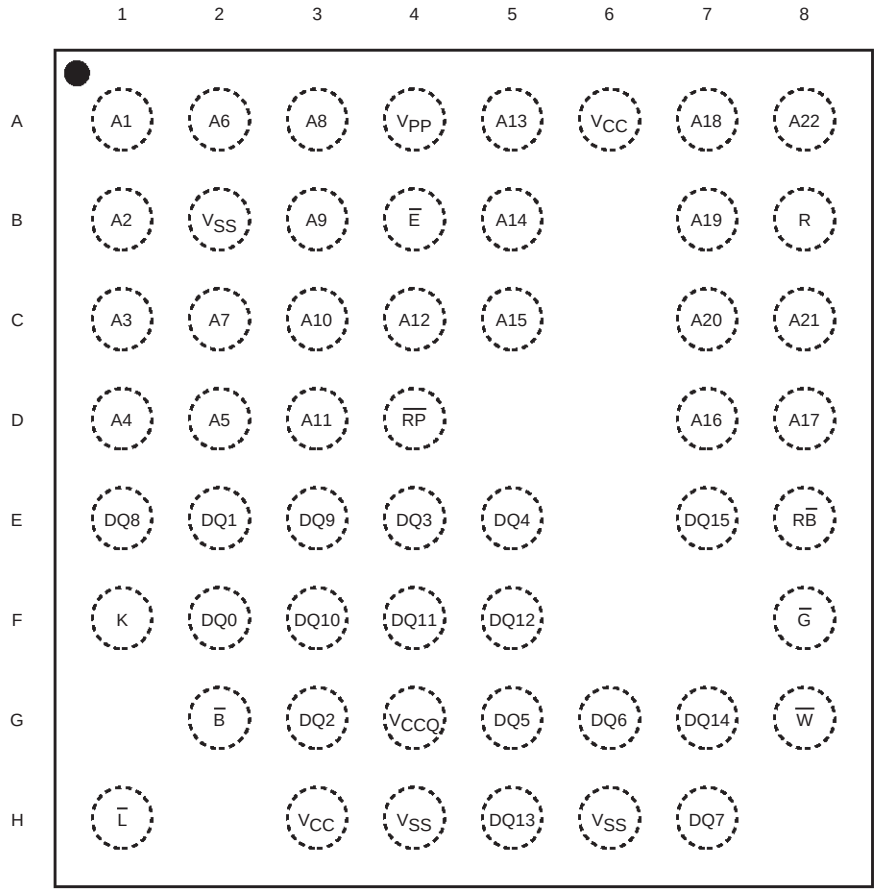


Figure 5. PQFP Connections

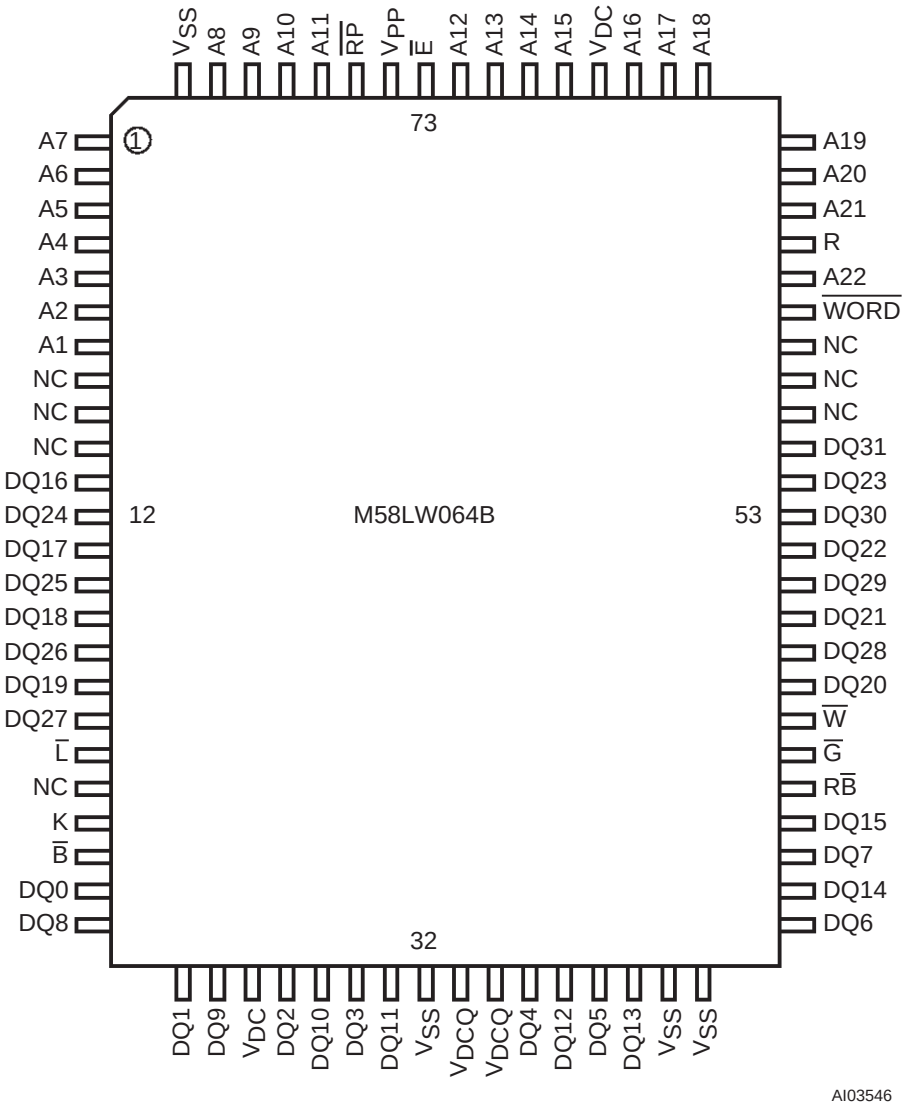


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	Grade 1	0 to 70	°C
		Grade 6	–40 to 85	°C
T_{BIAS}	Temperature Under Bias		–40 to 125	°C
T_{STG}	Storage Temperature		–55 to 150	°C
V_{IO}	Input or Output Voltage		–0.6 to V_{CCQ} +0.6	V
V_{CC}, V_{CCQ}	Supply Voltage		–0.6 to 5.0	V
V_{HH}	$\overline{RP}$ Hardware Block Unlock Voltage		–0.6 to 10 (2)	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Cumulative time at a high voltage level of 10V should not exceed 80 hours on $\overline{RP}$ pin.

ORGANIZATION

Memory control is provided by Chip Enable, $\overline{E}$, Output Enable, $\overline{G}$, and Write Enable, $\overline{W}$, inputs. A Latch Enable, L, input latches an address for both Read and Write operations. The Burst Clock, K, and the Burst Address Advance, B, inputs synchronize the memory to the microprocessor during burst read. Reset/Power-down, $\overline{RP}$, is used to reset all the memory circuitry, excluding the block protection bits, and to set the chip in deep power down mode.

Erase and Program operations are controlled by an internal Program/Erase Controller (P/E.C.).

A Status Register data output on DQ7 provides a Ready/Busy signal to indicate the state of the P/E.C. operations. A Ready/Busy, $\overline{RB}$, output also indicates the completion of the internal algorithms. A Valid Data Ready, R, output indicates the memory data output valid status during continuous synchronous burst mode operations.

A Word Organization, $\overline{WORD}$, input selects the x16 or x32 data width for the M58LW064B. For the x16 only organization of the M58LW064A or the x16 organization of the M58LW064B the address lines are A1-A22 and the Data Input/Output is on DQ0-DQ15. For the x32 organization of the M58LW064B the address lines are A2-A22 and the Data Input/Output is DQ0-DQ31.

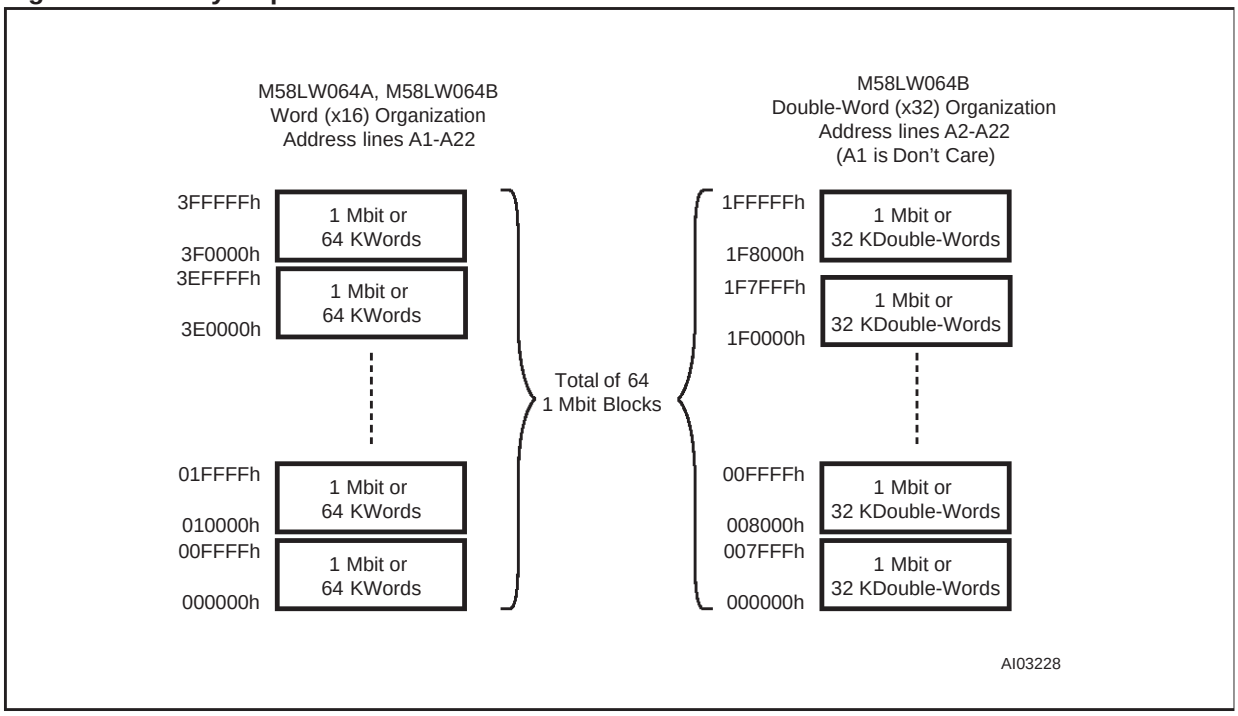
MEMORY BLOCKS

The memory has a uniform block architecture with an array of 64 separate blocks of 1Mbit each. Each block is erased separately. Erase operations are managed automatically by the P/E.C. leaving all of the values in the Block erased to '1'.

Individual block protection against Program or Erase provides additional data security. All blocks are protected during power-up. The protection of the blocks is non-volatile; after power-up the protection status of each block is restored to the state when power last was removed. A software instruction is provided to cancel all block protection bits simultaneously in an application and a higher level input on $\overline{RP}$ can temporarily disable the protection mechanism. A software instruction is provided to allow protection of some or all of the blocks in an application. All Program or Erase operations are blocked when the Program/Erase Enable input, V_{PP}, is Low.

The memory features a software Erase Suspend of a block allowing read or programming within any other block. A suspended Erase operation can be resumed to complete block erasure. A Program Suspend operation on a block allows reading only within any other block. A suspend Program operation can be resumed to complete programming. At any moment of the sequence the Status Register indicates the status of the operation.

Figure 6. Memory Map



SIGNAL DESCRIPTIONS

See Figure 1 and Table 1.

Address Inputs (A1-A22). A1 is used to select between the high and low Word in the x16 configuration of the M58LW064A or M58LW064B; when A1 is Low, V_{IL}, the LSW (Data Inputs/Outputs DQ0-DQ15 of the x32 mode) are output; when A1 is High, V_{IH}, the MSW (Data Inputs/Output DQ16-DQ31 of the x32 mode) are output. A1 is not used in the x32 mode of the M58LW064B.

When Chip Enable, $\overline{E}$, is at V_{IL} the address bus is used to input addresses for the memory array in Read mode, or addresses for the data to be programmed, or to input addresses associated with Commands to be written to the Command Interface. The address latch is transparent when Latch Enable, $\overline{L}$, is at V_{IL}. The address inputs for the memory array are latched on the rising edge of Chip Enable, $\overline{E}$, Latch Enable, $\overline{L}$, or Write Enable, $\overline{W}$, whichever occurs first in a write operation. The address is also internally latched in the command for an Erase or Program Instruction.

Data Inputs/Outputs (DQ0-DQ31). Input data for a Write to Buffer and Program operation and for writing Commands to the Command Interface are latched on the rising edge of Write Enable, $\overline{W}$, or Chip Enable, $\overline{E}$, whichever occurs first.

When Chip Enable, $\overline{E}$, and Output Enable, $\overline{G}$, are at V_{IL} data is output from the Array, the Electronic Signature (the Manufacturer and the Device code), the Block Protection status, the CFI Query information or the Status Register. The data bus is high impedance when the memory is deselected with Chip Enable, $\overline{E}$, at V_{IH}, Output Enable, $\overline{G}$, is at V_{IH}, or $\overline{RP}$ is at V_{IL}. When the P/E.C. is active the Status Register content is output on DQ0-DQ7 and DQ8-DQ31 are at V_{IL}.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, input activates the memory control logic, input buffers, decoders and sense amplifiers. Chip Enable, $\overline{E}$, at V_{IH} deselects the memory and reduces the power consumption to the standby level.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a read operation. When Output Enable, $\overline{G}$, is at V_{IH} the outputs are high impedance. Output Enable, $\overline{G}$, can be used to suspend the data output in a burst read operation.

Write Enable ($\overline{W}$). The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data are latched on the rising edge of, $\overline{W}$, (see also Latch Enable $\overline{L}$).

Reset/Power-down ($\overline{RP}$). The Reset/Power-down input, $\overline{RP}$, provides a hardware reset of the memory and power-down functions. Reset/Power-down of the memory is achieved by pulling $\overline{RP}$ to V_{IL} for at least t_{PLPH}. Writing is inhibited to protect data, the Command Interface and the P/E.C. are reset. The Status Register information is cleared and power consumption is reduced to deep power-down level. The memory acts as deselected and the data outputs are high impedance.

When $\overline{RP}$ rises to V_{IH}, the memory will be available for new operations after a delay of t_{PHQV} and will be configured by default for Asynchronous Random Read. The minimum delay required to access the Command Interface by a write cycle is t_{PHWL}.

If the $\overline{RP}$ input is activated during a Block Erase, a Write to Buffer and Program or a Block Protect/Unprotect operation the cycle is aborted; data is altered and may be corrupted. The Ready/Busy output, $\overline{RB}$, may remain low for a maximum time of t_{PLRH} from the start of the Reset/Power-down, $\overline{RP}$, pulse.

Applying the higher voltage V_{HH} to the Reset/Power-down input, $\overline{RP}$, temporarily unprotects and enables Erase and Program operations on all blocks. Thus it acts as a hardware block unprotect input.

In an application, it is recommended to associate $\overline{RP}$ to the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the memory is performing an Erase or Program cycle, the Flash memory may output the Status Register information instead of being re-initialized to the default Asynchronous Random Read.

Latch Enable ($\overline{L}$). Latch Enable, $\overline{L}$, latches the address bits A1-A22 on its rising edge for the Asynchronous Latch Enable Controlled Read or Write, or Synchronous Burst Read operations. The address latch is transparent when Latch Enable, $\overline{L}$, is at V_{IL}.

Burst Clock (K). The Burst Clock, K, is used only in burst mode. It is the fundamental synchronous signal that allows internal latching of the address from the address bus, together with Latch Enable, $\overline{L}$; increment of the internal address counter in association with Burst Address Advance, $\overline{B}$; and to indicate valid data on the external data bus. All these operations are synchronously controlled on the valid edge of the Burst Clock, K, which can be selected to be the rising or falling edge depending on the definition in the Burst Configuration Register.

For Asynchronous Read or Write, the Burst Clock input, K, is Don't Care. For Synchronous Burst Read the address is latched on the first valid clock edge when Latch Enable, $\overline{L}$, is at V_{IL}, or the rising edge of Latch Enable, $\overline{L}$, whichever occurs first.

Burst Address Advance ($\overline{B}$). Burst Address Advance, $\overline{B}$, enables increment of the internal ad-

dress counter when it falls to V_{IL} during Synchronous Burst Read. It is sampled on the last valid edge of the Burst Clock, K, at the expiry of the X-latency time. If sampled at V_{IL}, new data will be output on the next Burst Clock, K, valid edge (or second next depending on the definition in the Burst Configuration Register). If it is at V_{IH} when sampled, the previous data remains on the Data Outputs. The Burst Address Advance, $\overline{B}$, may be tied to V_{IL}.

Ready (R). The Valid Data Ready, R, is an output signal used during Continuous Synchronous Burst Read operations. During other Bus Operations it is inactive. It indicates, at the valid clock edge (or one cycle before depending on the definition in the Burst Configuration Register), if valid data is ready on the Data Outputs. New Data Outputs are valid if Valid Data Ready, R, is at V_{IH}, the previous Data Outputs remain active if Valid Data Ready, R, is at V_{IL}.

In all operations except Burst Read, Valid Data Ready, R, is at V_{IH}. It may be tied to other components with the same Valid Data Ready, R, signal to create a unique system Ready signal. The Valid Data Ready, R, output has an internal pull-up resistor of around 1 MΩ powered from V_{CCQ}, designers should use an external pull-up resistor of the correct value to meet the external timing requirements for, R, going to V_{IH}.

Word Organization ($\overline{WORD}$). The Word Organization input, $\overline{WORD}$, is present only on the M58LW064B and selects x16 or x32 organization. The $\overline{WORD}$ input selects the data width as Word wide (x16) or Double-Word wide (x32). When $\overline{WORD}$ is at V_{IL}, Word-wide x16 width is selected and data is read and programmed on DQ0-DQ15, DQ16-DQ31 are at high impedance and A1 is the LSB address. When $\overline{WORD}$ is at V_{IH}, the Double-Word wide x32 width is selected and the data is read and programmed on DQ0-DQ31, and A2 is the LSB of the address bus.

Ready/Busy ($R\overline{B}$). Ready/Busy, $R\overline{B}$, is an open-drain output and gives the internal state of the P/E.C. When Ready/Busy, $R\overline{B}$, is at V_{IL} the memory is busy with a Program or Erase operation and it will not accept any additional program or erase instructions except for the Program or Erase Suspend instructions. When a Program or Erase Suspend is given the $R\overline{B}$ signal rises to V_{IH}, after a latency time, to indicate that the Command Interface is ready for a new instruction. When $R\overline{B}$ is at V_{IH}, the memory is ready for any Read, Program or Erase operation. Ready/Busy, $R\overline{B}$, is also at V_{IH} when the memory is in Erase/Program Suspend or Standby modes.

Program/Erase Enable (V_{PP}). Program/Erase Enable, V_{PP}, automatically protects all blocks from programming or erasure when at V_{IL}.

Supply Voltage (V_{CC}). The Supply Voltage, V_{CC}, is the main power supply for all operations (Read, Program and Erase).

A 0.1µF capacitor should be connected between the Supply Voltage, V_{CC}, and the Ground, V_{SS}, to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations, I_{CC4}.

Input/Output Supply Voltage (V_{CCQ}). The Input/Output Supply Voltage, V_{CCQ}, is the Input and Output buffer power supply for all operations (Read, Program and Erase).

A 0.1µF capacitor should be connected between the Supply Voltage, V_{CCQ}, and the Ground, V_{SS}, to decouple the current surges from the power supply.

Ground (V_{SS}). Ground, V_{SS}, is the reference for all the voltage measurements.

BUS OPERATIONS

See Tables 3, 4 and 7.

Address Latch. An address is latched on the rising edge of the Latch Enable input, $\overline{L}$, for Asynchronous Latch Enable Controlled Read. For Asynchronous Latch Enable Controlled Write, the address is latched on the rising edge of Chip Enable, $\overline{E}$, Write Enable, $\overline{W}$, or Latch Enable, $\overline{L}$, whichever occurs first.

For Synchronous Burst Read the address is latched on the first valid Burst Clock edge when Latch Enable, $\overline{L}$, is at Low, or on the rising edge of Latch Enable, $\overline{L}$, whichever occurs first.

Asynchronous Random Read. Asynchronous Random Read outputs the contents of the Array. Both Chip Enable, $\overline{E}$, and Output Enable, $\overline{G}$, must be Low in order to read the output of the memory.

By first writing the appropriate Instruction, the Electronic Signature (RSIG), the Status Register (RSR), the Read Query Instruction (RCFI) or the Block Protection Status (RSIG) can be read.

Asynchronous Random Read is the default read mode that the memory enters on power-up or on return from Reset/Power-down.

Table 3. Asynchronous Bus Operations(1) (M15 = 1(2))

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	M3(2)	$\overline{L}$	A1-A22	DQ0-DQ31
Read	V_{IL}	V_{IL}	V_{IH}	High	0	X	Address	Data Output
					1	V_{IH}	X	
Write	V_{IL}	V_{IH}	V_{IL}	High	X	V_{IL}	Address	Data Input
Latch Address	V_{IL}	V_{IH}	X	High	1	↑	Address	High-Z
Output Disable	V_{IL}	V_{IH}	V_{IH}	High	X	X	X	High Z
Standby	V_{IH}	X	X	High	X	X	X	High Z
Reset/Power-down	X	X	X	V_{IL}	X	X	X	High Z

Note: 1. X = Don't Care V_{IL} or V_{IH}. High = V_{IH} or V_{HH}.
2. Bits M15 and M3 are in the Burst Configuration Register.

Table 4. Synchronous Burst Read Operations(1)(M15 = 0(2))

Operation	$\overline{E}$	$\overline{G}$	$\overline{RP}$	K(3)	$\overline{L}$(4)	$\overline{B}$	A1-A22 DQ0-DQ31
Address Latch	V_{IL}	X	V_{IH}	T	V_{IL}	X	Address Input
Burst Read (no address advance)	V_{IL}	V_{IL}	V_{IH}	T	X	V_{IH}	Data Output
Burst Read (with address advance)	V_{IL}	V_{IL}	V_{IH}	T	X	V_{IL}	Data Output
Burst Read Suspend	V_{IL}	V_{IH}	V_{IH}	X	X	V_{IH}	High Z
Burst Read Resume (no address advance)	V_{IL}	V_{IL}	V_{IH}	T	X	V_{IH}	Data Output
Burst Read Resume (with address advance)	V_{IL}	V_{IL}	V_{IH}	T	X	V_{IL}	Data Output
Burst Read Abort	V_{IH}	X	V_{IH}	X	X	V_{IH}	High Z

Note: 1. X = Don't Care, V_{IL} or V_{IH}.
2. Bit M15 is in the Burst Configuration Register.
3. T = transition, see M6 in the Burst Configuration Register for details on the active edge of K.
4. Where Address Latch, $\overline{L}$, is Don't Care, X, it may be V_{IL} or V_{IH}, but its value must remain constant.

Asynchronous Page Read. Asynchronous Page Read may be used for Random or Latch Enable Controlled Reads of the Array, which are performed independent of the Burst Clock signal. A page has a size of 4 Words or 2 Double-Words and is addressed by the address inputs A1 and A2 in the x16, or A2 only in the x32 organization. Data is read internally and stored in the Page Buffer. The page read starts when both Chip Enable, $\overline{E}$, and Output Enable, $\overline{G}$, are Low. The first data is internally read and is output after the normal access time t_{AVQV}. Successive Words or Double-Words can be read with a much reduced access time of t_{AVQV1} by changing only the low address bits.

Synchronous Burst Read. The memory supports different types of burst access using a Burst Configuration Register to configure the burst type, length and latency.

In continuous burst read, one burst read operation can access the entire memory sequentially by keeping the Burst Address Advance, $\overline{B}$, Low for the appropriate number of clock cycles. At the end of the memory address space the burst read restarts from the beginning at address 000000h.

Synchronous Burst Read is activated when the Burst Clock input, K, is clocking and Chip Enable, $\overline{E}$, is Low. The burst start address is latched and loaded into the internal Burst Address Counter on the valid Burst Clock edge (rising or falling depending on the M6 bit value for the Burst Clock Edge Configuration in the Burst Configuration Register) when Latch Enable, $\overline{L}$, is Low, or upon the rising edge of Latch Enable, $\overline{L}$, when the Burst Clock, K, is valid. After an initial memory latency time, the memory outputs data each clock cycle (or two clock cycles depending on M9 bit value defined in the Burst Configuration Register). The Burst Address Advance input, $\overline{B}$, controls the memory burst output. The second burst output is on the next clock valid edge after the Burst Address Advance, $\overline{B}$, has been pulled Low.

The Valid Data Ready output signal, R, monitors if the memory burst boundary is exceeded and the Burst Controller of the microprocessor needs to insert wait states. When Valid Data Ready, R, is Low on the active clock edge, no new data is available and the memory does not increment the internal address counter at the active clock edge even if Burst Address Advance, $\overline{B}$, is Low.

Synchronous Burst Read will be suspended when Burst Address Advance, $\overline{B}$, is High. The Valid Data Ready signal, R, may be configured (by bit M8 of Burst Configuration Register) to be valid immediately at the valid clock edge or one data cycle before the valid clock edge.

To increase the data throughput the memory has been built with an internal pipelined architecture allowing the user to enter a burst read input command and the next starting address location to be read while the memory is filling the output data bus with its current burst content. This pipelined structure is intended to produce no wait-states on the output data bus for successive burst read mode operations.

Pipelined Burst Read. An overlapping Burst Read operation is possible. That is, the address and data phases of consecutive synchronous read operations can be overlapped by several clock cycles. This is done by applying a pulse on Latch Enable, $\overline{L}$, input to latch a new address before the completion of the data output of the current cycle. This reduces or avoids wait-states in the data output for the burst read mode. The minimum clock edge number for the following read sequence must be six before the last data output of the previous read cycle. The pipelined burst read mode is available in the x16 organization for both burst length definitions of four and eight, and in the x32 organization for the burst length of four. It is not possible for a burst length of one or two

Asynchronous and Latch Enable Controlled Write. Asynchronous Write is used to give commands to the Command Interface for Instructions to the memory or to latch addresses and input data to be programmed. To perform any Instruction the Command Interface is activated starting with a write cycle. A write cycle is also required give the Instruction to clear the Status Register information. Two write cycles are needed to define the Block Erase and the Write to Buffer and Program Instructions. The first write cycle defines the Instruction selection and the second indicates the appropriate block address to be erased for the Block Erase instruction, or the address locations to program with the number of Words or Double-Words in the Write to Buffer and Program Instruction.

An Asynchronous Write is initiated when Chip Enable, $\overline{E}$, Write Enable, $\overline{W}$, and Latch Enable, $\overline{L}$, are Low with Output Enable, $\overline{G}$, High. Commands and Input Data are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first. For an Asynchronous Latch Enable Controlled Write the address is latched on the rising edge of Latch Enable, $\overline{L}$, Write Enable, $\overline{W}$, or Chip Enable, $\overline{E}$, whichever occurs first.

Data to be programmed in the array is internally latched in the Write Buffer before the programming operation starts and a minimum of 4 Words or 2 Double-Words need to be programmed in the same sequence and must be contained in the same address location boundary defined by A1 to A2 for the x16 and A2 for the x32 organization. Write operations are asynchronous and the Burst Clock signal, K, is ignored during a write operation.

Output Disable. The data outputs are high impedance when the Output Enable, $\overline{G}$, is High.

Standby. The memory is in standby when Chip Enable, $\overline{E}$, goes High and the P/E.C. is idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of Output Enable, $\overline{G}$, or Write Enable, $\overline{W}$.

Automatic Low Power. After a short time of bus inactivity (no Chip Enable, $\overline{E}$, Latch Enable, $\overline{L}$, or Address transitions) the chip automatically enters a pseudo-standby mode where consumption is reduced to the Automatic Low Power standby value, while the outputs may still drive the bus. The Automatic Low Power feature is available only for Asynchronous Read.

Power-down. The memory is in Power-down when Reset/Power-down, $\overline{RP}$, is Low. The power consumption is reduced to the power-down level and the outputs are high impedance, independent of Chip Enable, $\overline{E}$, Output Enable, $\overline{G}$, or Write Enable, $\overline{W}$.

Table 5. Burst Type Definition (x16 mode)

Burst Length	Starting Address (binary)	Sequential (decimal)	Interleaved (decimal)
	A3-A2-A1		
2	0-0-0	0-1	0-1
	0-0-1	1-0	1-0
4	0-0-0	0-1-2-3	0-1-2-3
	0-0-1	1-2-3-0	1-0-3-2
	0-1-0	2-3-0-1	2-3-0-1
	0-1-1	3-0-1-2	3-2-1-0
8	0-0-0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0-0-1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0-1-0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0-1-1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1-0-0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1-0-1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1-1-0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1-1-1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Table 6. Burst Type Definition (x32 mode)

Burst Length	Starting Address (binary)	Sequential (decimal)	Interleaved (decimal)
	A2-A1		
2	0-0	0-1	0-1
	0-1	1-0	1-0
4	0-0	0-1-2-3	0-1-2-3
	0-1	1-2-3-0	1-0-3-2
	1-0	2-3-0-1	2-3-0-1
	1-1	3-0-1-2	3-2-1-0

INITIALIZATION

The memory must be powered up and initialized in a predefined manner. Procedures other than specified may result in undefined operation.

Power should be applied to V_{CC} and V_{CCQ} at the same time with the $\overline{RP}$ input held Low. When the supplies are stable $\overline{RP}$ can be taken High. Output Enable, $\overline{G}$, Chip Enable, $\overline{E}$, and Write Enable, $\overline{W}$, should also be held High during power-up. The memory will be ready to accept the first Instruction after the power-up time t_{PHW}. The memory is automatically configured for Asynchronous Random Read at power-up or after leaving Reset/Power-down.

BURST CONFIGURATION REGISTER

See Tables 8, 9, 10 and 11.

The Synchronous Burst Read, Asynchronous Random Read, Asynchronous Latch Enable Controlled Read are selected using the Burst Configuration Register.

For Synchronous Read the register defines the X and Y Latencies, Valid Data Ready signal timing, Burst Type, Valid Clock Edge and Burst Length. The Burst Configuration Register is programmed using the Set Burst Configuration Register (SBCR) Instruction and will retain the stored information until it is programmed again or the memory is reset or goes into the Reset/Power-down.

The Burst Configuration Register bits M2-M0 specify the burst length (1, 2, 4, 8 or continuous); bit M3 specifies Asynchronous Random Read or Asynchronous Latch Enable Controlled Read; bits M4 and M5 are not used; bit M6 specifies the rising or falling burst clock edge as valid; bit M7 specifies the burst type (Sequential or Interleaved); M8 specifies the Valid Data Ready output period; bit M9 specifies the Y-latency; bit M10 is not used; M14-M11 specify the X-latency; and bit M15 selects between Synchronous Burst Read or Asynchronous Read. M10, M5 and M4 are reserved for future use.

M15 Read Select

The memory features three kinds of read operation: Asynchronous Random Read, Asynchronous Latch Enable Controlled Read and Synchronous Burst Read. Page Read may be used in either of the Asynchronous Read operations.

The Burst Configuration Register bit M15 selects between Synchronous Burst and Asynchronous Read.

M14-M11 and M9 X and Y Latency

The values of X and Y are used to define the burst latency for the data sequence. The X-latency defines the number of clock cycles before the output of the first data from the clock edge that latches the address. The X-latency can be set from 7 to 16. A value of 7 is only valid for continuous burst.

The Y-latency is the number of clock cycles needed to output the next data from the burst register, following the first data output. The latency can be set to 1 or 2 clock cycles.

The minimum X-Latency value to consider depends on the frequency of the Burst Clock signal, K. The burst performance in terms of frequency is listed in Table 11 and indicates the minimum X-latency and Y-latency values (X.Y.Y.Y) related to the burst type, burst length and x16 or x32 organization.

M8 Valid Data Ready R Signal Configuration

During Continuous Synchronous Burst Read operations the Valid Data Ready R output signal indicates when valid data is on the data outputs synchronous with the valid burst clock edge. It can be asserted by the memory synchronously with the valid clock edge or one clock cycle before.

M7 Burst Type

Accesses within a given burst may be programmed to be either Sequential or Interleaved. This is referred to as the burst type and is selected by the Burst Configuration Register M7 bit. The access order within a burst is determined by the burst length, the burst type and the starting address (See Table 8).

M6 Valid Clock Edge Configuration

All the synchronous operations such as Burst Read, Output Data or Ready signal validation can be synchronized on the valid rising or on the falling edge of the Burst Clock signal, K.

Table 7. Burst Configuration Register (1)

BCR mode bit	Description	Value	Description
M15	Read Select	0	Synchronous Burst Read
		1	Asynchronous Read
M14-M11	X-Latency (3)	0001	Reserved
		0010	7, only for F_K = 33MHz (4)
		0011	8, only for F_K = 33MHz
		0100	9, only for F_K = 33MHz
		0101	10, only for F_K = 50MHz (5)
		0110	11, only for F_K = 50MHz (6)
		1001	12, only for F_K = 50MHz
		1010	13, only for F_K = 50MHz
		1011	14, only for F_K = 66MHz (7)
		1101	16, only for F_K = 66MHz
M9	Y-Latency (3)	0	One Burst Clock cycle
		1	Two Burst Clock cycles
M8	Valid Data Ready	0	R valid Low during valid Burst Clock edge
		1	R valid Low one data cycle before valid Burst Clock edge
M7	Burst Type	0	Interleaved
		1	Sequential
M6	Valid Clock Edge	0	Falling Burst Clock edge
		1	Rising Burst Clock edge
M3	Asynchronous	0	Random Read
		1	Latch Enable Controlled Read
M2-M0	Burst Length (2)	100	1 Word or Double-Word
		101	2 Words or Double-Words
		001	4 Words or Double-Words
		010	8 Words
		111	Continuous

Note: 1. The BCR defines both the read mode and the burst configuration.
2. Synchronous burst length is defined as Word or Double-Word, the data bus width depends only on the $\overline{WORD}$ input. Asynchronous Page read is two Words or one Double-Word.
3. At F_K > 50MHz when X-Latency = 10 or 12, Y-Latency = 2 independent of the value of M9. At F_K = 66MHz when X-Latency = 14 or 16, Y-Latency = 2 independent of the value of M9.
4. Latency 7 valid only for continuous burst. Otherwise Latency = 8.
5. Latency 10 valid only for continuous burst. Otherwise Latency = 12.
6. Latency 11 valid only for continuous burst. Otherwise Latency = 12.
7. Latency 14 valid only for continuous burst. Otherwise Latency = 16.

Table 8. Burst Performance (1)

X-Y Latencies (minimum)						Clock Frequency
x16 organization		x32 organization		x16 organization	x32 organization	
Sequential	Interleaved	Sequential	Interleaved	V_{CC} = 2.7 to 3.6V		
Burst length: 1,2,4,8	Burst length: 1,2,4,8	Burst length: 1,2,4	Burst length: 1,2,4	Continuous Burst		
8.1.1.1	8.1.1.1	8.1.1.1	8.1.1.1	7.1.1.1	7.1.1.1	≤ 33 MHz
12.1.1.1	12.1.1.1	12.1.1.1	12.1.1.1	10.1.1.1	10.1.1.1	≤ 50 MHz
t.b.a.	t.b.a.	t.b.a.	t.b.a.	t.b.a.	t.b.a.	≤ 60 MHz
16.2.2.2	16.2.2.2	16.2.2.2	16.2.2.2	14.2.2.2	14.2.2.2	≤ 66 MHz

Note: 1. The burst length of 8 is not available in the x32 organization.

M2-M0 Burst Length

Synchronous reads have a programmable burst length, set using the M2 - M0 bits of the Burst Configuration Register. The burst length corresponds to the maximum number of Words or Double-Words that can be output. Burst lengths of 1, 2, 4 or 8 are available for both the Sequential and Interleaved burst types, and a continuous burst is available for the Sequential type. The burst length of 8 is not available in the x32 configuration.

When a Read command is issued, a block of Words or Double-Words equal to the burst length is selected. All accesses for that burst take place within this block, meaning that the burst wraps within the burst block if a boundary is reached.

If a Continuous Burst Read has been initiated the memory will output data synchronously. Depending on the starting address of the read, the memory activates the Valid Data Ready output, R, to indicate that it needs a delay to complete the internal read operation before outputting data. If the starting address is aligned to a four Word boundary the continuous burst mode will run without activating the Valid Data Ready R output. If the starting address is not aligned to a four Word boundary, Valid Data Ready R is activated at the beginning of the continuous burst read to indicate that the memory needs an internal delay to read the content of the four successive words in the array.

INSTRUCTIONS AND COMMANDS

The Command Interface latches commands written to the memory. Instructions are made up of one or more commands to perform:

- Read Array (RD),
- Read Electronic Signature or Read Block Protection (RSIG),
- Read Status Register (RSR),
- Read Query (RCFI),
- Clear Status Register (CLRS),
- Block Erase (EE),
- Write to Buffer and Program (WBPR),
- Erase/Program Suspend (PES),
- Erase/Program Resume (PER),
- Set Burst Configuration Register (SBCR),
- Block Protect (BP), and
- Block Unprotect (BU).

Instructions (see Table 9) are composed of a first write sequence followed by either a second write sequence needed to confirm an Erase or Program instruction or by a read operation in order to read data from the array, the Electronic Signature, the Block Protection information, the CFI or the Status Register information. The instructions for Write to Buffer and Program and Block Erase operations consist of two commands written into the memory Command Interface (C.I.) that start the automatic P/E.C. operation. Erasure of a memory block may be suspended, in order to read data from or to program data in an other block, and then be resumed. Write to Buffer and Program operation may be suspended, in order to read data from another block, and then be resumed.

At power-up the Command Interface is reset to Read Array. The appropriate Instruction must be given to access Read Query (RCFI), Read Electronic Signature or Block Protection Status (RSIG) or Read Status Register (RSR). Reading of the memory array is disabled during a Block Protect/ Unprotect (BP, BU), a Block Erase (EE) or a Write to Buffer and Program (WBPR) Instruction. A Erase/Program Suspend Instruction (PES) must be given to read under these conditions.

Read Array Instruction (RD). The Read Array Instruction consists of one write cycle giving the command FFh. Subsequent read operations will read the array content addressed and output the corresponding data. The Read Array Instruction remains active until another one is written into the Command Interface. At Power-up or at the exit of the Reset/Power-down mode, the memory is by default initialized to Read Array.

Read Electronic Signature Instruction (RSIG).

An Electronic Signature can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of the memory. The Electronic Signature instruction consists of a first write cycle giving the command 90h, followed by a subsequent read which will output the Manufacturer Code, the Device Code or the Block Protection Status. The Manufacturer Code is output when all the address inputs are at VIL. The Device Code is output when A1 (for the M58LW064A) or A2 (for the M58LW064B) is at V_{IH}, with all other address inputs at V_{IL}. The code is output on DQ0-DQ7 with DQ8-DQ31 at V_{IL}.

The RSIG Instruction also allows access to the Block Protection Status for the selected block address defined by A17-A22. After the Read Electronic Signature (RSIG) command, A1-A2 (for the M58LW064A) or A2-A3 (for the M58LW064B) are set to V_{IH}, while A17-A22 define the address of the block to be queried. A read operation outputs 01h if the block is protected and 00h if the block is not protected.

Read Query Instruction (RCFI). The Read Query Instruction is initiated with one write cycle giving the command 98h at any address. Subsequent read operations, depending on the address specified, will output the Block Status information, the Common Flash Interface ID string, the System Interface information, the Device Geometry Configuration or STMicroelectronics Specific Query information. The address mapping for the information is shown in Table 14.

Read Status Register Instruction (RSR). The Read Status Register Instruction consists of one write cycle giving the command 70h. Subsequent read operations, independent of the address, output the Status Register information that indicates if a Block Erase, Write to Buffer and Program, Block Protect or Block Unprotect operation has been completed successfully. See Table 12. Once initiated the RSR Instruction is active until another command is given to the Command Interface.

For Asynchronous Read, the Status Register information is present on the output data bus when both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are Low. An interactive update of the status register information is possible by toggling Output Enable $\overline{G}$, or when the memory is deactivated by Chip Enable $\overline{E}$ High and then reactivated by Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ Low, during an Erase or Program operation. The content of Status Register may also be read at the completion of an Erase/Program and/or Suspend operation.During a Block Erase, Write to Buffer and Program, Block Protect or Block Unprotect Instruction, DQ7 indicates the P/E.C. status. It is valid until the operation is completed or suspended, DQ0-DQ7 output the Status Register content and DQ8-DQ31 are Low. The Status Register should only be read using asynchronous bus operations. It is not available through synchronous bus operations.

Table 9. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle			Comments
			Op.	Address	Data	Op.	Address	Data	
RD	Read Array	1+	Write	X	FFh				Read Array until a new write cycle is initiated
RSIG	Read Manufacturer Code	≥ 2	Write	X	90h	Read	000000h	20h	Read Manufacturer Code
RSIG	Read Device Code or Block Protection Status	≥ 2	Write	X	90h	Read	IAh	IDh	Read Device ID Code
RSR	Read Status Register	2	Write	X	70h	Read	X	SRDh	SRD = Status Register Data
RCFI	Read Query	≥ 2	Write	X	98h	Read	QAh	QDh	QA = Query Address QD = Query Data
CLRS	Clear Status Register	1	Write	X	50h				
EE	Block Erase	2	Write	X	20h	Write	BAh	D0h	BA = Block Address to erase
WBPR	Write to Buffer and Program	≥ 2	Write	BAh	E8h	Write	BAh	N	BA = Block Address N = Word/Double-Word Count Argument
PES	Erase/ Program Suspend	1	Write	X	B0h				
PER	Erase/ Program Resume	1	Write	X	D0h				Confirm command for Write to Buffer and Program instruction
SBCR	Set Burst Configuration Register	2	Write	BCRh	60h	Write	BCRh	03h	BCR = Burst Configuration Register
BP	Block Protect	2	Write	BAh	60h	Write	BAh	01h	Keep the Block Protect bit active of the selected block BA = Block Address
BU	Block Unprotect	2	Write	X	60h	Write	X	D0h	Clear all the Block protect bits simultaneously

Table 10. Status Register Definition

Mnemonic	DQ	Function	Status
P/ECS	DQ7	P/E.C. Status	1 = Ready 0 = Busy (1)
ESS	DQ6	Erase Suspend Status	1 = Block Erase Suspended 0 = Block Erase in Progress/Completed (2)
ES	DQ5	Erase/Block Unprotect Status (7)	1 = Error in Block Erase operation or Block Unprotect 0 = Successful Block Erase operation or Block Unprotect (3)
PS	DQ4	Write to Buffer and Program/Block Protect Status (7)	1 = Error in Write to Buffer and Program, Block Protect (4) 0 = Write to Buffer and Program, Block Protect Completed successfully
PVS	DQ3	Program Voltage Status	1 = Error in V_{PP} level, Hardware programming/ erase protection 0 = Operation in Progress/Completed
PSS	DQ2	Program Suspend Status	1 = Program Suspended 0 = Program operation in Progress/Completed (5)
EPPB	DQ1	Erase/Write to Buffer and Program in a Protected Block	1 = Error in the defined operation 0 = Operation in Progress/Completed (6)
	DQ0	Not used	

Note: 1. DQ0-DQ6 are High Impedance when DQ7 is indicating that the part is busy. Status Register P/ECS bit7 indicates the P/E.C. status, check during Program or Erase, and on completion before checking bit4 or bit5 for Program or Erase Success.
2. DQ6 indicates the Erase Suspend Status. On an Erase Suspend instruction P/ECS and ESS bits are set to '1'. ESS bit remains '1' until an Erase Resume instruction is given.
3. Erase Status, ES bit5 is set to '1' if the P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
4. Program Status, PS bit4 is set to '1' if the P/E.C. has failed to program a Word or Double-Word.
5. DQ2 indicates the Program Suspend Status. On a Program Suspend instruction P/ECS and PSS bits are set to '1'. PSS bit remains '1' until an Program Resume instruction is given.
6. DQ1 defines the status of an Erase or Write to Buffer and Program instruction defined in a protected block. $\overline{RP}$ pin must be held at V_{HH} to temporarily override the block protect feature once it has been enabled.
7. DQ5 and DQ4 simultaneously at '1' after an Erase or Block Unprotect instruction indicates that an improper command was entered.

Clear Status Register Instruction (CLRS). The Clear Status Register Instruction is given with the command 50h at any address location. It is a reset instruction that resets DQ5, DQ4 and DQ1 in the Status Register to '0'.

If an operation such as Block Erase, Write to Buffer and Program Block Protect or Block Unprotect has failed, the P/E.C. will set DQ5, DQ4 or DQ1 to '1' depending on the failure detected (see Table 12, Status Register Definition). The Clear Status Register Instruction must be given before restarting any corrective Erase/Program Instruction. The CLRS Instruction should be given also after an Erase or Program Suspend Instruction failure or before a Resume Instruction if the previous instruction has been detected to have failed. It is also a software reset solution that may allow the execution of several operations such as cumulated Erase or Block Protect operations of multiple blocks. The Clear Status Register instruction is valid when the P/E.C. is inactive or the memory is in a suspend mode and it is also valid independent of the voltage V_{IH} or V_{HH} applied on the $\overline{RP}$ input.

Write to Buffer and Program Instruction (WB-PR). The Write to Buffer and Program Instruction is used to program the memory array. Up to 16 Words or 8 Double-Words can be loaded into the Write Buffer and programmed into the memory.

The memory is always programmed one page at a time, where a page is 4 words with A3-A22 constant. After a page is programmed it cannot be reprogrammed successfully until it has been erased. This applies even if only part of the page is programmed; although the other words appear in the erased state they cannot be successfully programmed until the block containing the page has been erased.

The Write to buffer and Program Instruction is composed of four successive steps. The first step is to give the Write to Buffer and Program command, E8h with the selected memory Block Address where the program operation should occur. The second step is to write the block address again, along with the value N, where N+1 is the number of Words (x16 organization) or Double-Words (x32 organization) to be programmed. In the third step, a sequence of N+1 write cycles loads the addresses and data to the write buffer (see boundary constraints below). The addresses must lie between the starting address and the starting address + (N+1). Finally, in the fourth step the Confirm Command, D0h (the same as Erase/ Program Resume PER Instruction) needs to be given immediately after the completion of the Write to Buffer and Program Instruction.

Following Write to Buffer and Program instruction Read operations read the Status Register. The Status Register can only be read using asynchronous bus operations. It is not available through synchronous bus operations.

The array must be programmed in 4 Word or 2 Double-Word blocks, which must be aligned with an A2 = A1 = 0 starting address (or A2 = 0 for x32 organization). Invalid data will be flagged and the operation will abort with the status register bits DQ4 and DQ5 set to 1.

The P/E.C. is enabled only if the whole previous sequence is fully respected. Otherwise an Invalid Command/Sequence error will be generated with the Status Register DQ5 and DQ4 set to '1'. For additional Write to Buffer and Program operations, after the initial input command the software can check the availability of the write buffer by checking DQ7 status from the Status Register.

If an error appears during a program sequence, the memory will stop its operation and DQ4 of the Status Register will be set to '1' to indicate a program failure. DQ5 will indicate if an error has been detected during a Block Erase operation. If these bits, DQ4 or DQ5 are set to '1', the Write to Buffer and Program input command is not accepted by the memory until the status register has been cleared.

Additionally, if the Block is protected and $V_{IH} < \overline{RP} < V_{HH}$ instead of $\overline{RP} = V_{HH}$, the Write to Buffer and Program Instruction will not be accepted by the memory, and DQ4 and DQ1 of the status register will be set to '1'.

Block Protect Instruction (BP). The Block Protect Instruction BP uses a two-cycle write sequence. The first write cycle gives the command 60h to any address in the block to be protected. The second write cycle gives the block address memory location to be protected and the command 01h.

Block protection can be cleared with the BU Instruction, which unprotects all blocks. Alternatively, temporary unprotect can be achieved by raising the $\overline{RP}$ input to V_{HH} and holding it at that level throughout the Block Erase or Write to Buffer and Program operations.

Block Unprotect Instruction (BU). The Block Unprotect Instruction BU uses a two-cycle write sequence. All the Block Protect bits are simultaneously erased. The Block Protect bit register is erased by giving the command 60h and then the Confirm command D0h, at any address location. The sequence is aborted if the Confirm command is not given and the memory will output the Status Register Data with DQ4 and DQ5 set to '1'.

Block Erase Instruction (EE). The Block Erase Instruction EE uses a two-cycle command sequence. The Erase Setup command 20h is written to any address location. Then a second write cycle is given with the block address to be erased and the Confirm command D0h. The sequence is aborted if the Confirm command is not given and the memory will output the Status Register Data with DQ4 and DQ5 set to '1'.

During the execution of the erase cycle by the P/ E.C., the memory accepts only the Erase/Program Suspend instructions. Read operations output the Status Register bits. A complete state of the erase operation is given by the Status Register bits.

Erase/Program Suspend Instruction (PES).

The Block Erase or Write to Buffer and Program operations may be suspended by writing the command B0h at any address. The Erase/Program Suspend Instruction interrupts the P/E.C. Erase or Program sequence at a predetermined point in the algorithm. After the Suspend command is written the memory outputs the Status Register data.

It is possible to read or program data in a block other than the one in which the Erase Suspend operation is effective. It is only possible to read in a block other than the one in which a Program Suspend operation is effective. The suspended Erase/ Program operation has to be resumed in order to complete the previous erase/program sequence.

The Erase Suspend instruction is accepted only during a Block Erase operation execution. Program Suspend also is valid only during the Write to Buffer and Program instruction execution. Block Erase or Erase/Program Suspend instructions are ignored if the memory is already in the Suspend mode.

The Suspend Instruction may be presented at any time during the execution of a Block Erase. For a Write to Buffer and Program instruction the Suspend Instruction is accepted only when the P/E.C. is running.

The memory outputs information about the suspend in the Status Register information on DQ7, DQ6 and DQ2. If the operation has been completed DQ7 = '1' and DQ6 = '0' (Erase Suspend) or DQ2 = '0' (Program Suspend).

If the Suspend instruction occurred after the P/E.C. has completed its operation (DQ7 = 1, DQ6 = 0 and DQ2 = 0), the Status Register information remains available by toggling Output Enable $\overline{G}$. No command is accepted by the memory with the exception of a Read Memory Array Instruction FFh. After the FFh Command is issued, the memory is ready for Read Array (in the mode defined by the last Set Configuration Register issued).

When a program operation is completed inside a Block Erase Suspend Instruction, Read Array Instruction FFh will reset the memory to Read Array. The Erase Resume Instruction has to be issued to complete the whole sequence.

When erase is suspended, the memory will respond only to the Read Array, Read Electronic Signature, Read Query, Read Status Register, Clear Status Register, Erase/Program Resume and the Write to Buffer and Program instructions.

When a Write to Buffer and Program instruction is suspended, the memory will respond only to the Read Array, Read Electronic Signature, Read Query, Read Status Register, Clear Status Register and Erase/Program Resume instructions.

Erase/Program Resume Instruction (PER). If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command D0h, at any address. This also serves as the Confirm command for the Write to Buffer and Program (WPBR) Instruction which is issued after the write buffer loading sequence is completed, and which starts the P/E.C.

Set Burst Configuration Register (SBCR). This instruction uses two command cycles. The Burst Configuration Setup command 60h is written with the address corresponding to the Set Burst Configuration Register content. Then in the second write cycle the address bus A2-A17 specifies the BCR, Burst Configuration Register, information and the command 03h. The burst length, type, latency, synchronous/asynchronous read mode and clock edge active configuration are defined in that operation. After the command 03h the memory will default in the Read array mode.

Status Register Bits. The P/E.C. status is indicated during execution with a Ready/Busy output available on DQ7. Any read attempt during Program or Erase command execution will automatically update the Status Register bits. The P/E.C. automatically sets bits DQ1, DQ2, DQ4, DQ5, DQ6 and DQ7. The bit DQ0 is reserved for future use and should be masked. It is not necessary to specify an address when the Status Register bits are read. The Status Register is a static memory register that is reset when RP signal is active or on a power-down operation.

POWER SUPPLY

Power Down. The memory provides Reset/Power-down control using the input $\overline{RP}$. When Reset/Power-down $\overline{RP}$ is pulled to VIL the supply current drops to typically less than 1µA, the memory is deselected and the outputs are at high impedance. If $\overline{RP}$ is pulled to V_{IL} during a Program or Erase operation, this operation is aborted after a latency time of t_{PLRH} and the memory content is no longer valid.

RESET, POWER-DOWN AND POWER-UP

See Figure 16.

The memory is reset if the Reset/Power-down $\overline{RP}$ input is pulled to V_{IL} for longer than tPLPH. If the memory was in a Read mode then it will recover from reset after a time of t_{PHQV} to give valid data output. If the memory was executing an Erase or Program operation, with the P/E.C. active, the operation will abort in a time of t_{PLRH} maximum. The memory will be ready to accept new write commends after a time of t_{PHWL} or t_{PHEL}.

The supply voltages V_{CC} and V_{CCQ} must be high a time t_{VDHEL} or t_{VDHWL} before a read or write cycle. At first power up Reset/Power-down should be held Low for a time of t_{VDHPH} after V_{CC} and V_{CCQ} are high. The memory will be ready to accept its first read or write commands after a time of t_{PHR} or t_{PHW}.

COMMON FLASH INTERFACE - CFI

The introduction to the JEDEC CFI specification Rel. 1.2 quotes, "The Common Flash Interface (CFI) specification outlines a device and host system software interrogation handshake which allows specific software algorithms to be used for entire families of devices. This allows device-independent, JEDEC, ID independent and forward- and backward-compatible software support for the specified flash memory families. It allows flash vendors to standardize their existing interfaces for long-term compatibility."

The CFI Query instruction RCFI describes how the memory enters the CFI Query mode which enables information to be read from the Flash memory. CFI allows a system software to query the flash memory to determine various electrical and timing parameters, density information and functions supported by the memory. CFI allows the system to easily interface to the flash memory, to learn about its features and parameters, enabling the software to upgrade itself when necessary.

Query Structure Overview

The flash memory displays the CFI data structure when the CFI Query Instruction RCFI is issued. A list of the main subsections is detailed in Tables 11 to 16.

Table 11. Query Structure Overview

Offset	Sub-section Name	Description
00h		Manufacturer Code
01h		Device Code
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing and voltage information
27h	Device Geometry Definition	Flash memory layout
P(h)	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A(h)	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)
(BA+3)h	Block Status Register	Block-related Information

Table 12. CFI - Query Address and Data Output in the x16/x32 organization

Address (4) A22-A1 (M58LW064A) A22-A2 (M58LW064B)	Data		Instruction
10h	51h	"Q"	Query ASCII String 51h; "Q" 52h; "R" 59h; "Y"
11h	52h	"R"	
12h	59h	"Y"	
13h	20h		Primary Vendor: Command Set and Control Interface ID Code
14h	00h		
15h	31h		Primary algorithm extended Query Address Table: P(h)
16h	00h		
17h	00h		Alternate Vendor: Command Set and Control Interface ID Code
18h	00h		
19h	31h		Alternate Algorithm Extended Query address Table
1Ah	00h		

Note: 1. The x8 or Byte Address mode is not available.
2. In the x16 organization, the value of the address location of the CFI Query is independent of A1 pad (M58LW064B).
3. Query Data are always presented on the lowest order data outputs (DQ7-DQ0) only. Others data (DQ31-DQ8) are set to '0'.
4. For M58LW064B, A1 = Don't Care.

Table 13. CFI - Device Voltage and Timing Specification

Address (4) A22-A1 (M58LW064A) A22-A2 (M58LW064B)	Data	Instruction
1Bh	27h (1)	V_{CC} Min, 2.7V
1Ch	36h (1)	V_{CC} max, 3.6V
1Dh	00h (2)	V_{PP} min – Not Available
1Eh	00h (2)	V_{PP} max – Not Available
1Fh	00h (3)	2^N ms Word, DWord prog. typical time-out
20h	07h	2^N ms, typical time out for max buffer write
21h	0Ah	2^N ms, Erase Block typical time-out
22h	00h (3)	2^N ms, chip erase time-out typ. – Not Available
23h	00h (3)	2^N times typ. for Word Dword time-out max – Not Available
24h	04h	2^N times typ. for buffer write time-out max
25h	04h	2^N x typ. individual block erase time-out maximum
26h	00h (3)	2^N times typ. for chip erase max time-out – Not Available

Note: 1. Bits are coded in Binary Code Decimal, bit7 to bit4 are scaled in Volt and bit3 to bit0 in mV.
2. Bit7 to bit4 are coded in Hexadecimal and scaled in Volt while bit3 to bit0 are in Binary Code Decimal and scaled in 100mV.
3. Not supported.
4. For M58LW064B, A1 = Don't Care.

Table 14. Device Geometry Definition

Address (1) A22-A1 (M58LW064A) A22-A2 (M58LW064B)	Data	Instruction
27h	17h	2^N number of bytes memory Size
28h	01h.	Device Interface Sync./Async.
29h	00h	Organization Sync./Async.
2Ah	05h	Page size in bytes, 2^N
2Bh	00h	
2Ch	01h	Bit7-0 = number of Erase Block region
2Dh	3Fh	Number (N-1) of Erase Blocks of identical size; N=64
2Eh	00h	
2Fh	00h	x times 256 bytes per Erase block (128K bytes)
30h	02h	

Note: 1. For M58LW064B, A1 = Don't Care.

Table 15. Block Status Register

Address A22-A2	Data (Hex) x32 organization		Selected Block Information
(BA+3)h[1]	bit0	0	Block Unlocked
		1	Block Locked
	bit1	0	Last erase operation ended successfully [2]
		1	Last erase operation not ended successfully [2]
	bit7-2	0	Reserved for future features

Note: 1. BA specifies the block address location, i-e, A22-A17.
2. Not Supported.

Table 16. Extended Query information

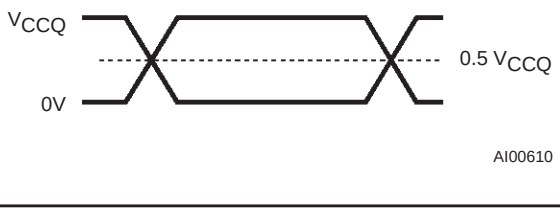
	M58LW064B - x32 M58LW064A - x16			M58LW064B - x16 organization		Instruction
Address offset	Address A22-A2	Data (Hex) x32 organization		Address A22-A1	Data	
(P)h	31h	50h	"P"	62h, 63h	50h	Query ASCII string - Extended Table
(P+1)h	32h	52h	"R"	64h, 65h	52h	
(P+2)h	33h	49h	"Y"	66h, 67h	49h	
(P+3)h	34h	31h		68h, 69h	31h	Major version number
(P+4)h	35h	31h		6Ah, 6Bh	31h	Minor version number
(P+5)h	36h	0Eh		6Ch, 6Dh	0Eh	Optional Feature: (1=yes, 0=no) bit0, Chip Erase Supported (0=no) bit1, Suspend Erase Supported (1=yes) bit2, Suspend Program Supported (1=yes) bit3, Lock/Unlock Supported (1=yes) bit4, Queue Erase Supported (0=no) Bit 31-5 reserved for future use
(P+6)h	37h	00h		6Eh, 6Fh	00h	Optional Features
(P+7)h	38h	00h		70h, 71h	00h	
(P+8)h	39h	00h		72h, 73h	00h	
(P+9)h	3Ah	01h		74h, 75h	00h	Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h	3Bh	00h [2]		76h, 77h	00h [2]	Block Status Register Mask
(P+C)h	3Ch	33h		78h, 79h	33h	V_{CC} OPTIMUM Program/Erase voltage conditions
(P+D)h	3Dh	50h		7Ah, 7Bh	50h	V_{PP} OPTIMUM Program/Erase voltage conditions
(P+E)h	3Eh	00h		7Ch, 7Dh	00h	Reserved for future use
(P+F)h	3Fh	00h		7Dh, 7Fh	00h	Reserved for future use

Note: 1. Bit7 to bit4 are coded in Hexadecimal and scaled in Volt while bit3 to bit0 are in Binary Code Decimal and scaled in mV.
2. Not supported.

Table 17. AC Measurement Conditions

Clock Rise and Fall Times	≤3ns
Input Rise and Fall Times	≤4ns
Input Pulses Voltages	0V to V_{CCQ}
Input and Output Timing Ref. Voltages	$V_{CCQ}/2$

Figure 7. AC Testing Input Output Waveform



Note: $V_{CC} = V_{CCQ}$.

Figure 8. AC Testing Load Circuit

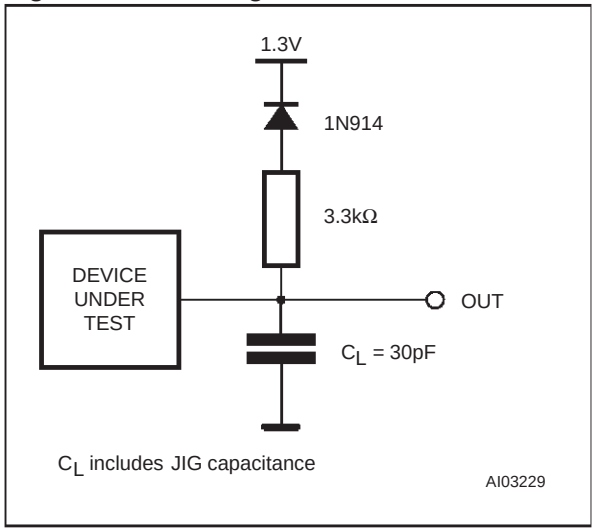


Table 18. Capacitance (T_A = 25°C, f = 1 MHz)

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Table 19. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C, V_{CC} = 2.7V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CCQ}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CCQ}$		±5	µA
I_{CC}	Supply Current (Random Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{add} = 6MHz		30	mA
I_{CCB}	Supply Current (Burst Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{clock} = 50MHz		50	mA
I_{CC1}	Supply Current (Standby)	$\overline{E} = V_{CCQ} \pm 0.2V$, $\overline{RP} = V_{CCQ} \pm 0.2V$		40	µA
I_{CC5}	Supply Current (Auto Low-Power)	$\overline{E} = V_{SS} \pm 0.2V$, $\overline{RP} = V_{CCQ} \pm 0.2V$		2	mA
I_{CC2}	Supply Current (Reset/Power-down)	$\overline{RP} = V_{SS} \pm 0.2V$		1	µA
I_{CC3} (1)	Supply Current (Program or Erase, Set Lock Bit, Erase Lock Bit)	Write to Buffer and program Block Erase in progress		30	mA
I_{CC4}	Supply Current (Erase/Program Suspend)	$\overline{E} = V_{IH}$		40	µA
V_{IL}	Input Low Voltage		–0.5	0.4	V
V_{IH}	Input High Voltage		V_{CCQ} –0.4	V_{CCQ} +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA		0.1	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CCQ} –0.1		V
V_{HH} (2)	$\overline{RP}$ Hardware Block Unlock Voltage	Block Erase in progress, Write to Buffer and Program	8.5	9.5	V
V_{LKO}	V_{CC} Supply Voltage (Erase and Program lockout)			2.2	V

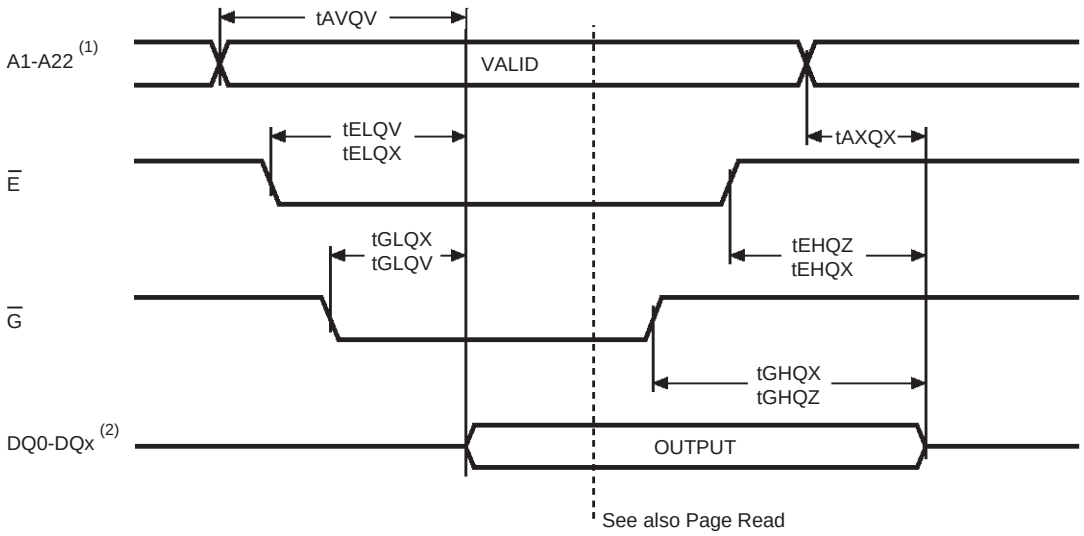
Note: 1. Sampled only, not 100% tested.
2. Biasing $\overline{RP}$ pin to V_{HH} is allowed for a maximum cumulative period of 80 hours.

Table 20. Asynchronous Random Read
(T_A = 0 to 70°C, –40 to 85°C, V_{CC} = 2.7V to 3.6V, V_{CCQ} = 1.8V to V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{AVAV}	Address Valid to Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	150		ns
t_{AVQV}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		150	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		ns
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		10	ns
t_{ELQV}(1)	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		150	ns
t_{ELQX}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		10	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50	ns
t_{GLQX}	Output Enable to Output Transition	$\overline{E}$ = V_{IL}	0		ns

Note: 1. Output Enable $\overline{G}$ may be delayed up to t_{ELQV} - t_{GLQV} after the falling edge of Chip Enable $\overline{E}$ without increasing t_{ELQV}.

Figure 9. Asynchronous Random Read AC Waveforms
Asynchronous Read (M15 = 1), Random (M3 = 0)



(1) A1 is not used (Don't Care) in x32 organization
(2) DQ0-DQ15 in x16 or DQ0-DQ31 in x32 organization

AI03250

Table 21. Asynchronous Latch Enable Controlled Read and Page Read
(T_A = 0 to 70°C, –40 to 85°C, V_{CC} = 2.7V to 3.6V, V_{CCQ} = 1.8V to V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{AVLL}	Address Valid to Latch Enable Low	$\overline{E} = V_{IL}$	10		ns
t_{AVQV1}	Address Valid to Output Valid (Page Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		25	ns
t_{AXQX}	Address Transition to Output Transition (Page Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	6		ns
t_{EHLX}	Chip Enable High to Latch Enable Transition		0		ns
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	0		ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$		10	ns
t_{ELLL}	Chip ENable Low to Latch Enable Low		10		ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	0		ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$		10	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		50	ns
t_{GLQX}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	0		ns
t_{LHAX}	Latch Enable High to Address Transition	$\overline{E} = V_{IL}$	10		ns
t_{LHLL}	Latch Enable High to Latch Enable Low		10		ns
t_{LLLH}	Latch Enable Low to Latch Enable High	$\overline{E} = V_{IL}$	10		ns
t_{LLQV}	Latch Enable Low to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		125	ns
t_{LLQV1}	Latch Enable Low to Output Valid (Page Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$		25	ns
t_{LLQX}	Latch Enable Low to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	0		ns

Figure 10. Asynchronous Read Latch Enable Controlled Read AC Waveforms (x16, x32 organization)
Asynchronous Read (M15 = 1), Latch Enable Controlled (M3 = 1)

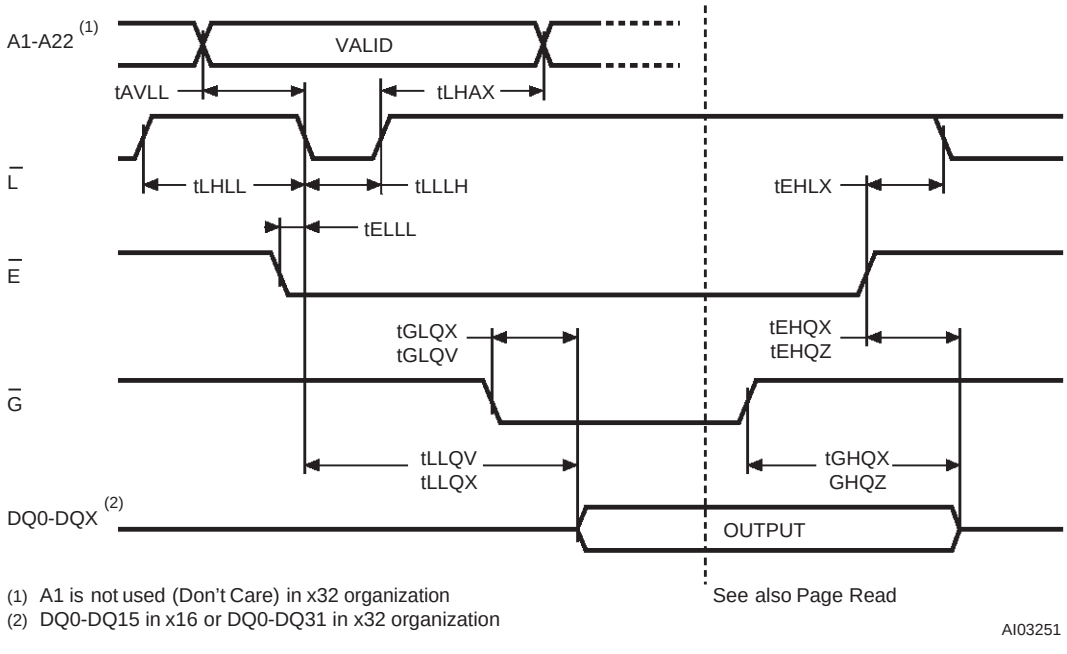
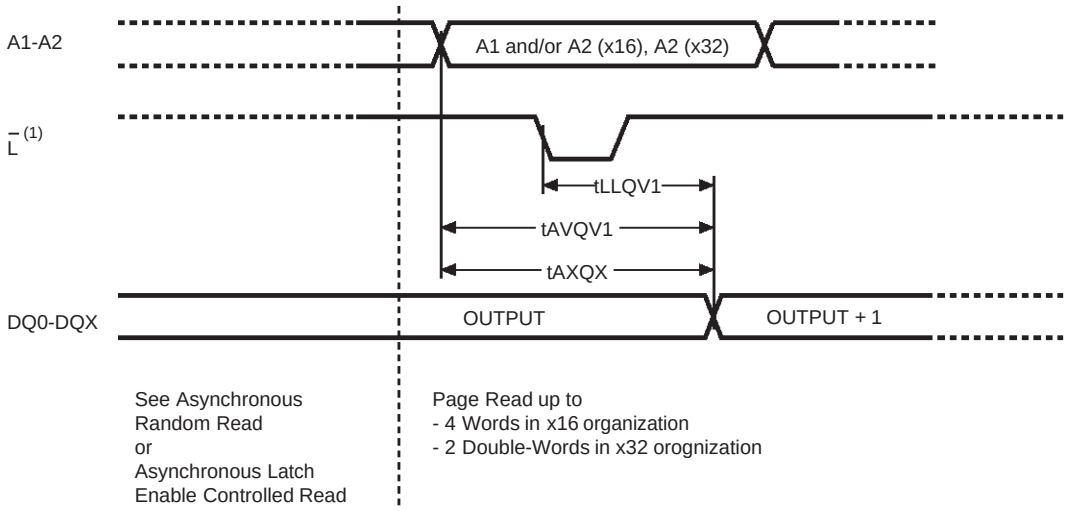


Figure 11. Asynchronous Page Read for Random or Latch Enable Controlled Read
Asynchronous Read (M15 = 1), Random (M3 = 0) or Latch Enable Controlled (M3 = 1)



(1) Only for Latch Enable Controlled Read

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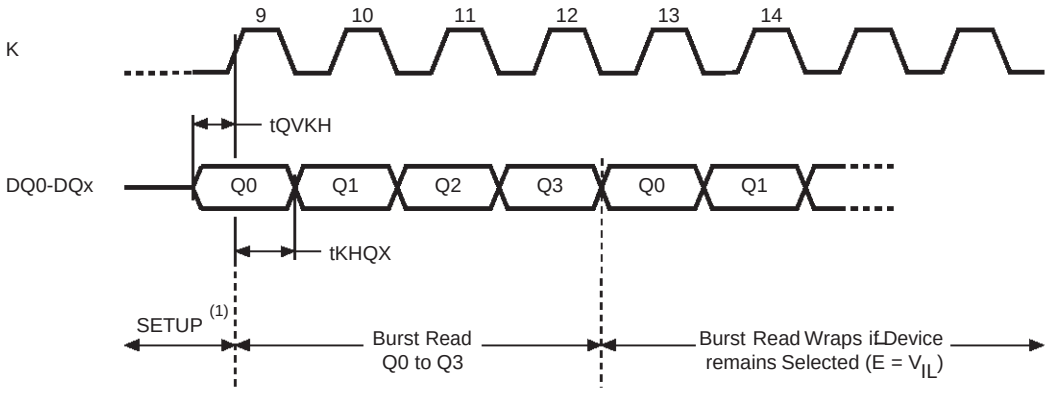
Table 22. Synchronous Burst Read
(T_A = 0 to 70°C, –40 to 85°C, V_{CC} = 2.7V to 3.6V, V_{CCQ} = 1.8V to V_{CC})

Symbol[1]	Parameter	Test Condition	Min	Max	Unit
t_{AVLL}	Address Valid to Latch Enable Low	$\overline{E} = V_{IL}$	10		ns
t_{BHKH}	Burst Address Advance High to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	10		ns
t_{BLKH}	Burst Address Advance Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	10		ns
t_{ELLL}	Chip Enable Low to Latch Enable low		0		ns
t_{GLKH}	Output Enable Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{L} = V_{IH}$	20		ns
t_{KHAX}	Valid Clock Edge to Address Transition	$\overline{E} = V_{IL}$	0		ns
t_{KHLL}	Valid Clock Edge to Latch Enable Low	$\overline{E} = V_{IL}$	0		ns
t_{KHLX}	Valid Clock Edge to Latch Enable Transition	$\overline{E} = V_{IL}$	0		ns
t_{KHQX}	Valid Clock Edge to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$		6	ns
t_{LLKH}	Latch Enable Low to Valid Clock Edge	$\overline{E} = V_{IL}$	10		ns
t_{QVKH}[2]	Output Valid to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	10		ns
t_{RLKH}	Valid Data Ready Low to Valid Clock Edge	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, $\overline{L} = V_{IH}$	10		ns

Note: 1. For parameters not listed see Asynchronous Read.
2. Data output should be read on the valid clock edge.

Figure 12. Synchronous Burst Read (9.1.1.1 example)
X-Latency = 0 (M14-M11 = 0100), Y-Latency = 1 (M9 = 0), Burst Length = 4 (M2-M0 = 001), Burst Type = Sequential (M7 = 1), Valid Clock Edge = Rising (M6 = 1)



(1) For set up signals and timings see Synchronous Burst Read 8.1.1.1

AI03698

Figure 13. Synchronous Burst Read (8.1.1.1 example)
X-Latency = 8 (M14-M11 = 0010), Y-Latency = 1 (M9 = 0), Burst Length = 1 (M2-M0 = 100), Burst Type = Any (M7 = 0 or 1), Valid Clock Edge = Rising (M6 = 1)

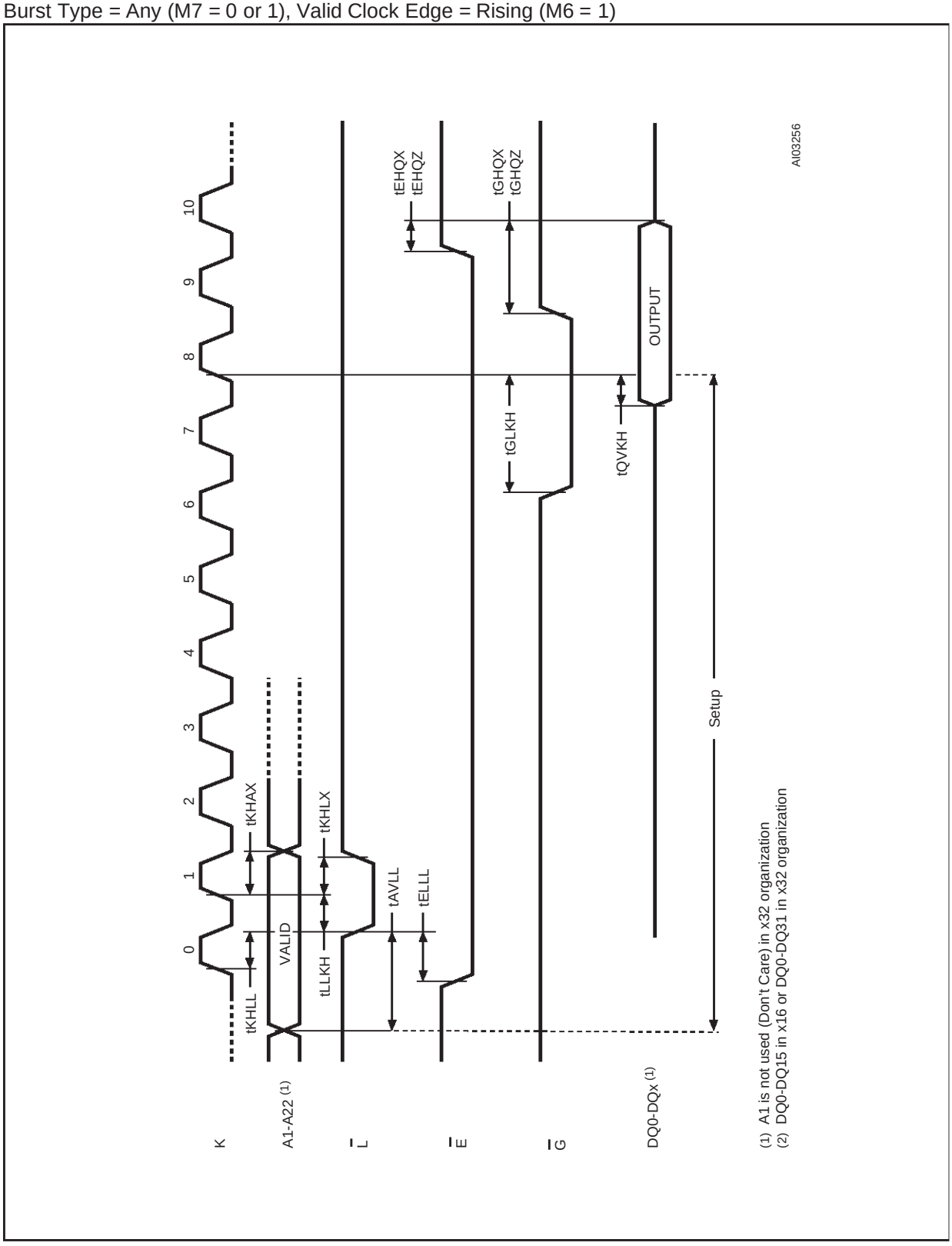
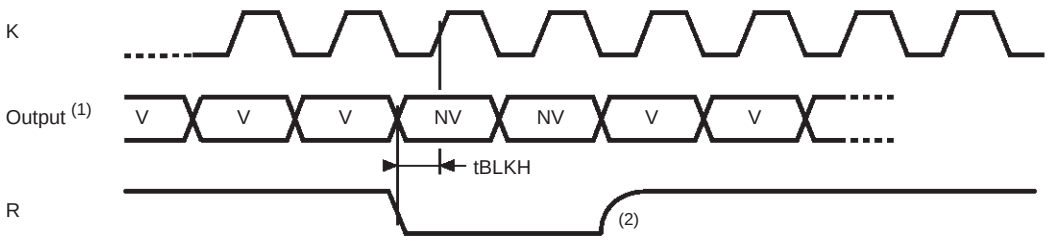


Figure 14. Synchronous Burst Read - Continuous - Valid Data Ready Output
Valid Data Ready = Valid Low during valid clock edge (M8 = 0)



(1) V = Valid output; NV = Not Valid output.
(2) R is an open drain output with an internal pull up resistor of 1MΩ.
The internal timing of R follows DQ. An external resistor, typically 300kΩ for a single memory on the R Bus, should be used to give a data valid set up time required to recognize valid data is available on the next valid clock edge.

AI03696

Figure 15. Synchronous Burst Pipeline Read (8.1.1.1 example)
X-Latency = 8 (M14-M11 = 0010), Y-Latency = 1 (M9 = 0), Burst Length = 1 (M2-M0 = 100), Burst Type = Any (M7 = 0 or 1), Valid Clock Edge = Rising (M6 = 1)

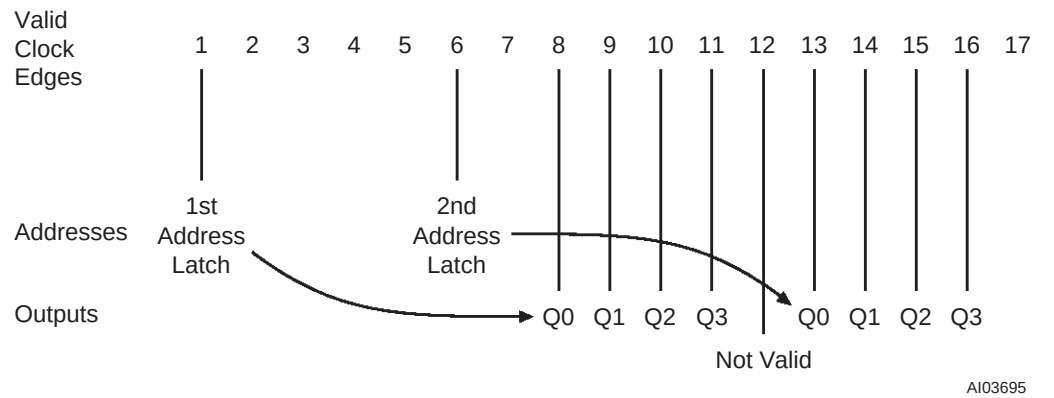


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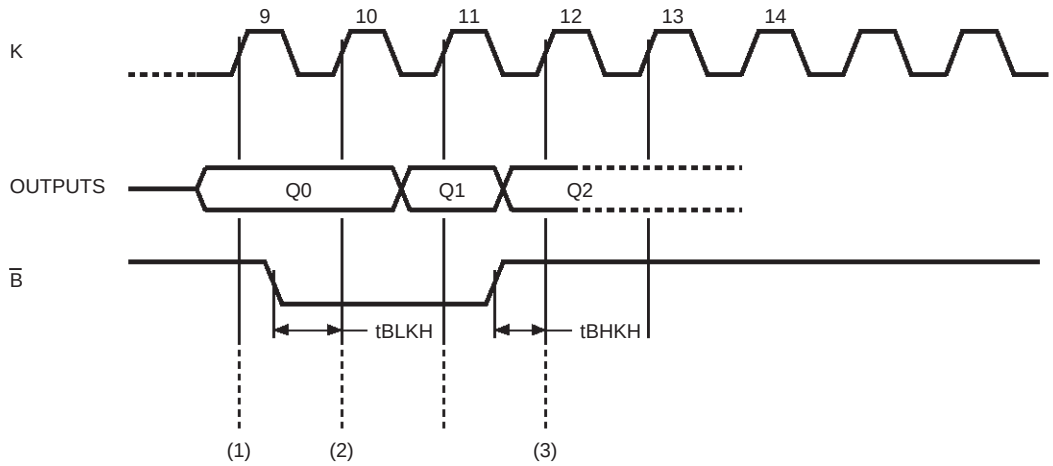
Figure 16. Synchronous Burst Read - Burst Address Advance



(1) Valid clock edge '9' is valid and outputs Q0.
(2) B goes low before valid clock edge '10' and output increments to Q1.
(3) B goes high before valid clock edge '12' and output remains Q2.

AI03697

Table 23. Asynchronous Write and Latch Enable Controlled Write AC Characteristics, Write Enable Controlled

(T_A = 0 to 70°C, –40 to 85°C, V_{CC} = 2.7V to 3.6V, V_{CCQ} = 1.8V to V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{AVLH}	Address Valid to Latch Enable High		10		ns
t_{AVWH}	Address Valid to Write Enable High	$\overline{E} = V_{IL}$	50		ns
t_{DVWH}	Data Input Valid to Write Enable High	$\overline{E} = V_{IL}$	50		ns
t_{ELWL}	Chip Enable Low to Write Enable Low		0		ns
t_{ELLL}	Chip Enable Low to Latch Enable Low		0		ns
t_{LHAX}	Latch Enable High to Address Transition		3		ns
t_{LLLH}	Latch Enable low to Latch Enable High		10		ns
t_{LLWH}	Latch Enable Low to Write Enable High		50		ns
t_{QVRH}	Output Valid to Reset/Power Down VCC		0		ns
t_{QVVPL}	Output Valid to Program/Erase Enable Low		0		ns
t_{RHHWH}	Reset/Power Down V_{HH} to Write Enable High		0		ns
t_{VPHWH}	Program/Erase Enable High to Write Enable High		0		ns
t_{WHAX}	Write Enable High to Address Transition	$\overline{E} = V_{IL}$	10		ns
t_{WHBL}	Write Enable High to Ready/Busy low			90	ns
t_{WHDX}	Write Enable High to Input Transition	$\overline{E} = V_{IL}$	10		ns
t_{WHEH}	Write Enable High to Chip Enable High		0		ns
t_{WHGL}	Write Enable High to Output Enable Low		35		ns
t_{WHWL}	Write Enable High to Write Enable Low		30		ns
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{E} = V_{IL}$	70		ns

Figure 17. Asynchronous Write AC Waveforms, Write Enable Controlled

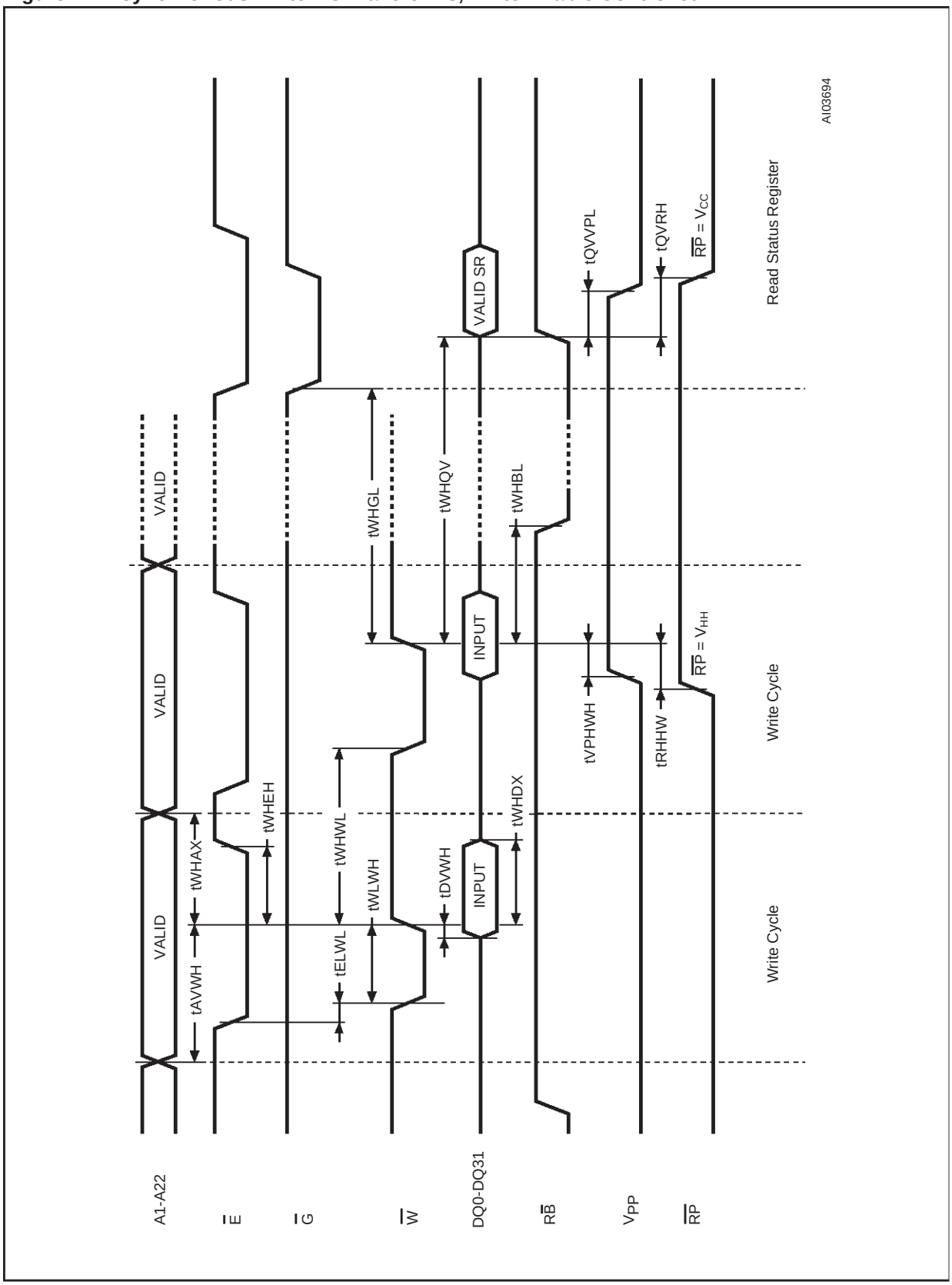


Figure 18. Asynchronous Latch Enabled Controlled Write AC Waveforms, Write Enable Controlled

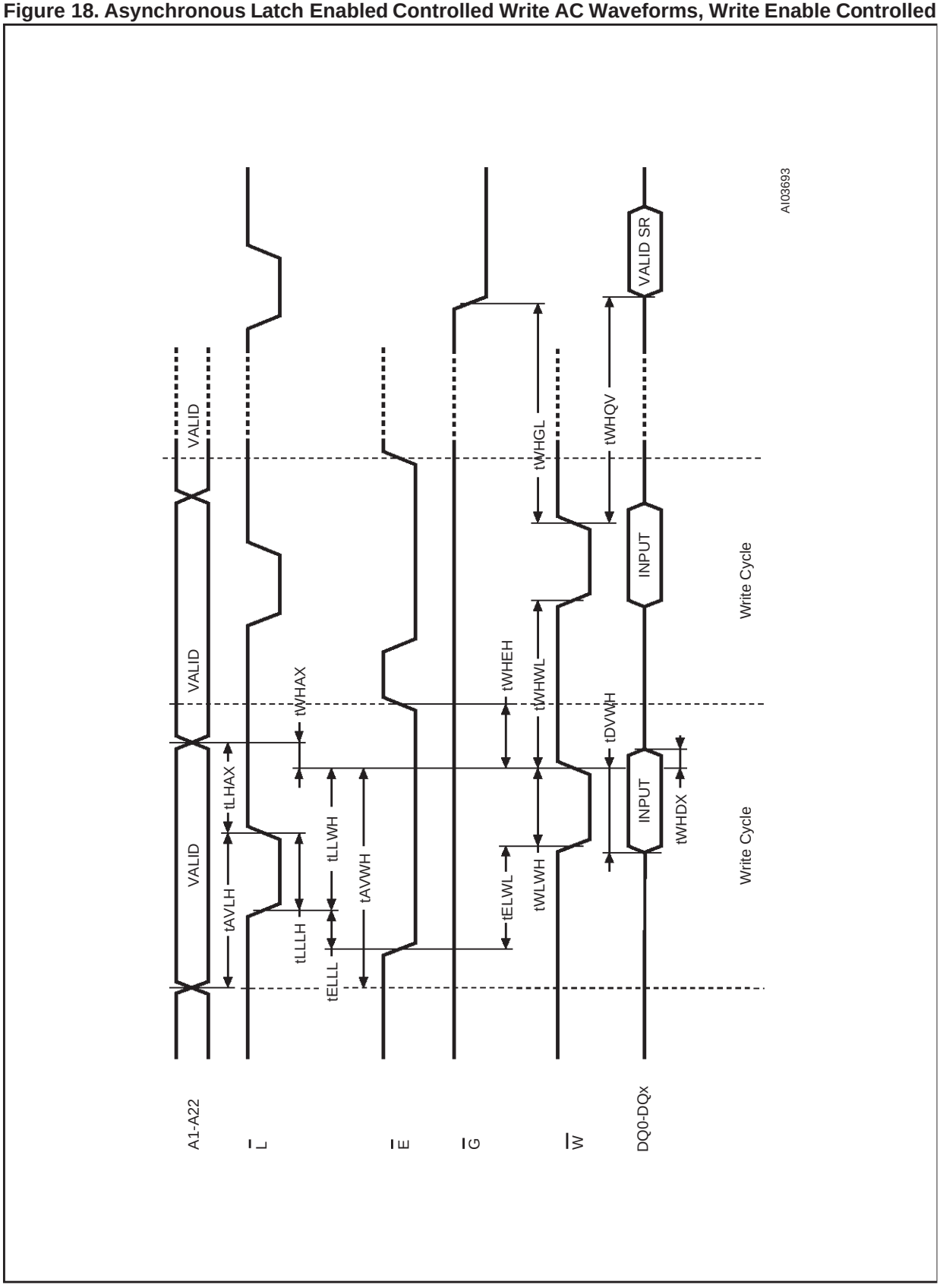


Table 24. Asynchronous Write and Latch Enable Controlled Write AC Characteristics, Chip Enable Controlled

(T_A = 0 to 70°C, –40 to 85°C, V_{CC} = 2.7V to 3.6V, V_{CCQ} = 1.8V to V_{CC})

Symbol	Parameter	Test Condition	Min	Max	Unit
t_{AVLH}	Address Valid to Latch Enable High		10		ns
t_{AVEH}	Address Valid to Chip Enable High	$\overline{W} = V_{IL}$	50		ns
t_{DVEH}	Data Input Valid to Chip Enable High	$\overline{W} = V_{IL}$	50		ns
t_{WLEL}	Write Enable Low to Chip Enable Low		0		ns
t_{WLLL}	Write Enable Low to Latch Enable Low		0		ns
t_{LHAX}	Latch Enable High to Address Transition		3		ns
t_{LLLH}	Latch Enable low to Latch Enable High		10		ns
t_{LLEH}	Latch Enable Low to Chip Enable High		50		ns
t_{QVRH}	Output Valid to Reset/Power Down VCC		0		ns
t_{QVVPL}	Output Valid to Program/Erase Enable Low		0		ns
t_{RHHEH}	Reset/Power Down V_{HH} to Chip Enable High		0		ns
t_{VPHEH}	Program/Erase Enable High to Chip Enable High		0		ns
t_{EHAX}	Chip Enable High to Address Transition	$\overline{W} = V_{IL}$	10		ns
t_{EHBL}	Chip Enable High to Ready/Busy low			90	ns
t_{EHDX}	Chip Enable High to Input Transition	$\overline{W} = V_{IL}$	10		ns
t_{EHEH}	Chip Enable High to Chip Enable High		0		ns
t_{EHGL}	Chip Enable High to Output Enable Low		35		ns
t_{EHEL}	Chip Enable High to Chip Enable Low		30		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	$\overline{W} = V_{IL}$	70		ns

Figure 19. Asynchronous Write AC Waveforms, Chip Enable Controlled

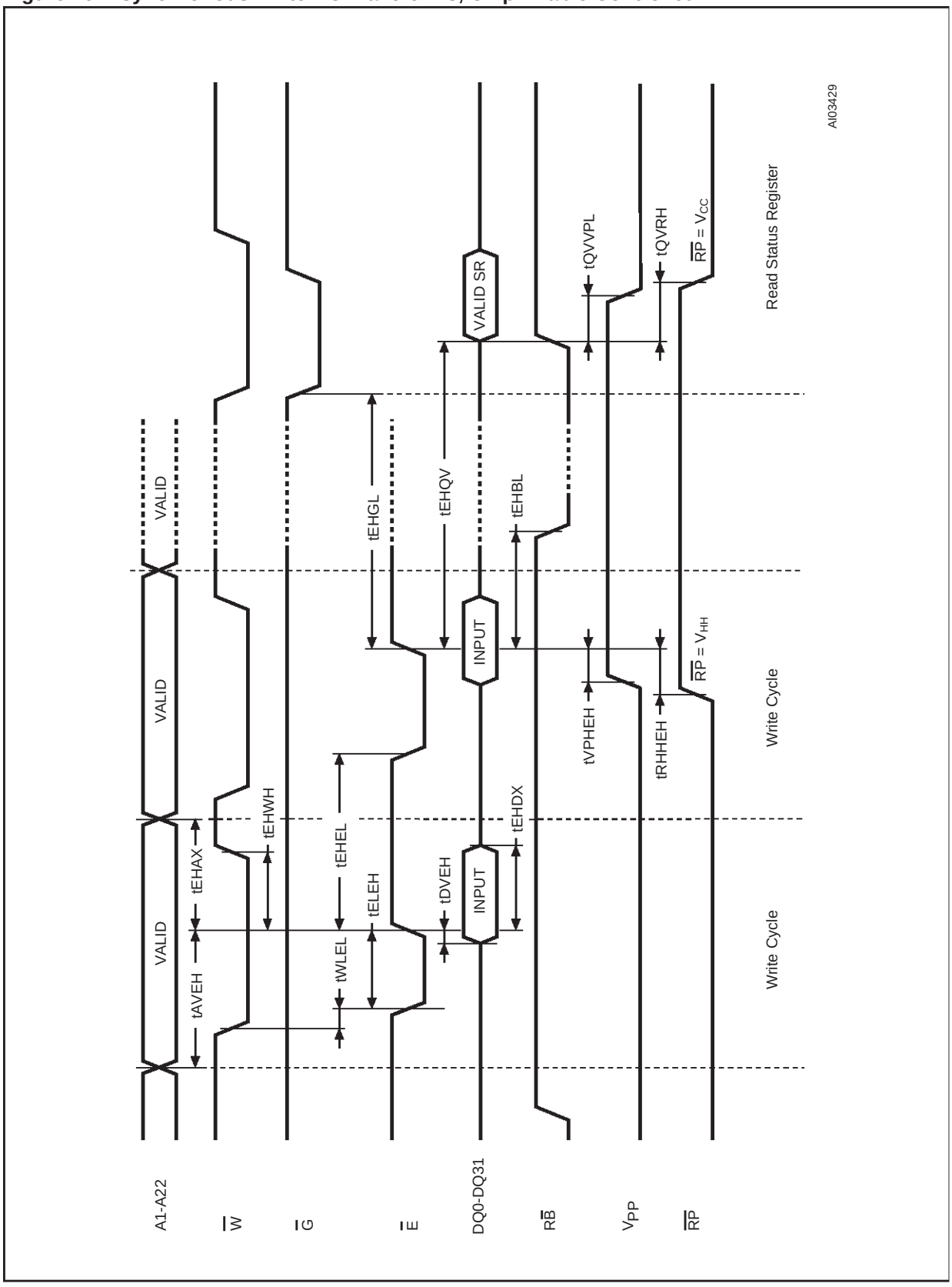


Figure 20. Asynchronous Latch Enabled Controlled Write AC Waveforms, Write Enable Controlled

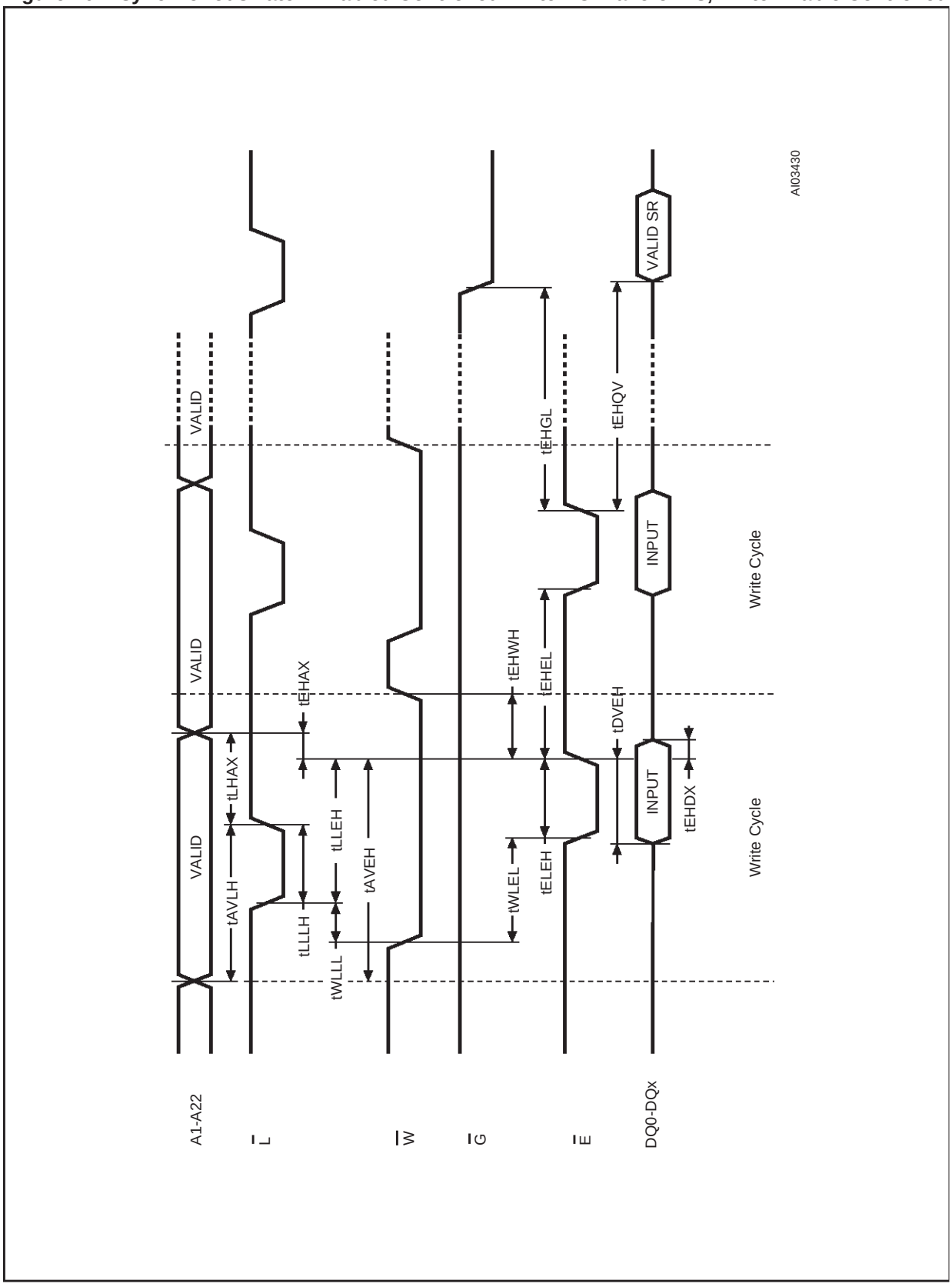


Table 25. Reset, Power-down and Power-up
(T_A = 0 to 70°C, –40 to 85°C, V_{CC} = 2.7V to 3.6V, V_{CCQ} = 1.8V to V_{CC})

Symbol	Parameter	Min	Max	Unit
t_{PHEL}	Reset/Power-down High to Chip Enable Low		10	µs
t_{PHQV}	Reset/Power-down High to Output Valid		10	µs
t_{PHWL}	Reset/Power-down High to Write Enable Low		10	µs
t_{PLPH}	Reset/Power-down Low to Reset/Power-down High	500		ns
t_{PLRH}	Reset/Power-down Low to Ready High	22		µs
t_{PHR}	Power-up to Read		10	µs
t_{PHW}	Power-up to Write		10	µs
t_{VDHPH}	Supply Voltages High to Reset/Power-down High	1		µs

Table 26. Program, Erase Times and Program Erase Endurance Cycles
(T_A = 0 to 70°C; V_{CC} = 2.7V to 3.6V; V_{CCQ} =1.7V to 1.9V)

Parameters	M58LW064A/B				Unit
	Min	Max	Typ	Typical after 100k W/E Cycles	
Uniform Block (1Mb) Erase		1.5	0.75	0.75	sec
Chip Program			54	54	sec
Write Buffer			192	192	µs
Program Suspend Latency Time		10	3		µs
Erase Suspend Latency Time		30	10		µs
Program/Erase Cycles (per Block)	100,000				cycles

Figure 21. Reset, Power-down and Power-up AC Waveform

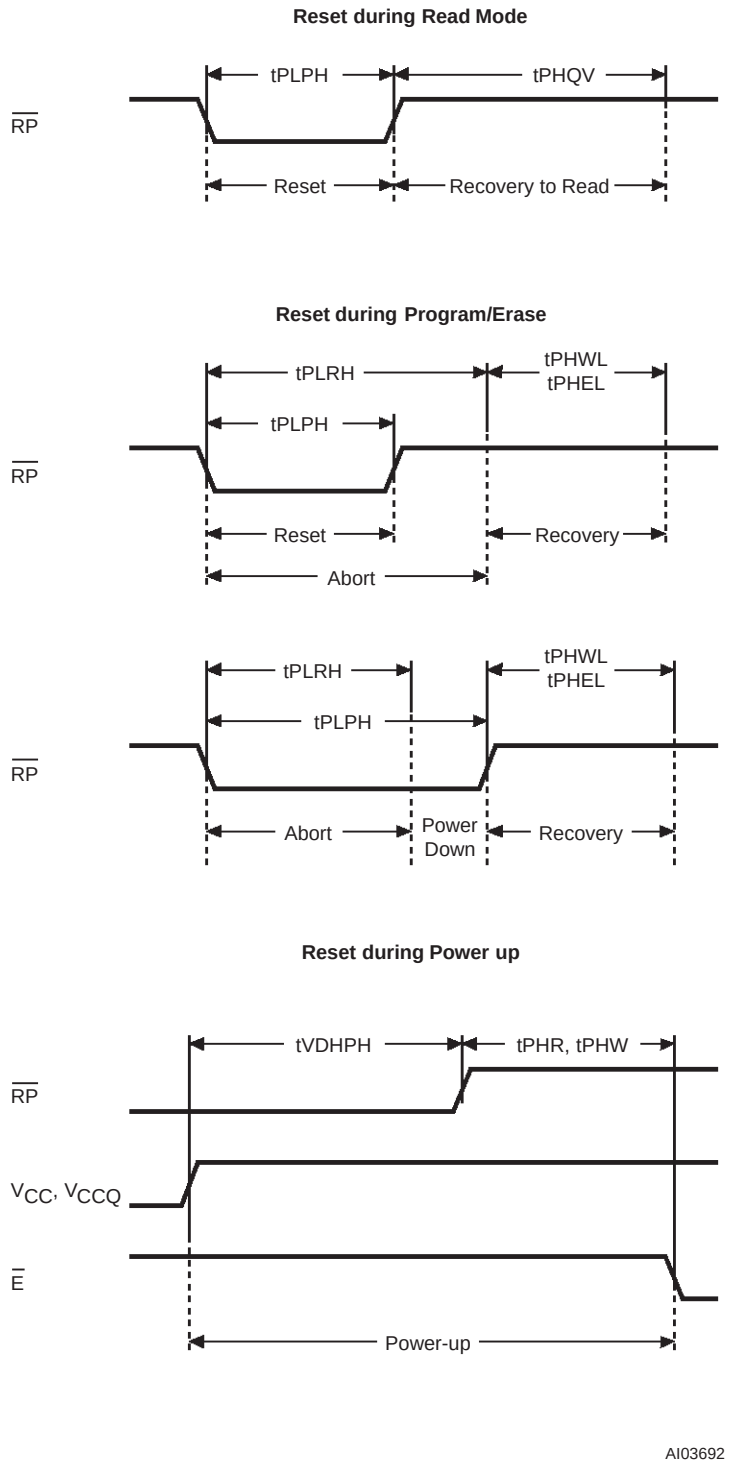


Figure 22. Write Buffer Program Flowchart and Pseudo Code

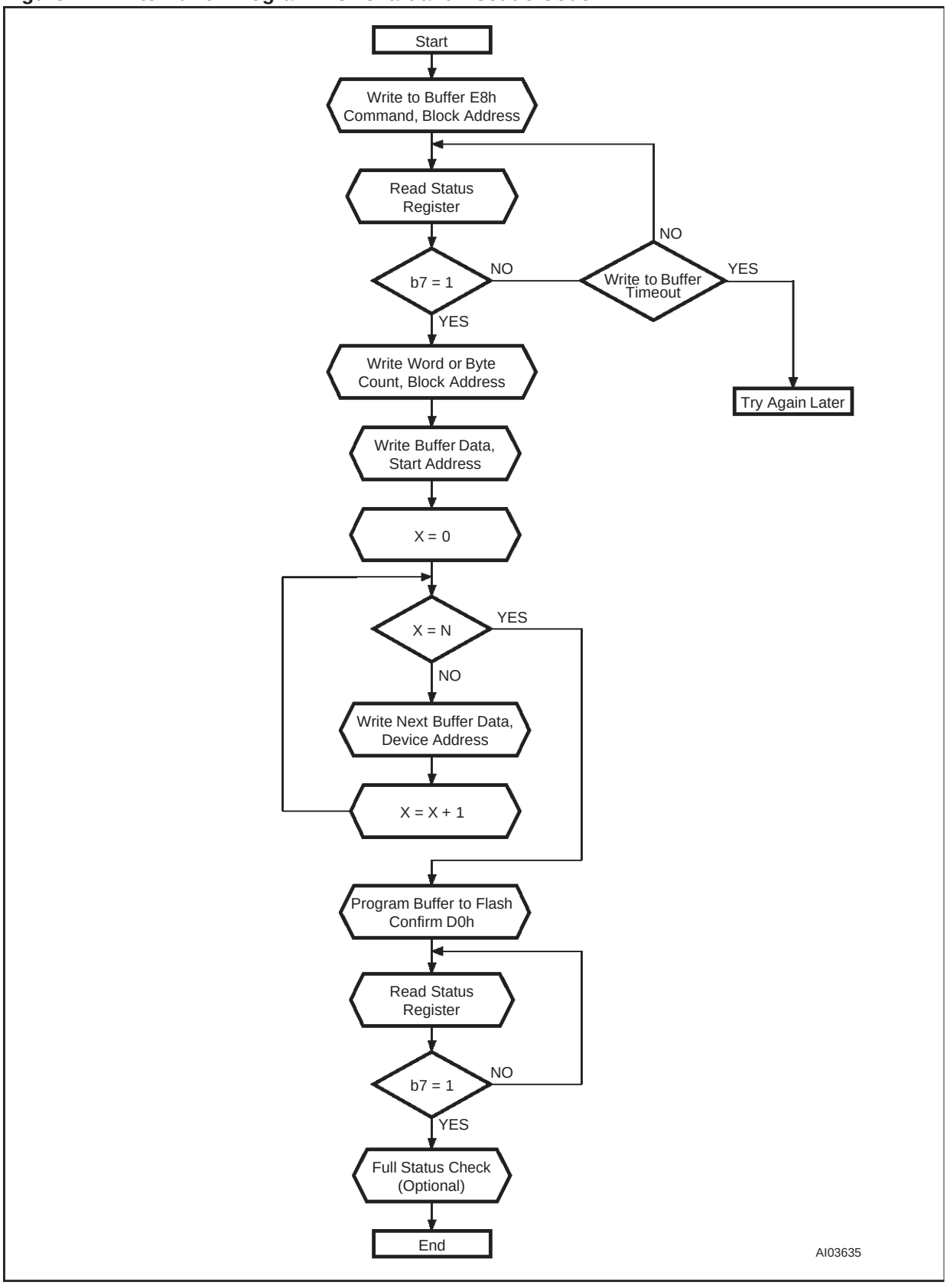
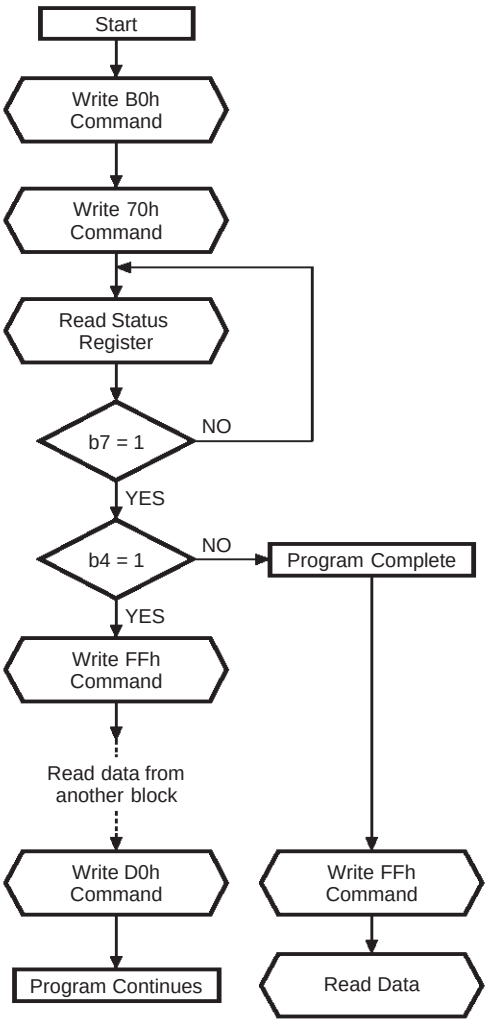


Figure 23. Program Suspend & Resume Flowchart and Pseudo Code



PES instruction:
– write B0h command
(memory enters read register state after the PES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

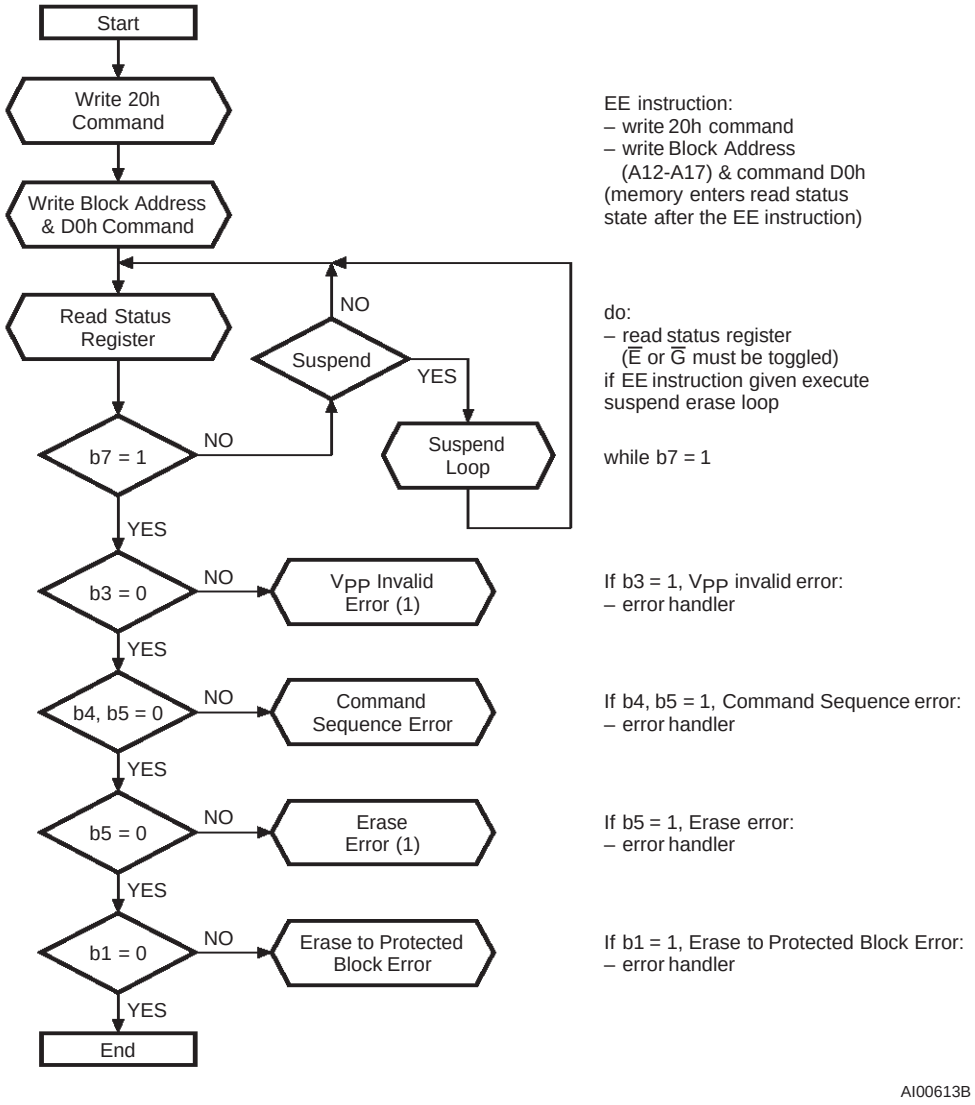
If b4 = 0, Program completed
(at this point the memory will accept only the RD or PER instruction)

RD instruction:
– write FFh command
– one or more data reads from another block

PER instruction:
– write D0h command to resume erasure
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase suspend was not issued).

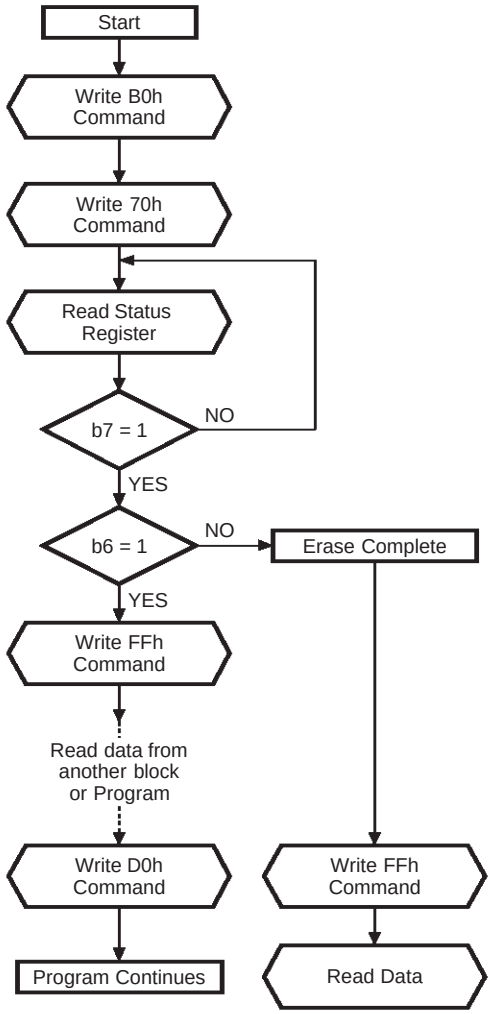
AI00612

Figure 24. Erase Flowchart and Pseudo Code



Note: 1. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 25. Erase Suspend & Resume Flowchart and Pseudo Code



PES instruction:
– write B0h command
(memory enters read register state after the PES instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

If b6 = 0, Erase completed
(at this point the memory wich accept only the RD or PER instruction)

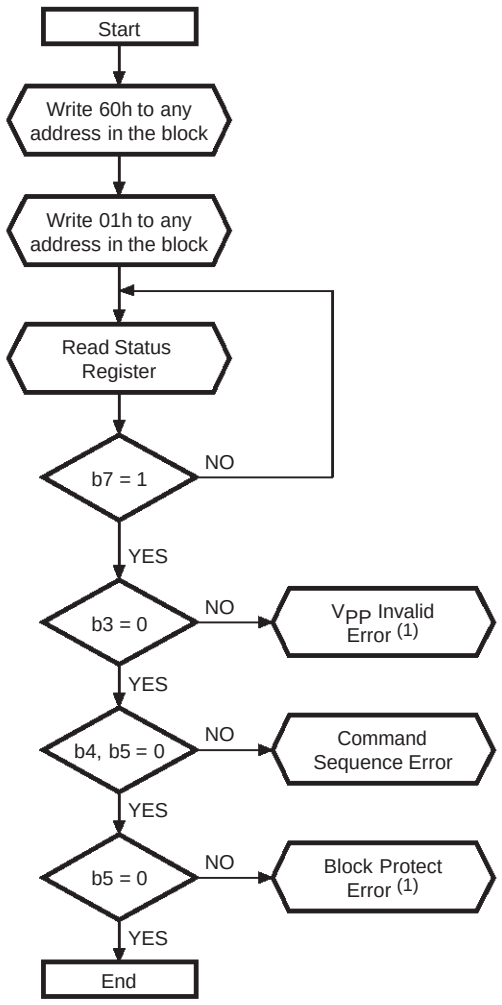
RD instruction:
– write FFh command
– one o more data reads from another block

PG instruction:
– write 40h command
– write Address & Data

PER instruction:
– write D0h command to resume erasure
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase suspend was not issued).

AI00615

Figure 26. Block Protect Flowchart and Pseudo Code



BP instruction:
– write 60h command to any address in the block
– write 01h command to any address in the block
(memory enters read status
state after the BP instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

If b3 = 1, V_{PP} invalid error:
– error handler

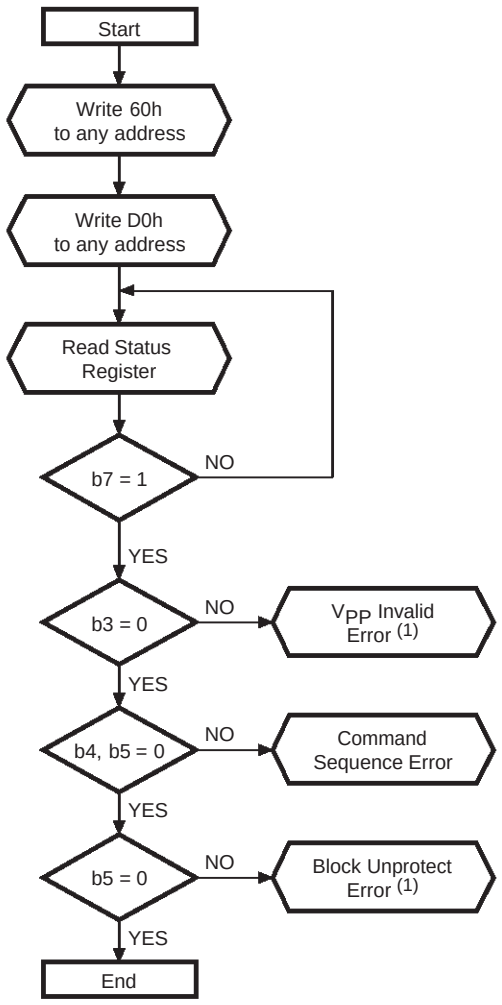
If b4. b5 = 1, Command Sequence error:
– error handler

If b5 = 1, Block Protect error:
– error handler

AI03427

Note: 1. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 27. Block Unprotect Flowchart and Pseudo Code



BU instruction:
– write 60h command to any address
– write D0h command to any address
(memory enters read status
state after the BU instruction)

do:
– read status register
($\overline{E}$ or $\overline{G}$ must be toggled)

while b7 = 1

If b3 = 1, V_{PP} invalid error:
– error handler

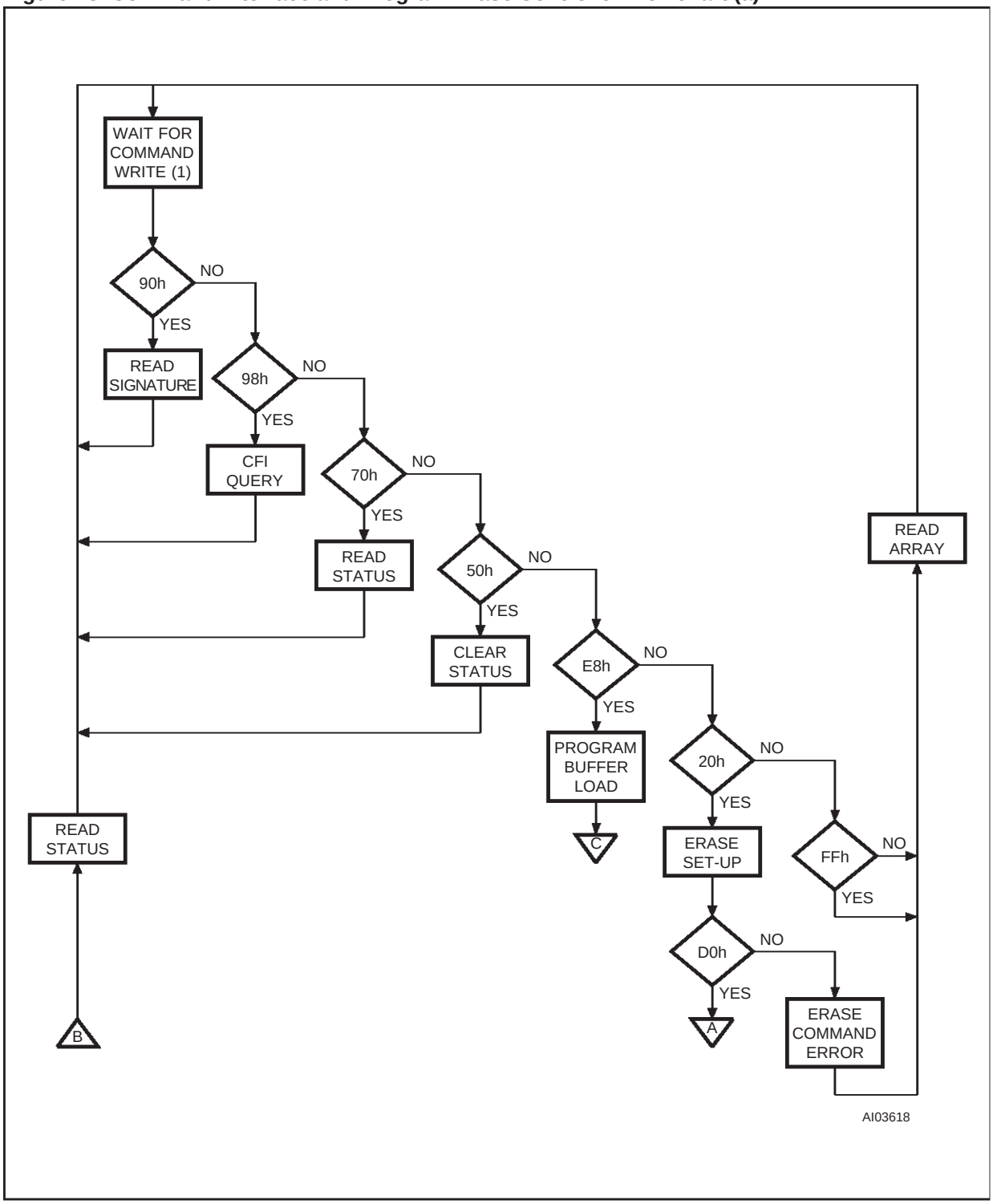
If b4. b5 = 1, Command Sequence error:
– error handler

If b5 = 1, Block Unprotect error:
– error handler

AI03428

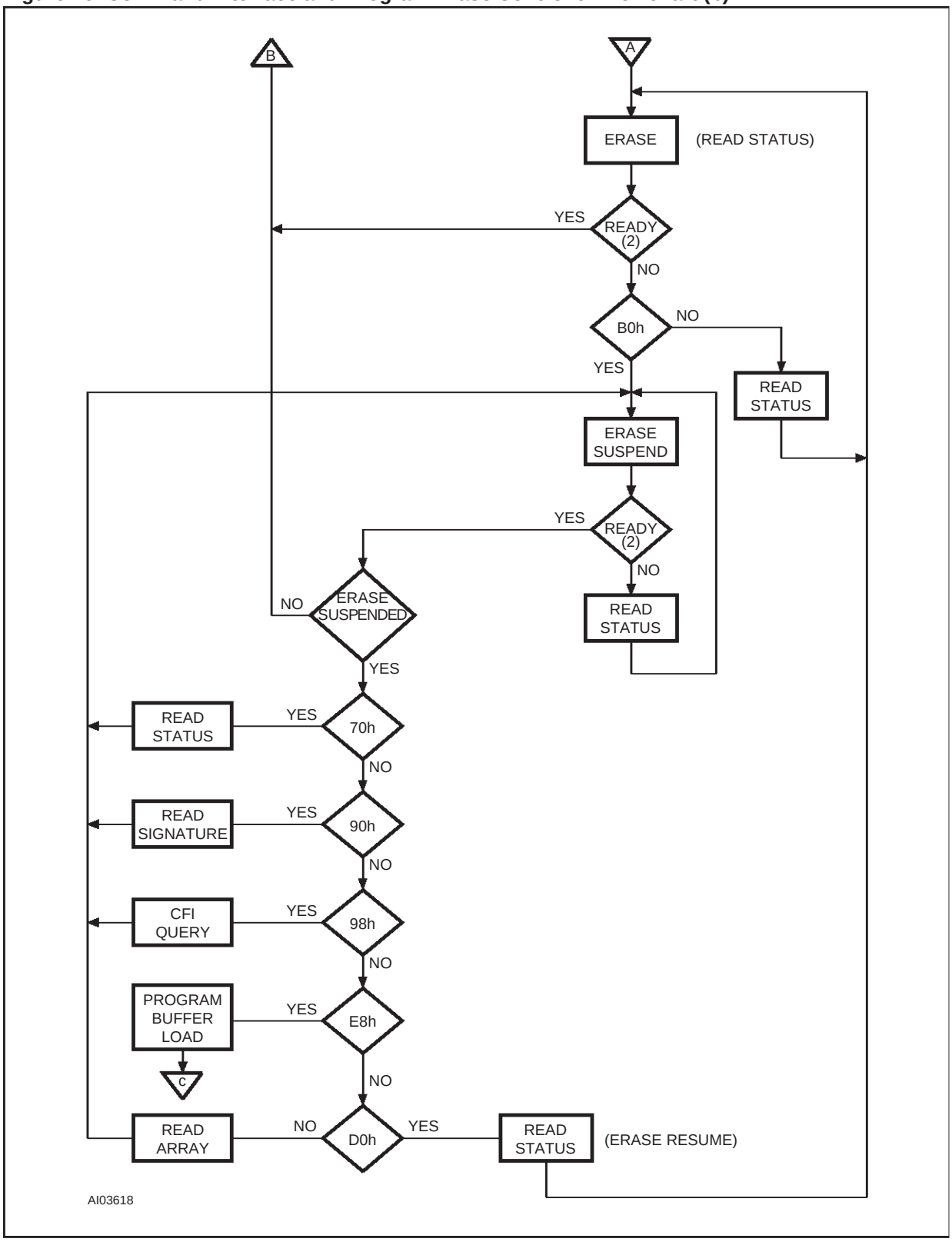
Note: 1. If an error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Figure 28. Command Interface and Program Erase Controller Flowchart (a)



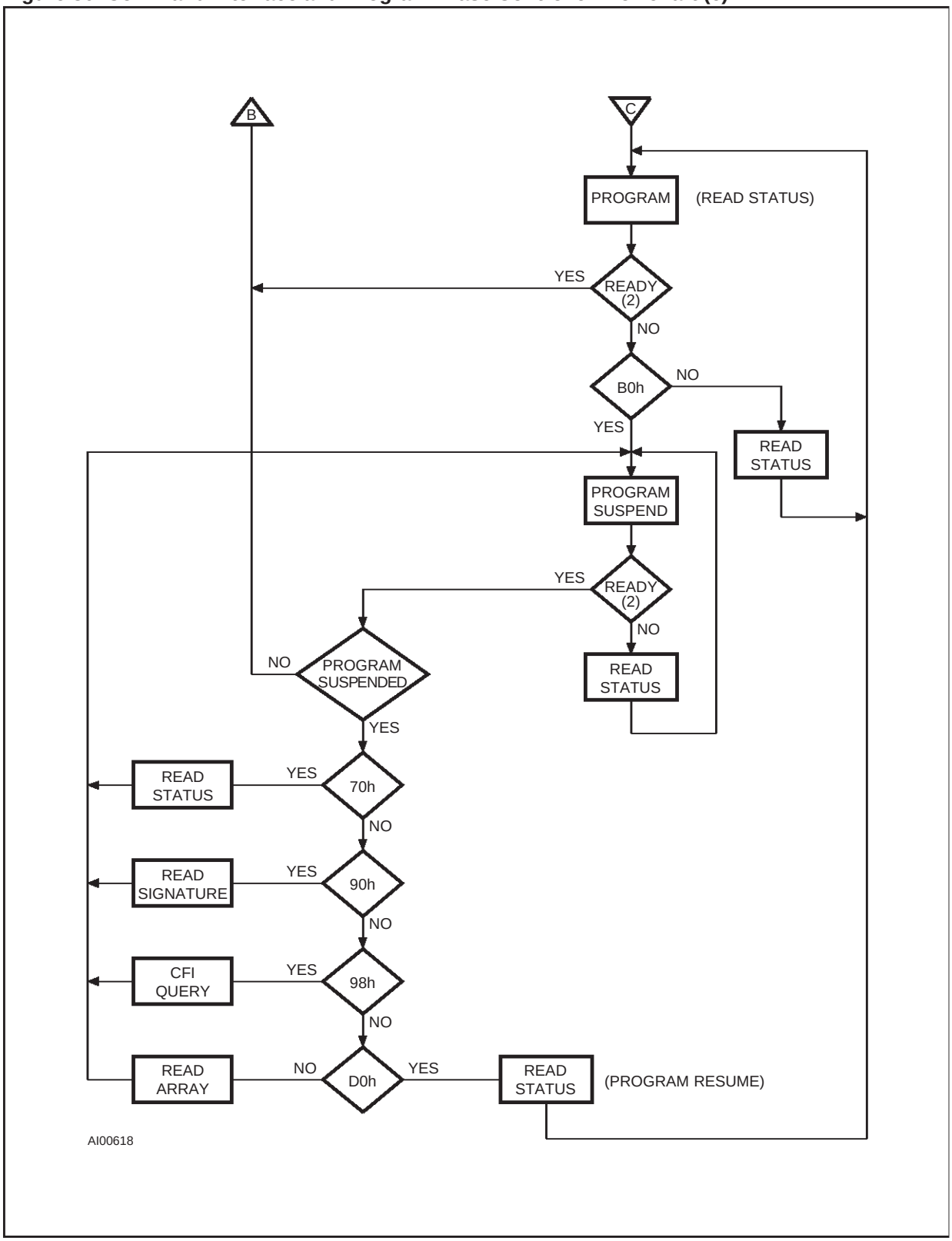
Note: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 29. Command Interface and Program Erase Controller Flowchart (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Figure 30. Command Interface and Program Erase Controller Flowchart (c)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

Table 27. Ordering Information Scheme

Example: M58LW064A 150 N 1 T

Device Type
M58

Architecture
L = Multi-Bit Cell, Burst Mode, Page Mode

Operating Voltage
W = V_{CC} = 2.7V to 3.6V; V_{CCQ} = 1.8 to V_{CC}

Device Function
064A = 64 Mbit (x16), Equal Block, Boot Block
064B = 64 Mbit (x16/x32), Equal Block, Boot Block

Speed
150 = 150 ns

Package
N = TSOP56: 14 x 20 mm
NC = TSOP86 Type II
T = PQFP80
ZA = LBGA54: 1 mm pitch

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

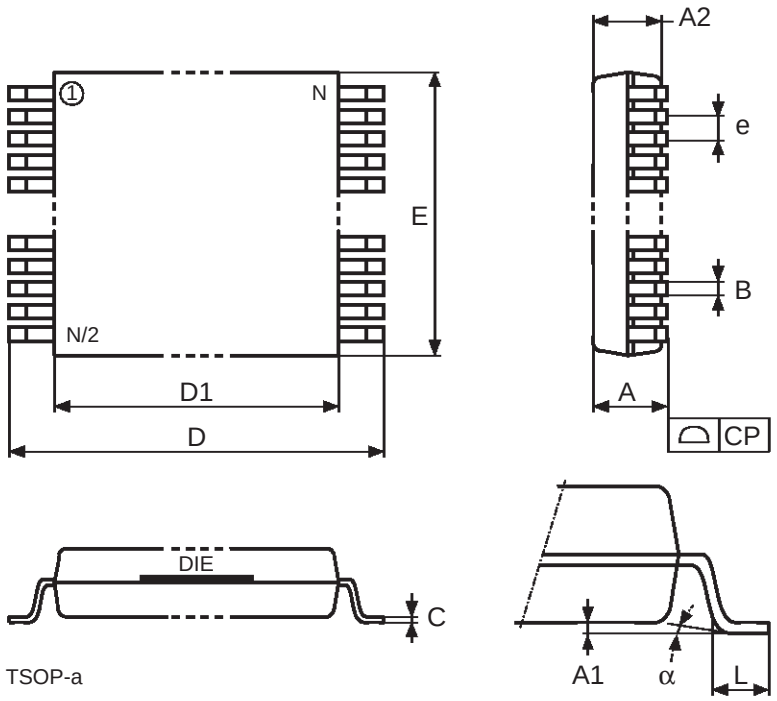
Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Configuration, Package, etc...) or for further information on any aspect of this memory, please contact the STMicroelectronics Sales Office nearest to you.

Table 28. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		13.90	14.10		0.5472	0.5551
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0276
α		0°	5°		0°	5°
N	56			56		
CP			0.10			0.0039

Figure 31. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Outline



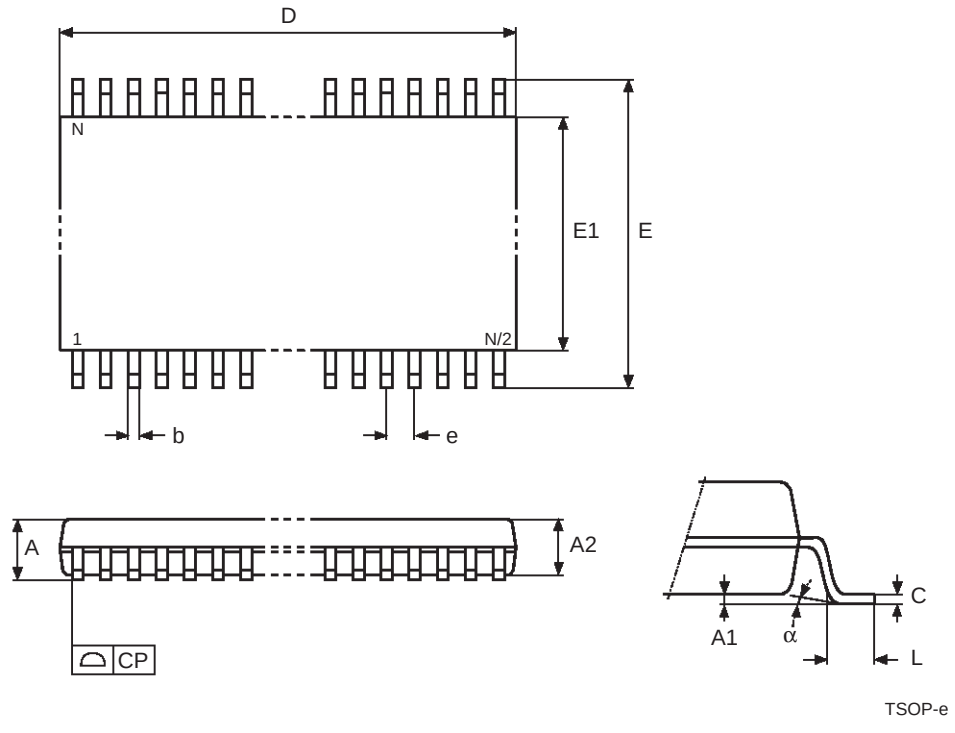
TSOP-a

Drawing is not to scale.

Table 29. TSOP86 Type II, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.950	1.050	0.0394	0.0374	0.0413
b		0.170	0.270		0.0067	0.0106
C		0.120	0.210		0.0047	0.0083
CP			0.200			0.0079
D	22.220	–	–	0.8748	–	–
e	0.500	–	–	0.0197	–	–
E	11.760	–	–	0.4630	–	–
E1	10.160	–	–	0.4000	–	–
L	0.500	0.400	0.600	0.0197	0.0157	0.0236
α		0°	8°		0°	8°
N	86			86		

Figure 32. TSOP86 Type II, Package Outline

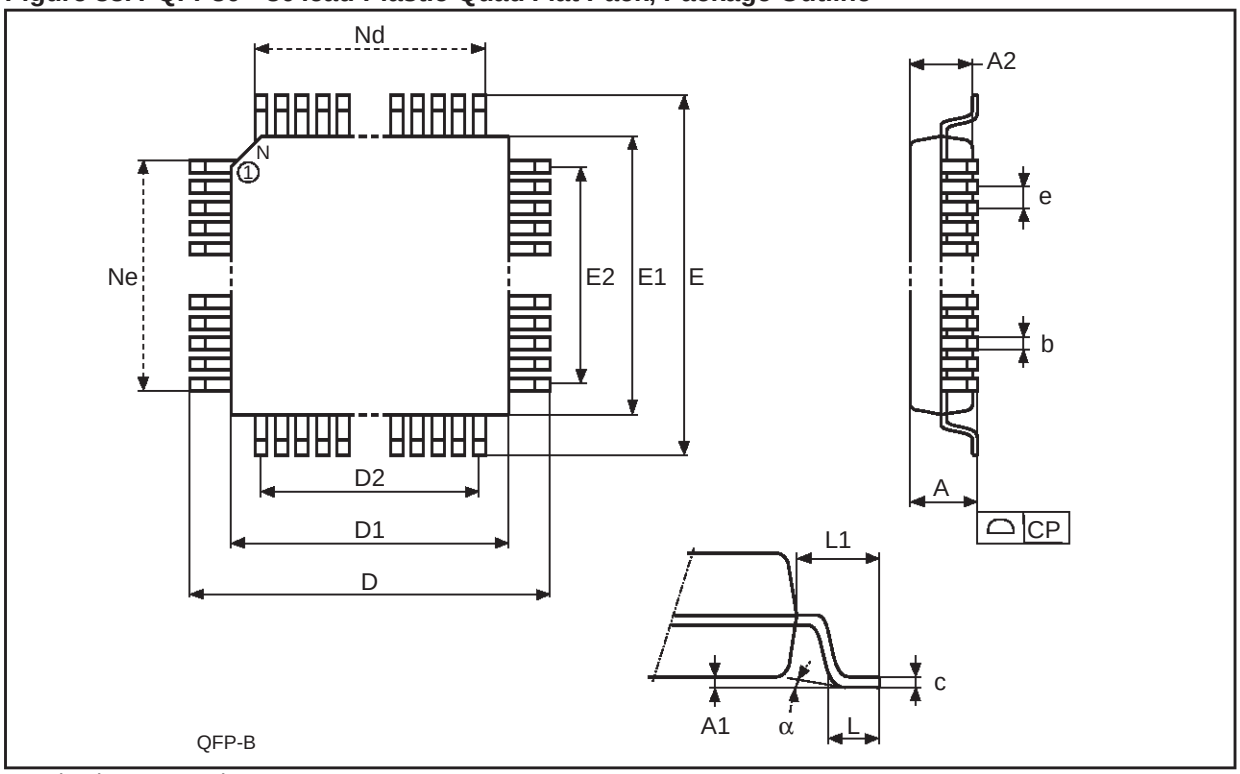


Drawing is not to scale.

Table 30. PQFP80 - 80 lead Plastic Quad Flat Pack, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.400			0.1339
A1		0.250			0.0098	
A2	2.800	2.550	3.050	0.1102	0.1004	0.1201
b		0.300	0.450		0.0118	0.0177
c		0.130	0.230		0.0051	0.0091
D	17.200	16.950	17.450	0.6772	0.6673	0.6870
D1	14.000	13.900	14.100	0.5512	0.5472	0.5551
D2	12.000	–	–	0.4724	–	–
e	0.800	–	–	0.0315	–	–
E	23.200	22.950	23.450	0.9134	0.9035	0.9232
E1	20.000	19.900	20.100	0.7874	0.7835	0.7913
E2	18.400	–	–	0.7244	–	–
L	0.800	0.650	0.950	0.0315	0.0256	0.0374
L1	1.600	–	–	0.0630	–	–
α		0°	7°		0°	7°
N	80			80		
Nd	24			24		
Ne	16			16		

Figure 33. PQFP80 - 80 lead Plastic Quad Flat Pack, Package Outline

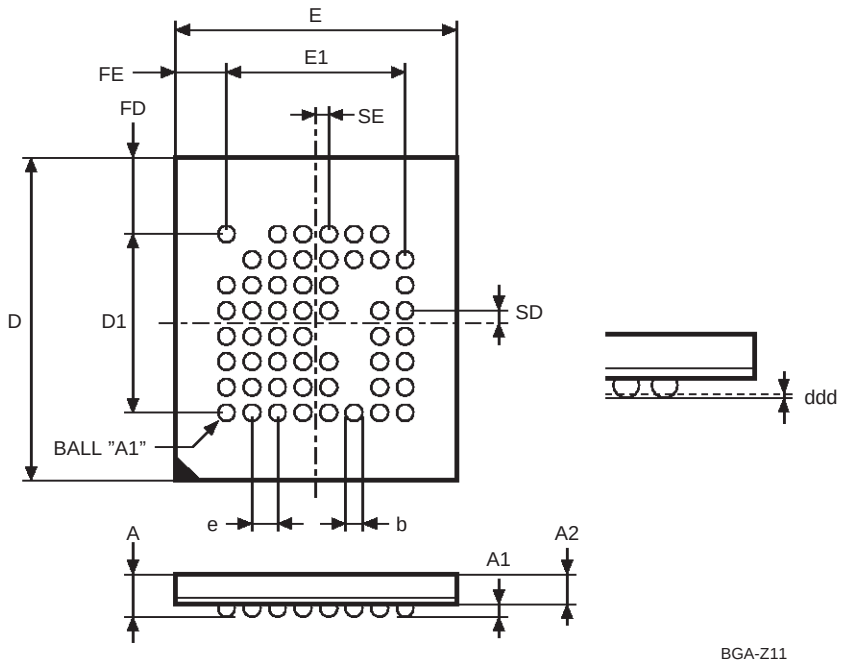


Drawing is not to scale.

Table 31. LBGA54 - 8 x 8 balls, 1 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	1.090	0.980	1.200	0.0429	0.0386	0.0472
A1	0.290	0.220	0.360	0.0114	0.0087	0.0142
A2	0.800	0.760	0.840	0.0315	0.0299	0.0331
b	0.430	0.300	0.560	0.0169	0.0118	0.0220
D	10.000	9.800	10.200	0.3937	0.3858	0.4016
D1	7.000	–	–	0.2756	–	–
ddd			0.150			0.0059
e	1.000	0.925	1.075	0.0394	0.0364	0.0423
E	13.000	12.800	13.200	0.5118	0.5039	0.5197
E1	7.000	–	–	0.2756	–	–
FD	3.000	–	–	0.1181	–	–
FE	1.500	–	–	0.0591	–	–
SD	0.500	–	–	0.0197	–	–
SE	0.500	–	–	0.0197	–	–

Figure 34. LBGA54 - 8 x 8 balls, 1 mm pitch, Package Outline



Drawing is not to scale.