PM7367

FREEDM-32P32

REVISION A DEVICE ERRATA

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PUBLIC REVISION HISTORY

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1   INTRODUCTION

In this document, Section 2 lists the known functional errata for revision A of PM7367 FREEDM-32P32 and Section 3 lists the errors found in Issue 2 of the PM7367 FREEDM-32P32 Long Form Data Sheet (PMC-1991499).

1.1   Device Identification

The information contained in the Errata relates to Revision A of PM7367 FREEDM-32P32 only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1.1). PM7367 FREEDM-32P32 Revision A is packaged in a 272-pin Plastic Ball Grid Array (PBGA).

Figure 1 – PM7367 FREEDM-32P32 Branding Format.

1.2   Reference

- PMC-1991499, FREEDM-32P32 Long Form Data Sheet, Issue 2

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2   FREEDM-32P32 REVISION A FUNCTIONAL DEFICIENCY LIST

This section lists the known functional deficiencies for Revision A of FREEDM-32P32 (as of the publication date of this document). For each deficiency, the known work-around and the operating constraints, with and without the work-around, are also described.

Please report any functional deficiencies not covered in this document to PMC-Sierra.

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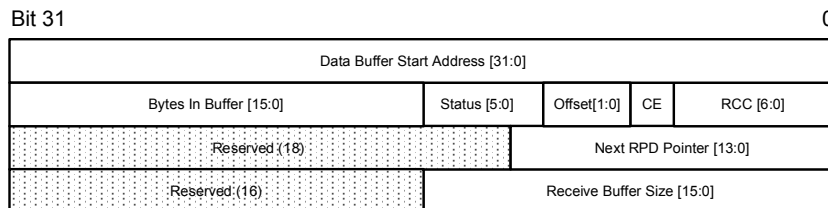## 2.1   Offset underflow in Receive Packet Descriptor

2.1.1 Description:

When ALL of the following conditions are met:

1. The offset[1:0] field of a Receive Packet Descriptor (RPD) is non-zero.

2. The STRIP bit of register "**0x204 RHDL Indirect Channel Data Register #1"** is logic one.

3. The incoming packet payload is smaller than the FCS field (2 bytes for CRC-CCITT or 4 bytes for CRC-32).

The value in the "Bytes in Buffer [15:0]" field of the RPD can be underflowed. That is, this field will contain a negative value. If this field is interpreted as an unsigned integer, the content of the buffer can be erroneously interpreted as a very large number.

2.1.1.1 Figure 2.1: Receive Packet Descriptor.

Bit 31   0

Data Buffer Start Address [31:0]				
Bytes In Buffer [15:0]	Status [5:0]	Offset[1:0]	CE	RCC [6:0]
Reserved (18)		Next RPD Pointer [13:0]		
Reserved (16)		Receive Buffer Size [15:0]		

2.1.2 Workarounds:

The following are **independent** workarounds for this error:

1. If the Offset[1:0] bits of RPD are set to zero, this problem will not occur.

2. If the STRIP field of "**0x204 RHDL Indirect Channel Data Register #1**" is set to zero, this problem will not occur.

3. If the buffer size is not larger than 32K Bytes, the most significant bit of the "Byte in Buffer" field can be used as a sign bit. The device software should discard RPDs that contain a negative "Bytes in Buffer" value.

For every RPD, the driver software can compare the "Bytes in Buffer[15:0]" field to ensure that it is smaller than or equal to "Receive Buffer Size[15:0]".

2.1.3 Performance with workaround:

FREEDM-32P32 works correctly.

2.1.4 Performance without workaround:

If the "Bytes in Buffer" field is interpreted as a very large number, the driver software may attempt to read data from outside of the allocated buffer space.

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2.2   TDR Status Bits Not Reporting All Underflow Events.

2.2.1 Description:

The underflow status bit (Status[2]) of Transmit Descriptor Reference (TDR) indicates whether or not an underflow condition is detected on the transmit packet[1].

In FREEDM-32P32 Rev A, the underflow status bit does NOT report ALL underflow events. That is, in some cases where underflow did occur, the underflow status bit would incorrectly return a value of zero ("0") to indicate that no underflow event was detected. On the other hand, when underflow did not occur this bit operates normally.

The total underflow count across all channels (register 0x508 PMON Transmit FIFO Underflow Count) is not affected by this and provides an accurate count.

2.2.2 Workarounds:

There is no workaround to this problem.

2.2.3 Performance with workaround:

Not applicable.

2.2.4 Performance without workaround:

The system will not be able to keep an accurate underflow count on a per HDLC channel basis.

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[1] For additional information on the operation of Status[2] in a TDR, please refer to Fig. 9.14, Transmit Descriptor Reference of PMC-991499 FREEDM-32P32 Datasheet.

2.3   PCI Hold Time Increased to 1ns

2.3.1 Description:

PCI Input and Bi-directional signals require a minimum hold time (tH_{PCI}) of 1 ns with respect to PCICLK.

2.3.1.1 Figure 2.2: PCI Interface Timing
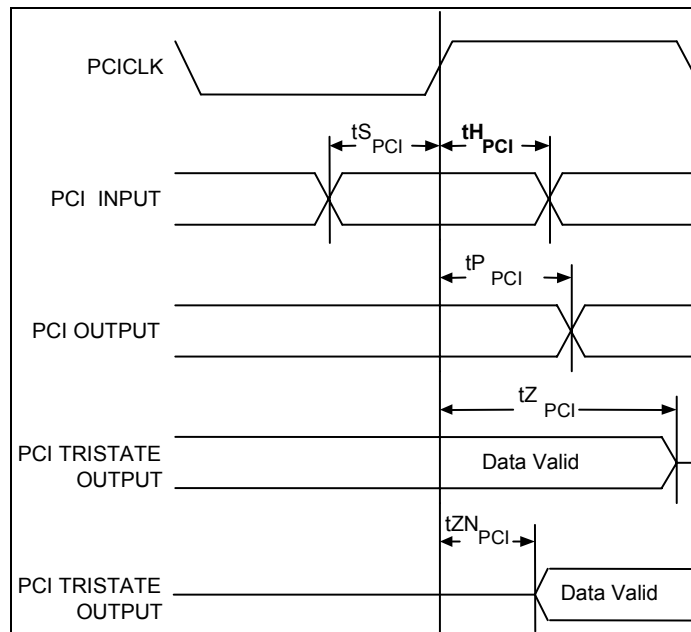
2.3.2 Workarounds:

The PCI 2.1 specification requires PCI outputs to have a minimum 2 ns propagation delay. The clock skew between FREEDM-32P32 and other PCI devices in a system must therefore be kept below 1 ns to ensure correct operation.

2.3.3 Performance with workaround:

Operates normally.

2.3.4 Performance without workaround:

If the clock skew is not kept within the above limit, FREEDM-32P32 may operate incorrectly.

3 DOCUMENTATION ERRORS

There are no known documentation errors in Issue 2 of PMC-1991499 FREEDM-32P32 Datasheet (as of the publication date of this document).

Please report any documentation errors not covered in this document to PMC-Sierra.

NOTES

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