ADVANCE INFORMATION

Am29BDD160G

16 Megabit (1 M x 16-bit/512 K x 32-Bit)
CMOS 2.5 Volt-only Burst Mode, Dual Boot, Simultaneous Read/ Write Flash Memory

DISTINCTIVE CHARACTERISTICS

ARCHITECTURE ADVANTAGES

- **Simultaneous Read/Write operations**
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
  - Two bank architecture: 75%/25%
- **User-Defined x16 or x32 Data Bus**
- **Dual Boot Block**
  - Top and bottom boot in the same device
- **Flexible sector architecture**
  - Eight 8 Kbytes, thirty 64 Kbytes, and eight 8 Kbytes sectors
- **Manufactured on 0.17 µm process technology**
- **SecSi (Secured Silicon) Sector (256 Bytes)**
  - *Factory locked and identifiable*: 16 bytes for secure, random factory Electronic Serial Number; remainder may be customer data programmed by AMD
  - *Customer lockable:* Can be read, programmed or erased just like other sectors. Once locked, data cannot be changed
- **Programmable Burst interface**
  - Interface to any high performance processor
  - Modes of Burst Read Operation:

    Linear Burst: 4 double words (x32), 8 words (x16) and double words (x32), and 32 words (x16) with wrap around

    Interleaved Burst: 2, 4, and 8 doubleword (x32) interleaved burst with wrap around

    Continuous Linear burst: x16 and x32 data bus
- **Single power supply operation**
  - Optimized for 2.3 to 2.75 volt read, erase, and program operations
- **Compatibility with JEDEC standards (JC42.4)**
  - Software compatible with single-power supply Flash
  - Backward-compatible with AMD Am29LV and Am29F flash memories

PERFORMANCE CHARACTERISTICS

- **High performance read access**
  - Initial/random access times as fast as 54 ns
  - Burst access time as fast as 8 ns
- **Ultra low power consumption**
  - Burst Mode Read: 90 mA @ 66 MHz max
  - Program/Erase: 50 mA max
  - Standby mode: CMOS: 9 µA max
- **Minimum 1 million write cycles guaranteed per sector**
- **20 year data retention at 125°C**
- **VersatileI/O™ control**
  - Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{IO} pin
  - 1.65 V to 2.75 V compatible I/O signals

SOFTWARE FEATURES

- **Persistent Sector Protection**
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector (requires only V_{CC} levels)
- **Password Sector Protection**
  - A sophisticated sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector using a user-definable 64-bit password
- **Supports Common Flash Interface (CFI)**
- **Unlock Bypass Program Command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program or erase operation completion

HARDWARE FEATURES

- **Program Suspend/Resume & Erase Suspend/Resume**
  - Suspends program or erase operations to allow reading, programming, or erasing in same bank
- **Hardware Reset (RESET#), Ready/Busy# (RY/BY#), and Write Protect (WP#) inputs**
- **ACC input**
  - Accelerates programming time for higher throughput during system production
- **Package options**
  - 80-pin PQFP
  - 80-ball Fortified BGA

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GENERAL DESCRIPTION

The Am29BDD160 is a 16 Megabit, 2.5 Volt-only single power supply burst mode flash memory device. The device can be configured for either 1,048,576 words in 16-bit mode or 524,288 double words in 32-bit mode. The device can also be programmed in standard EPROM programmers. The device offers a configurable burst interface to 16/32-bit microprocessors and microcontrollers.

To eliminate bus contention, each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls. Additional control inputs are required for synchronous burst operations: Load Burst Address Valid (ADV#), and Clock (CLK).

Each device requires only a **single 2.5 or 2.6 Volt power supply** (2.3 V to 2.75 V) for both read and write functions. A 12.0-volt V_{PP} is not required for program or erase operations, although an acceleration pin is available if faster programming performance is required.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. The software command set is compatible with the command sets of the 5 V Am29F and 3 V Am29LV Flash families. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

The **Simultaneous Read/Write architecture** provides simultaneous operation by dividing the memory space into two banks. The device can begin programming or erasing in one bank, and then simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device provides a 256-byte **SecSi™ (Secured Silicon) Sector** with an one-time-programmable (OTP) mechanism.

In addition, the device features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups: **Persistent Sector Protection** is a command sector protection method that replaces the old 12 V controlled protection method; **Password Sector Protection** is a highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted; **WP# Hardware Protection** prevents program or erase in the two outermost 8 Kbytes sectors of the larger bank.

The device defaults to the Persistent Sector Protection mode. The customer must then choose if the Standard or Password Protection method is most desirable. The WP# Hardware Protection feature is always available, independent of the other protection method chosen.

The **VersatileI/O™ (V_{CCQ})** feature allows the output voltage generated on the device to be determined based on the V_{IO} level. This feature allows this device to operate in the 1.8 V I/O environment, driving and receiving signals to and from other 1.8 V devices on the same bus. In addition, inputs and I/Os that are driven externally are capable of handling 3.6 V.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, by reading the DQ7 (Data# Polling), or DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **password and software sector protection** feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system at V_{CC} level.

The **Program/Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunnelling. The data is programmed using hot electron injection.

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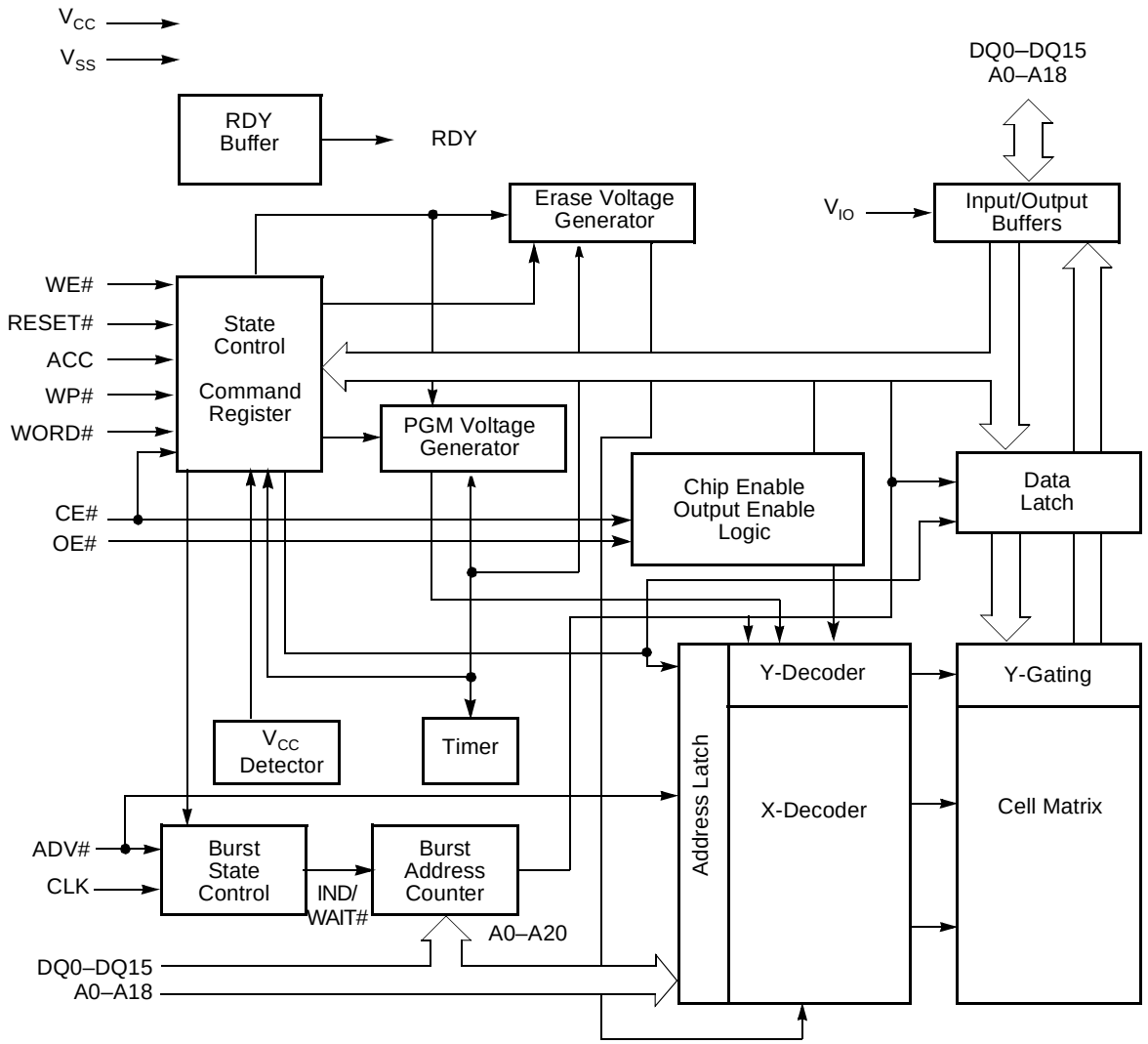
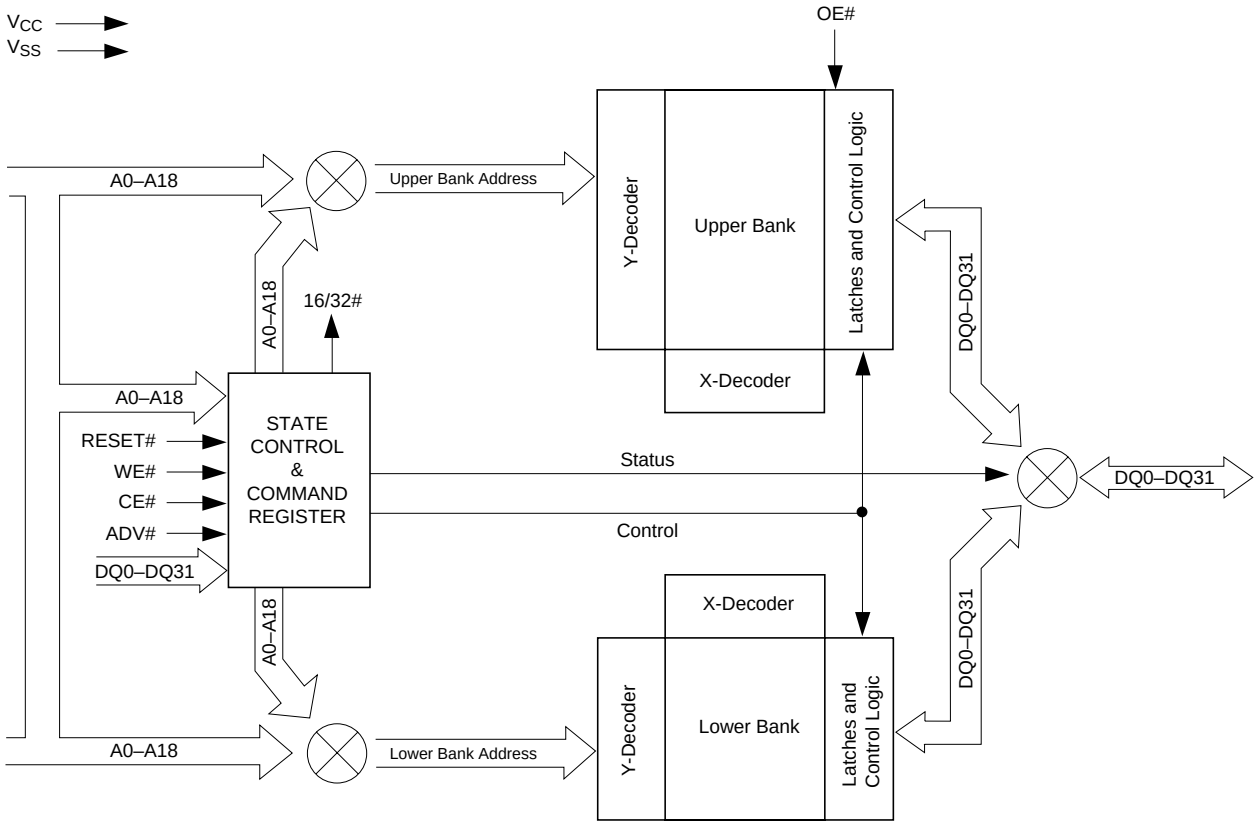
PRODUCT SELECTOR GUIDE

Part Number	Am29BDD160					
Standard Voltage Range: V_{CC} = 2.3 – 2.75 V	Synchronous/Burst or Asynchronous					
Speed Option (Clock Rate)	54D (66 MHz)	65D (66 MHz)	64C (56 MHz)	80C (56 MHz)	65A (40 MHz)	90A (40 MHz)
Max Initial/Asynchronous Access Time, ns (t_{ACC})	54	65	64	80	65	90
Max Burst Access Delay (ns)	8		10		17	
Max Clock Rate (MHz)	66		56		40	
Min Initial Clock Delay (clock cycles)	3	4	3	4	2	3
Max CE# Access, ns (t_{CE})	54	65	64	80	65	90
Max OE# Access, ns (t_{OE})	20					

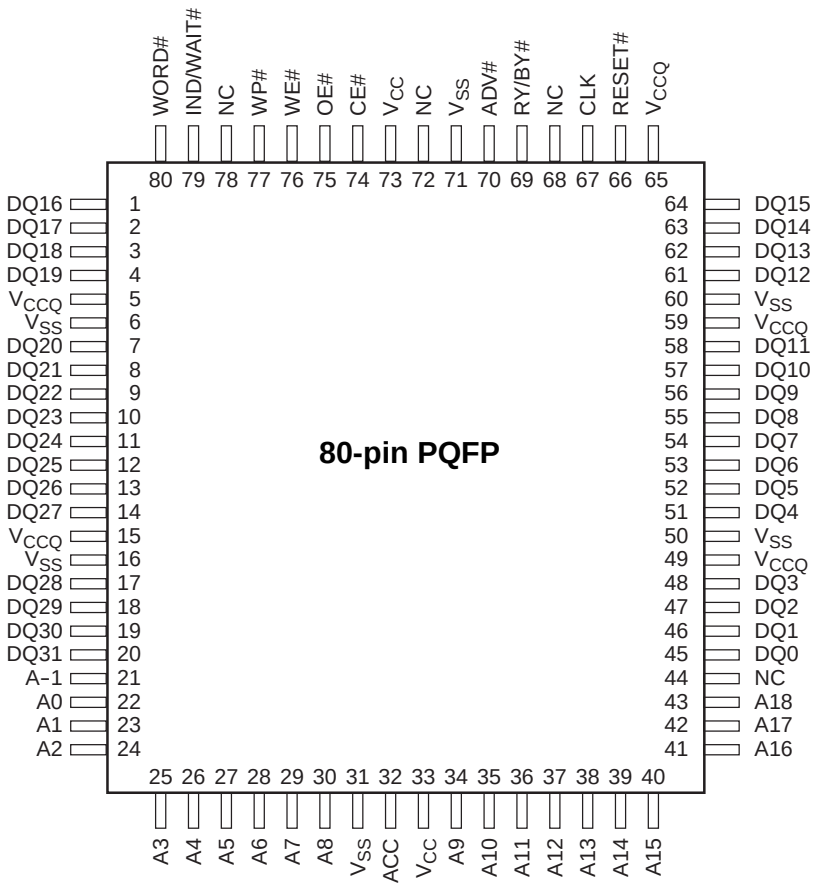
BLOCK DIAGRAM



BLOCK DIAGRAM OF SIMULTANEOUS OPERATION CIRCUIT

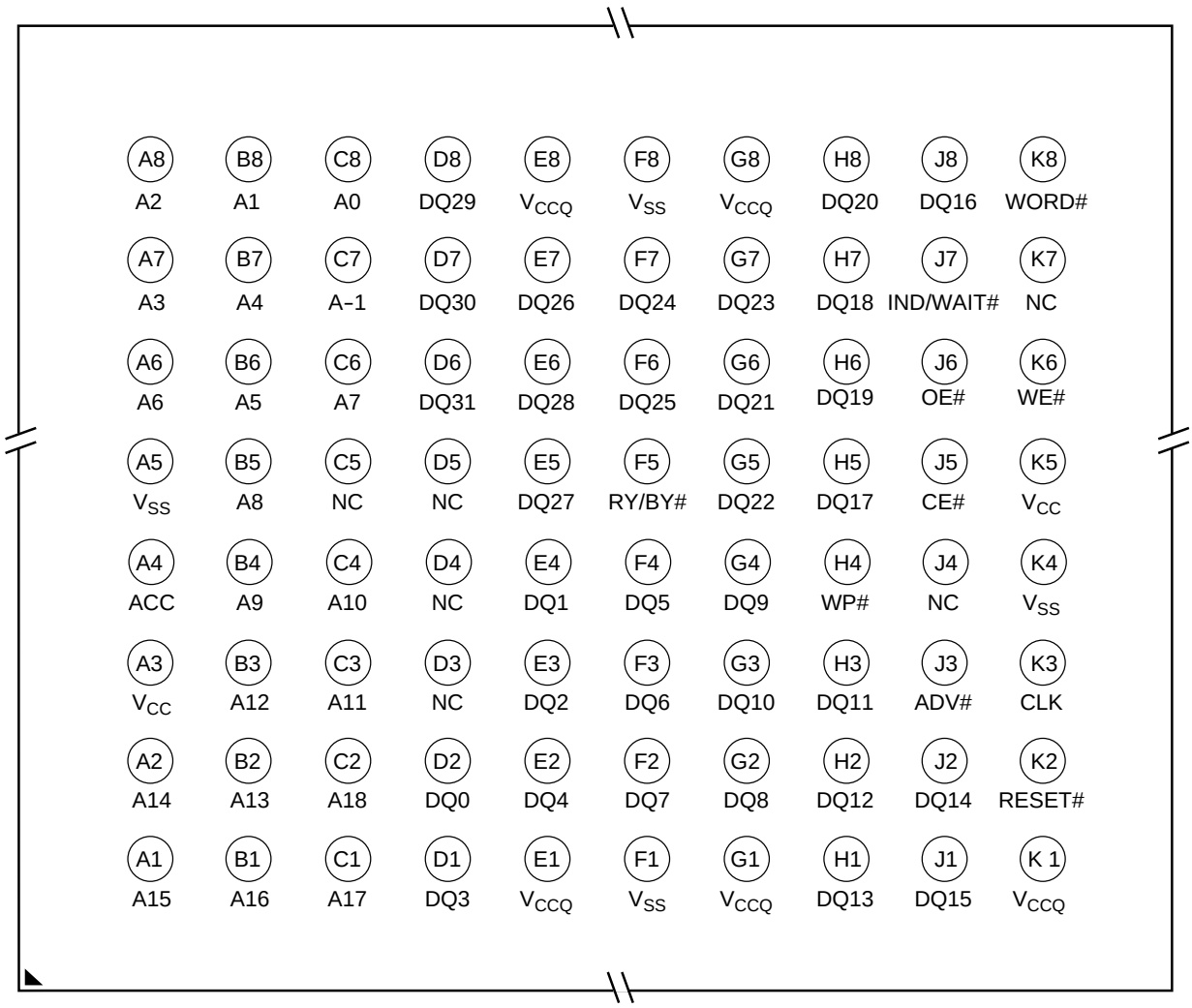


CONNECTION DIAGRAM



CONNECTION DIAGRAMS

80-Ball Fortified BGA



Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP, BGA, SSOP, PLCC, PDIP). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

A–1 = Least significant address bit for the 16-bit data bus, and selects between the high and low word. A –1 is not used for the 32-bit mode (WORD# = V_{IH}).

A0–A18 = 19-bit address bus for 16 Mb device. A9 supports 12 V autoselect inputs.

DQ0–DQ31 = 32-bit data inputs/outputs/float

WORD# = Selects 16-bit or 32-bit mode. When WORD# = V_{IH}, data is output on DQ31–DQ0. When WORD# = V_{IL}, data is output on DQ15–DQ0.

CE# = Chip Enable Input. This signal is asynchronous relative to CLK for the burst mode.

OE# = Output Enable Input. This signal is asynchronous relative to CLK for the burst mode.

WE# = Write enable. This signal is asynchronous relative to CLK for the burst mode.

V_{SS} = Device ground

NC = Pin not connected internally

RY/BY# = Ready/Busy output and open drain. When RY/BY# = V_{IH}, the device is ready to accept read operations and commands. When RY/BY# = V_{OL}, the device is either executing an embedded algorithm or the device is executing a hardware reset operation.

CLK = Clock Input that can be tied to the system or microprocessor clock and provides the fundamental timing and internal operating frequency.

ADV# = Load Burst Address input. Indicates that the valid address is present on the address inputs.

IND# = End of burst indicator for finite bursts only. IND is low when the last word in the burst sequence is at the data outputs.

WAIT# = Provides data valid feedback only when the burst length is set to continuous.

WP# = Write Protect input. When WP# = V_{OL}, the two outermost bootblock sector in the 75% bank are write protected regardless of other sector protection configurations.

ACC = Acceleration input. When taken to 12 V, program and erase operations are accelerated. When not used for acceleration, ACC = V_{SS} to V_{CC}.

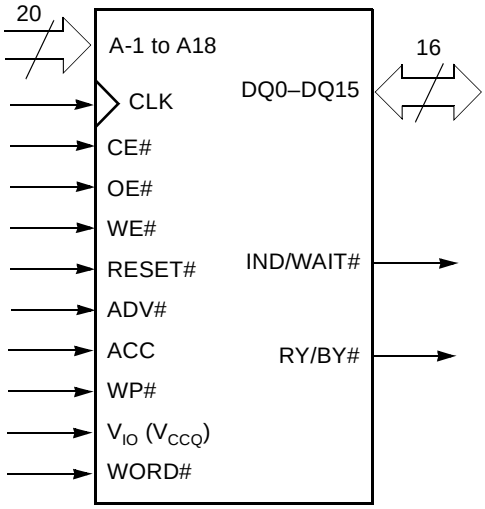
V_{IO} (V_{CCQ}) = Output Buffer Power Supply (1.65 V to 2.75 V)

V_{CC} = Chip Power Supply (2.3 V to 2.75 V)

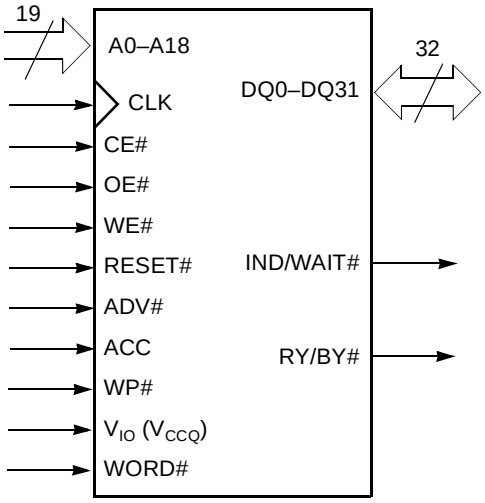
RESET# = Hardware reset input

LOGIC SYMBOLS

x16 Mode



x32 Mode



ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:

Am29BDD160 G T 54 D PB E

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)
E = Extended (–40°C to +125°C)

PACKAGE TYPE
K = 80-Pin Plastic Quad Flat Package (PQFP) PQR080
PB = 80-Ball Fortified Ball Grid Array (Fortified BGA)
1.0 mm pitch, 13 x 11 mm package (LAA080)

CLOCK RATE
A = 40 MHz
C = 56 MHz
D = 66 MHz

SPEED
(See Product Selector Guide and Valid Combinations)

BOOT CODE SECTOR ARCHITECTURE
T = Top Sector
B = Bottom Sector

PROCESS TECHNOLOGY
G = 0.17 µm

DEVICE NUMBER/DESCRIPTION
Am29BDD160
16 Megabit (2 M x 16-Bit/512 K x 32-Bit) CMOS 2.5 Volt-only Burst Mode, Dual Boot, Simultaneous Operation Flash Memory

Valid Combinations for PQFP Packages	
Am29BDD160GT54D Am29BDD160GB54D	KI, KE
Am29BDD160GT65D Am29BDD160GB65D	
Am29BDD160GT64C Am29BDD160GB64C	
Am29BDD160GT80C Am29BDD160GB80C	
Am29BDD160GT65A Am29BDD160GB65A	
Am29BDD160GT90A Am29BDD160GB90A	

Valid Combinations for Fortified BGA Packages			
Order Number		**Package Marking**	
Am29BDD160GT54D Am29BDD160GB54D	PBI, PBE	BD160GT54D BD160GB54D	I, E
Am29BDD160GT65D Am29BDD160GB65D		BD160GT65D BD160GB65D	
Am29BDD160GT64C Am29BDD160GB64C		BD160GT64C BD160GB64C	
Am29BDD160GT80C Am29BDD160GB80C		BD160GT80C BD160GB80C	
Am29BDD160GT65A Am29BDD160GB65A		BD160GT65A BD160GB65A	
Am29BDD160GT90A Am29BDD160GB90A		BD160GT90A BD160GB90A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operation

Operation		CE#	OE#	WE#	RESET#	CLK	ADV#	Addresses (Note 1)	Data (DQ0–DQ31)
Autoselect Manufacturer Code		L	L	H	H	X	X	A9 = V_{ID}, A6 = L, A1 = L, A0 = L	0000001h (Note 2)
Autoselect Device Code	Read Cycle 1	L	L	H	H	X	X	A9 = V_{ID}, A6 = L, A1 = L, A0 = H	000007Eh (Note 2)
	Read Cycle 2	L	L	H	H	X	X	A9 = V_{ID}, A7–A0 = 0Eh	0000008h
	Read Cycle 3	L	L	H	H	X	X	A9 = V_{ID}, A7–A0 = 0Fh	Top Boot Block 0000000h Bottom Boot Block 0000001h
Read		L	L	H	H	X	X	A_{IN}	D_{OUT}
Write		L	H	L	H	X	X	A_{IN}	D_{IN}
Standby (CE#)		H	X	X	H	X	X	X	HIGH Z
Output Disable		L	H	H	H	X	X	HIGH Z	HIGH Z
Reset		X	X	X	L	X	X	X	HIGH Z
PPB Protection Status (Note 4)		L	L	H	H	X	X	Sector Address, A9 = V_{ID}, A7 – A0 = 02h	00000001h, (protected) A6 = H 00000000h (unprotect) A6 = L
Burst Read Operations									
Load Starting Burst Address		L	X	H	H	↑	↓	A_{IN}	X
Advance Burst to next address with appropriate Data presented on the Data bus		L	L	H	H	↑	H	X	Burst Data Out
Terminate Current Burst Read Cycle		H	X	H	H	↑	X	X	HIGH Z
Terminate Current Burst Read Cycle with RESET#		X	X	H	L	X	X	X	HIGH Z
Terminate Current Burst Read Cycle; Start New Burst Read Cycle		L	H	H	H	↑	↓	A_{IN}	X

Legend:

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, X = Don't care.

Notes:

1. *DQ31–DQ16 are HIGH Z when WORD# = V_{IL}*
2. *When WORD# = V_{IL}, DQ31-DQ16 are floating*
3. *WP# controls the two outermost sectors of the top boot block or the two outermost sectors of the bottom boot block.*
4. *DQ0 reflects the sector PPB (or sector group PPB) and DQ1 reflects the DYB*
5. *Addresses are A0:A18 for the x32 mode and A–1:A18 for x16 mode.*

VersatileI/O™ (V_{IO}) Control

The VersatileI/O (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin.

The output voltage generated on the device is determined based on the V_{IO} (V_{CCQ}) level.

A V_{IO} of 1.65–1.95 volts is targeted to provide for I/O tolerance at the 1.8 volt level.

A V_{CC} and V_{IO} of 2.3–2.75 volts makes the device appear as 2.5 volt-only.

Address/Control signals are 3.6 V tolerant with the exception of CLK.

Word/Double Word Configuration

The WORD# pin controls whether the device data I/O pins operate in the word or double word configuration. If the WORD# pin is set at V_{IH}, the device is in double word configuration, DQ31–DQ0 are active and controlled by CE# and OE#.

If the WORD# pin is set at V_{IL}, the device is in word configuration, and only data I/O pins DQ15–DQ0 are active and controlled by CE# and OE#. The data I/O pins DQ31–DQ16 are tri-stated.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

Address access time (t_{ACC}) is the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable CE# to valid data at the output pins. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output pins (assuming the addresses have been stable for at least $t_{ACC}–t_{OE}$ time and CE# has been asserted for at least $t_{CE}–t_{OE}$ time).

See “Reading Array Data” for more information. Refer to the AC Read Operations table for timing specifications and to Figure 20 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Simultaneous Read/Write Operations With Zero Latency

The device is capable of reading data from one bank of memory while programming or erasing in the other bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Refer to the DC Characteristics table for read-while-program and read-while-erase current specifications.

Simultaneous read/write operations are valid for both the main Flash memory array and the SecSi OTP sector. Simultaneous operation is disabled during the CFI and Password Program/Verify operations. PPB Program/Erase operations and the Password Unlock operation permit reading data from the large (75%) bank while reading the operation status of these commands from the small (25%) bank.

Table 2. Top Boot Bank Select

Bank	A18:A17
Bank 1	00
Bank 2	01, 1X

Table 3. Bottom Boot Bank Select

Bank	A18
Bank 1	0X, 10
Bank 2	11

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, in the x32-mode the device accepts program data in 32-bit words and in the x16 mode the device accepts program data in 16-bit words.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The Sector Erase and Program Suspend Command section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 11 and 12 indicate the address space that each sector occupies. A “sector address” consists of the address bits required to uniquely select a sector. The “Command Definitions”

section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timing applies in this mode. Refer to the “Autoselect Mode” section for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for erase or program modes. The AC Characteristics section contains timing specification tables and timing diagrams for erase or program operations.

Accelerated Program and Erase Operations

The device offers accelerated program/erase operations through the ACC pin. When the system asserts V_{HH} (12V) on the ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence to do accelerated programming. The device uses the higher voltage on the ACC pin to accelerate the operation. A sector that is being protected with the WP# pin will still be protect during accelerated program or Erase. *Note that the ACC pin must not be at V_{HH} during any operation other than accelerated programming, or device damage may result.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when CE# is held at $V_{CC} \pm 0.3$ V and V_{CC} is held at V_{CC}(max). The device requires standard access time (t_{CE}) for read access when the device is in standby mode before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. I_{CC5} in the DC Characteristics table represents the standby current specification.

The second standby mode, $I_{CC7,}$ is entered by applying V_{IL} on the RESET# and CE# pins. I_{CC7} is entered anytime regardless of the logical condition of the CE# pin. Caution: entering the standby mode via the RESET# pin also resets the device to the read mode and floats the data I/O pins. Furthermore, entering I_{CC7} during a program or erase operation will leave erroneous data in the address locations being operated on at the time of the RESET# pulse. These locations require updating after the device resumes standard operations. Refer to the “RESET#: Hardware Reset Pin” section for further discussion of the RESET# pin and its functions.

RESET#: Hardware Reset Pin

The RESET# pin is an active low signal that is used to reset the device under any circumstances. A logic “0” on this pin forces the device out of any mode that is currently executing back to the reset state. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device. To avoid a potential bus contention during a system reset, the device is isolated from the DQ data bus by tristating the data output pins for the duration of the RESET pulse. All pins are “don’t care” during the reset operation.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains low until the reset operation is internally complete. This action requires between 1 µs and 7µs for either Chip Erase or Sector Erase. The RY/BY# pin can be used to determine when the reset operation is complete. Otherwise, allow for the maximum reset time of 20 µs. If RESET# is asserted when a program or erase operation is not executing (RY/BY# = “1”), the reset operation will complete within 500 ns. Since the Am29BDD160 is a Simultaneous Operation device the user may read a bank after 500 ns if the bank was in the read/reset mode at the time RESET# was asserted. If one of the banks was in the middle of either a program or erase operation when RESET# was asserted, the user must wait 20 µs before accessing that bank.

Asserting RESET# during a program or erase operation leaves erroneous data stored in the address locations being operated on at the time of device reset. These locations need updating after the reset operation is complete. See Figure 24 for timing specifications.

Asserting RESET# active during V_{CC} and V_{IO} power-up is required to guarantee proper device initialization until V_{CC} and V_{IO} have reached their steady state voltages.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled, and the output pins are placed in the high impedance (floating) state.

Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins A6, A1, and A0 must be as shown in Table 11 (top boot devices) or Table 12 (bottom boot devices). In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Tables 11 and 12). Table 4 shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command. This method does not require V_{ID}. See "Command Definitions" for details on using the autoselect mode.

Table 4. Am29BDD160 Autoselect Codes (High Voltage Method)

Description		CE#	OE#	WE#	A18 to A11	A10	A9	A8	A7	A6	A5 to A4	A3	A2	A1	A0	DQ7 to DQ0
Manufacturer ID: AMD		L	L	H	X	X	V_{ID}	X	X	L	X	X	X	L	L	0001h
Autoselect Device Code	Read Cycle 1	L	L	H	X	X	V_{ID}	X	L	L	X	L	L	L	H	007Eh
	Read Cycle 2	L	L	H	X	X	V_{ID}	X	L	L	L	H	H	H	L	0008h
	Read Cycle 3	L	L	H	X	X	V_{ID}	X	L	L	L	H	H	H	H	0000h (top boot block)
																0001h (bottom boot block)
PPB Protection Status		L	L	H	SA	X	V_{ID}	X	L	L	L	L	L	H	L	0000h (unprotected)
																0001h (protected)

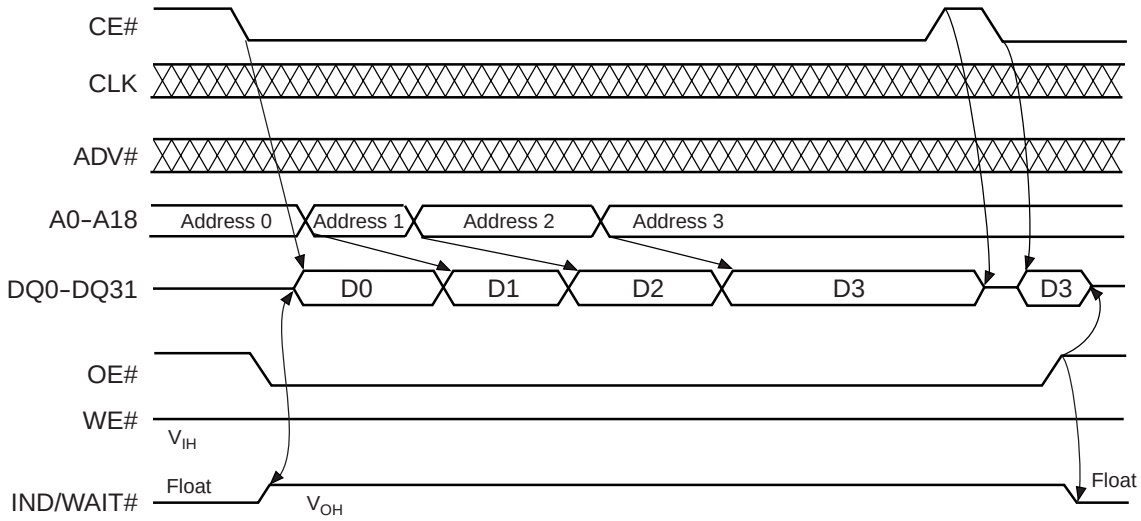
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care.

Note: *The autoselect codes may also be accessed in-system via command sequences. See Tables 18 and 20.*

Asynchronous Read Operation (Non-Burst)

The device has two control functions which must be satisfied in order to obtain data at the outputs. CE# is the power control and should be used for device selection. OE# is the output control and should be used to gate data to the output pins if the device is selected. The device is power-up in an asynchronous read mode. In the asynchronous mode the device has two control functions which must be satisfied in order to obtain data at the outputs. CE# is the power control and should be used for device selection. OE# is the output control and should be used to gate data to the output pins if the device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output pins. The output enable access time is the delay from the falling edge of OE# to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).



Note: *Operation is shown for the 32-bit data bus. For the 16-bit data bus, A-1 is required.*

Figure 1. Asynchronous Read Operation

Synchronous (Burst) Read Operation

The Am29BDD160 is capable of performing burst read operations to improve total system data throughput. The device is available in three burst modes of operation: linear, interleaved, and continuous sequential burst mode. 2, 4 and 8 double word (x32) and 4 and 8 word (x16) accesses are configurable as either sequential or x86 interleave burst accesses. 16 and 32 word (x16) accesses are only configurable as linear burst accesses. Attempting to configure a 16 or 32 word (x16) access as an interleave access results in the device forcing the Burst Sequence bit in the Configuration Register to Linear Burst Order (See “Configuration Register” for more information). Additional options for all burst modes include initial access delay configurations (1–15 CLKs), data hold for either 1 or 2 CLKs, and whether the data is presented on either the rising or falling edge of the CLK signal. Device configuration for burst mode operation is accomplished by writing the Configuration Register with the desired burst configuration information. Once the Configuration Register is written to enable burst mode operation, all subsequent reads from the array are returned using the burst mode protocols. Like the main memory access, the SecSi Sector memory is accessed with the same burst or asynchronous timing as defined in the Configuration Register. However, the user must recognize that continuous burst operations past the 256 byte SecSi boundary returns invalid data.

Burst read operations occur only to the main flash memory arrays. The Configuration Register and protection bits are treated as single cycle reads, even when burst mode is enabled. Read operations to these locations results in the data remaining valid while OE# is at V_{IL}, regardless of the number of CLK cycles applied to the device.

Linear And Interleaved Burst Read Operations

Linear burst read mode reads either 4, 8, 16, or 32 words (1 word = 16 bits), depending upon the Configuration Register option. If the device is configured with a 32 bit interface (WORD# = V_{IH}), the burst access is comprised of 4 clocked reads for 8 words and 16 clocked reads for 32 words (See Table 5 for all valid burst output sequences). The number of clocked reads is doubled when the device is configured in the 16-bit data bus mode (WORD# = V_{IL}). The IND/WAIT# pin transitions active (V_{IL}) during the last transfer of data during a linear or interleaved burst read before a wrap around, indicating that the system should initiate another ADV# to start the next burst access. If the system continues to clock the device, the next access wraps around to the starting address of the previous burst access. The IND/WAIT# signal remains inactive (floating) when not active.

The Am29BDD160 burst contains the burst option for either linear addressing or x86 interleaved burst accesses. X86 interleave is limited to 2, 4, or 8 double-word (x32) configurations. When interleaved, the data is presented in an 8-byte block addressing order. See Table 5 for a complete 32 and 16 bit data bus interface order. Only 2, 4, and 8 word configurations have the option for x86 interleave burst sequence. 16 and 32 word options are restricted to sequential burst accesses, only.

Table 5. 16-Bit and 32-Bit Linear and Interleaved Burst Data Order

Data Transfer Sequence (Independent of the WORD# pin)	Output Data Sequence (Initial Access Address) (x16/ x32)
Two Linear and Interleaved Data Transfers, (x32 only)	0-1 (A0 = 0) 1-0 (A0 = 1)
Four Linear Data Transfers	0-1-2-3 (A0:A-1/A1-A0 = 00) 1-2-3-0 (A0:A-1/A1-A0 = 01) 2-3-0-1 (A:A-1/A1-A0 = 10) 3-0-1-2 (A0:A-1/A1-A0 = 11)
Four Interleaved Data Transfers	0-1-2-3 (A0:A-1/A1-A0 = 00) 1-0-3-2 (A0:A-1/A1-A0 = 01) 2-3-0-1 (A0:A-1/A1-A0 = 10) 3-2-1-0 (A0:A-1/A1-A0 = 11)
Eight Linear Data Transfers	0-1-2-3-4-5-6-7 (A1:A-1A2-A0 = 000) 1-2-3-4-5-6-7-0 (A1:A-1/A2-A0 = 001) 2-3-4-5-6-7-0-1 (A1:A-1/A2-A0 = 010) 3-4-5-6-7-0-1-2 (A1:A-1/A2-A0 = 011) 4-5-6-7-0-1-2-3 (A1:A-1/A2-A0 = 100) 5-6-7-0-1-2-3-4 (A1:A-1/A2-A0 = 101) 6-7-0-1-2-3-4-5 (A1:A-1/A2-A0 = 110) 7-0-1-2-3-4-5-6 (A1:A-1/A2-A0 = 111)
Eight Interleaved Data Transfers	0-1-2-3-4-5-6-7 (A1:A-1/ A2-A0 = 000) 1-0-3-2-5-4-7-6 (A1:A-1/ A2-A0 = 001) 2-3-0-1-6-7-4-5 (A1:A-1/ A2-A0 = 010) 3-2-1-0-7-6-5-4 (A1:A-1/ A2-A0 = 011) 4-5-6-7-0-1-2-3 (A1:A-1/ A2-A0 = 100) 5-4-7-6-1-0-3-2 (A1:A-1/ A2-A0 = 101) 6-7-4-5-2-3-0-1 (A1:A-1/ A2-A0 = 110) 7-6-5-4-3-2-1-0 (A1:A-1/ A2-A0 = 111)
Sixteen Linear Data Transfers	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F (A2:A-1/ A3-A0 = 0000) 1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0 (A2:A-1/ A3-A0 = 0001) 2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1 (A2:A-1/ A3-A0 = 0010) 3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2 (A2:A-1/ A3-A0 = 0011) 4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3 (A:A-1/ A3-A0 = 0100) 5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4 (A2:A-1/ A3-A0 = 0101) 6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5 (A2:A-1/ A3-A0 = 0110) 7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6 (A2:A-1/ A3-A0 = 0111) 8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7 (A2:A-1/ A3-A0 = 1000) 9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8 (A2:A-1/ A3-A0 = 1001) A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9 (A2:A-1/ A3-A0 = 1010) B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A (A2:A-1/ A3-A0 = 1011) C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B (A2:A-1/ A3-A0 = 1100) D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C (A2:A-1/ A3-A0 = 1101) E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D (A2:A-1/ A3-A0 = 1110) F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E (A2:A-1/ A3-A0 = 1111)

Table 5. 16-Bit and 32-Bit Linear and Interleaved Burst Data Order (Continued)

Data Transfer Sequence (Independent of the WORD# pin)	Output Data Sequence (Initial Access Address) (x16/ x32)
Thirty-Two Linear Data Transfers (x16 only)	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-G-H-I-J-K-L-M-N-O-P-Q-R-S-T-U-V (A3:A-1 = 00000) 1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-G-H-I-J-K-L-M-N-O-P-Q-R-S-T-U-V-0 (A3:A-1 = 00001) : U-V-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-G-H-I-J-K-L-M-N-O-P-Q-R-S-T (A3:A-1 = 11110) V-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-G-H-I-J-K-L-M-N-O-P-Q-R-S-T-U (A3:A-1 = 11111)

CE# Control in Linear or Interleave Mode

The CE# (Chip Enable) pin enables the Am29BDD160 during read mode operations. CE# must meet the required burst read setup times for burst cycle initiation. If CE# is taken to V_{IH} at any time during the burst linear or burst cycle, the device immediately exits the burst sequence and floats the DQ bus and IND/WAIT# signal. Restarting a burst cycle is accomplished by taking CE# and ADV# to V_{IL}.

ADV# Control In Linear or Interleave Mode

The ADV# (Address Valid) pin is used to initiate a linear or interleave burst cycle at the clock edge when CE# and ADV# are at V_{IL} and the device is configured for either linear or interleave burst mode operation. A burst access is initiated and the address is latched on the first rising (or falling, depending upon the CR6 configuration register setting) CLK edge when ADV# is active or upon a rising ADV# edge, whichever occurs first. If the ADV# signal is taken to V_{IL} prior to the end of a linear or interleave burst sequence, the previous address is discarded and subsequent burst transfers are invalid until ADV# transitions to V_{IH} before a clock edge, which initiates a new burst sequence.

RESET# Control in Linear or Interleave Mode

The RESET# pin immediately halts the linear or interleave burst access when taken to V_{IL}. The DQ data bus and IND/WAIT# signal float. Additionally, the Configuration Register contents are reset back to the default condition where the device is placed in asynchronous access mode.

OE# Control in Linear or Interleave Mode

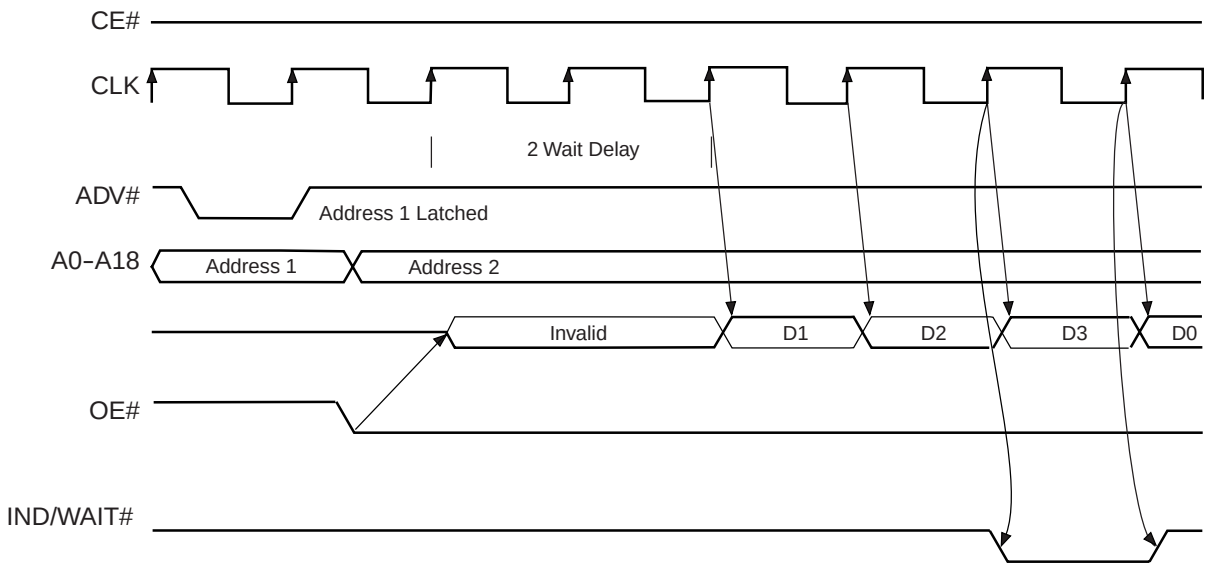
The OE# (Output Enable) pin is used to enable the linear or interleave burst data on the DQ data bus and the IND/WAIT# pin. De-asserting the OE# pin to V_{IH} during a burst operation floats the data bus and the IND/WAIT# pin. However, the device will continue to operate internally as if the burst sequence continues until the linear or interleave burst is complete. The OE# pin does not halt the burst sequence, this is accomplished by either taking CE# to V_{IH} or re-issuing a new ADV# pulse. The DQ bus and IND/WAIT# signal remain in the float state until OE# is taken to V_{IL}.

IND/WAIT# Operation in Linear or Interleave Mode

The IND/WAIT#, or End of Burst Indicator signal (when in linear or x86 interleave modes), informs the system that the last address of a burst sequence is on the DQ data bus. For example, if a 4-word linear or x86 interleave burst access is enabled using a 16-bit DQ bus (WORD# = V_{IL}), the IND/WAIT# signal transitions active on the fourth access. If the same scenario is used, but instead the 32-bit DQ bus is enabled, the IND/WAIT# signal transitions active on the second access. The IND/WAIT# signal has the same delay and setup timing as the DQ pins. Also, the IND/WAIT# signal is controlled by the OE# signal. If OE# is at V_{IH}, the IND/WAIT# signal floats and is not driven. If OE# is at V_{IL}, the IND/WAIT# signal is driven at V_{IH} until it transitions to V_{IL} indicating the end of burst sequence. The IND/WAIT# signal timing and duration is controlled by WC (WAIT#), CC (Clock Configuration), and DOC (Data Output Configuration) bits in the Configuration Register (See “Configuration Register” for more information). The following table lists the valid combinations of the Configuration Register bits that impact the IND/WAIT# timing.

Table 6. Valid Configuration Register Bit Definition for IND/WAIT#

DOC	WC	CC	Definition
0	0	0	IND/WAIT# = V_{IL} for 1-CLK cycle, Active on last transfer, Driven on falling CLK edge
0	0	1	IND/WAIT# = V_{IL} for 1-CLK cycle, Active on last transfer, Driven on rising CLK edge
0	1	0	IND/WAIT# = V_{IL} for 1-CLK cycle, Active on second to last transfer, Driven on falling CLK edge
0	1	1	IND/WAIT# = V_{IL} for 1-CLK cycle, Active on second to last transfer, Driven on rising CLK edge
1	0	0	IND/WAIT# = V_{IL} for 2-CLK cycles, Active on last transfer, Driven on falling CLK edge
1	0	1	IND/WAIT# = V_{IL} for 2-CLK cycles, Active on last transfer, Driven on rising CLK edge
1	1	0	IND/WAIT# = V_{IL} for 2-CLK cycles, Active on second to last transfer, Driven on falling CLK edge
1	1	1	IND/WAIT# = V_{IL} for 2-CLK cycles, Active on second to last transfer, Driven on rising CLK edge



Note: *Operation is shown for the 32-bit data bus. For a 16-bit data bus, A-1 is required. Figure shown with 1-CLK initial access delay configuration, linear address, 4-doubleword burst, output on rising CLK edge, data hold for 1-CLK, IND/WAIT# asserted on the last transfer before wrap-around.*

Figure 2. End of Burst Indicator (IND/WAIT#) Timing for Linear or Interleaved 8-Word Burst Operation

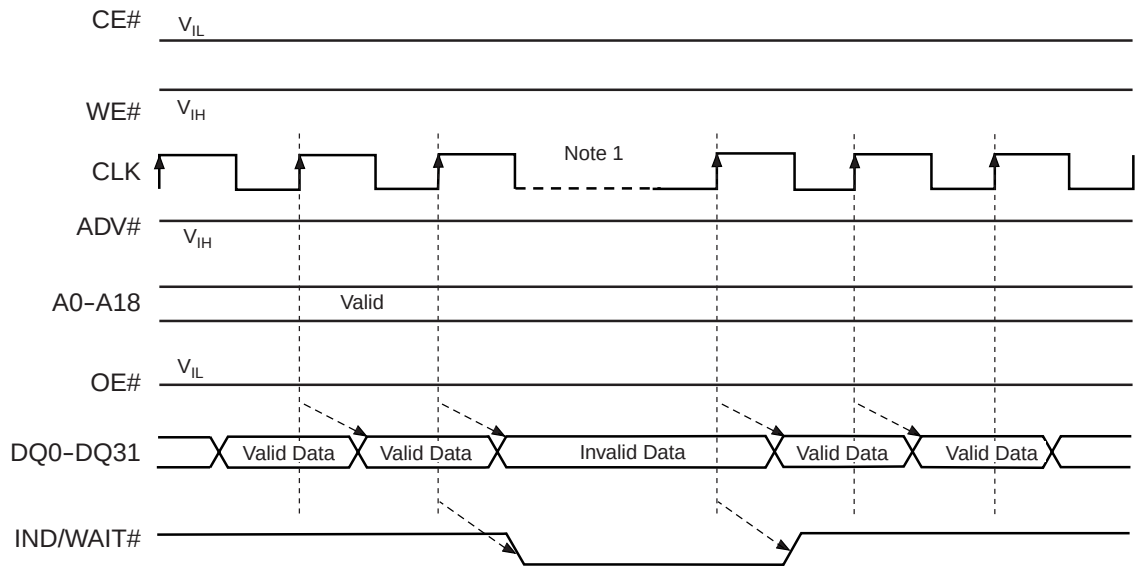
Continuous Burst Read Operations

In addition to linear and interleaved burst read options, the Am29BDD160 is available with a continuous burst read option. This continuous burst read option is a sequential address (no interleave capability) that reads through the entire address range of the device. If the ADV# signal is not asserted, the device will roll back at the lowest order address (00000h) from the highest order address (7FFFFh). Continuous burst operation forces the device to perform an initial read access every time the address crosses a row boundary. When this boundary condition occurs, the IND/WAIT# pin goes low, indicating that the data is invalid until the IND/WAIT# signal transitions back to high. The IND/WAIT# signal remains high when the device is in continuous burst mode.

If an odd starting address is applied to the Am29BDD160, the device presents the first data transfer after the selected number of wait cycles. However, the IND/WAIT# pin will transition low to indicate a wait condition until the device has time to internally align accesses on an even address boundary (see Figure 3). The duration of the IND/WAIT# active low time is no greater than an initial access time. Once aligned, the device will continue to present data at the optimal burst rate until the end of a row is encountered, at which time, the IND/WAIT# signal transitions low. Even starting addresses do not require an early

alignment requiring the IND/WAIT# pin to transition after the first data transfer.

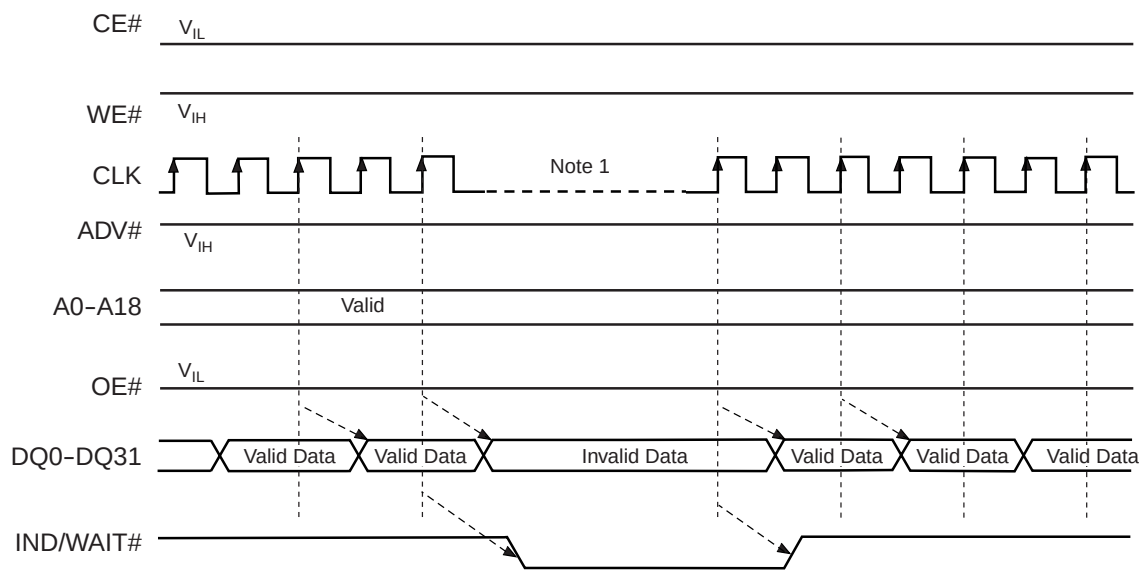
While it is acceptable to read from the SecSi OTP sector while configured for continuous burst reads, the user must take into account that data past the 256 byte boundary and before the next sector boundary returns invalid data. While the simultaneous read/write function is being used, a continuous burst read that crosses a bank boundary returns neither array data nor autoselect data. If the simultaneous read/write function is not being used, a continuous burst read returns valid data from the entire array.



Notes:

1. Delay is variable, but will not exceed t_{ACC}.

Figure 3. Wait Function During Continuous Burst Reads at Wordline (Row) Boundary



Note: *Delay is variable, but will not exceed t_{ACC}.*

Figure 4. Wait Function During Continuous Burst Reads at Wordline (Row) Boundary, 2-CLK Option

CE# Control in Continuous Burst Read Mode

The CE# (Chip Enable) pin enables the device during read mode operations. CE# must meet the required burst read setup times for burst cycle initiation. If CE# is taken to V_{IH} at any time during the continuous burst cycle, the device immediately exits the burst sequence and floats the DQ bus and IND/WAIT# signal. Restarting a burst cycle is accomplished by taking CE# and ADV# to V_{IL}.

ADV# Control in Continuous Burst Read Mode

The ADV# (Address Valid) pin is used to initiate a continuous burst cycle when CE# is at V_{IL} and the device is configured for continuous burst accesses. A burst access is initiated and the address is latched on the first rising (or falling, depending upon the CR6 configuration register setting) CLK edge when ADV# is active or upon a rising ADV# edge, whichever occurs first. If the ADV# signal is taken to V_{IL} the previous starting address is discarded and subsequent burst transfers are invalid until ADV# transition to V_{IH}, which re-initiates the burst sequence.

RESET# Control in Continuous Burst Read Mode

The RESET# pin immediately halts the continuous burst access when taken to V_{IL}. The DQ bus and IND/WAIT# signal float. Additionally, the Configuration Register contents are reset back to the default condition where the device is placed in asynchronous access mode.

OE# Control In Continuous Burst Read Mode

The OE# (Output Enable) pin is used to enable the continuous burst data on the DQ bus and the IND/WAIT# pin. De-asserting the OE# pin to V_{IH} during a burst operation floats the DQ bus and the IND/WAIT# pin. However, the device will continue to operate internally as if the burst sequence continues in continuous burst mode. The OE# pin does not halt the burst sequence, this is accomplished by either taking CE# to V_{IH} or re-issuing a new ADV# pulse. The DQ bus and IND/WAIT# signal remain in the float state until OE# is taken to V_{IL}.

IND/WAIT# Operation in Continuous Mode

The IND/WAIT#, or End of Row Access Indicator/Wait signal, informs the system that the next burst access requires reading from the next continuous row. The Am29BDD160 perform an initial read access from the next row (wordline) which requires additional time. The IND/WAIT# signal is available to inform the system when this boundary condition occurs. The device will assert IND/WAIT# until the next row is read and the data is available for reading by the system. The IND-WAIT# signal will transition to V_{IH} when the next sequential word or double word (depending upon the status of WORD#) is valid. When the device is configured for continuous burst read operations, the OE# signal will float the IND/WAIT# signal when OE# is at V_{IH}. When OE# is at V_{IL}, the output drives the IND/WAIT# status to either V_{IH} or V_{IL}.

The IND/WAIT# function has the option of going active during a continuous burst either at the time of the burst delay or one CLK before the time of the burst delay, depending upon bit 8 (WC) in the Control Register (CR8). If the WC (Wait# Configuration) bit is set to a “1”, the IND/WAIT# is shifted up by one data transfer and will transition inactive when the device drives the last data transfer of the wordline (row). If bit 8 is cleared (=0), then IND/WAIT# transitions low at the start of the burst delay. If bit 8 is set (=1), then IND/WAIT# transitions low one CLK before the start of the burst delay. The default configuration is bit 8 cleared after reset.

If the user starts a continuous burst access on an odd address boundary (A0 = 1 for x32, A_{-1} = 1 for x16), the device will insert an additional IND/WAIT# pulse after the first data transfer in addition to the IND/WAIT# pulse when the device crosses to a new row. This additional IND/WAIT# pulse allows the device to synchronize the internal access to an even column address, thus insuring a smooth row transition.

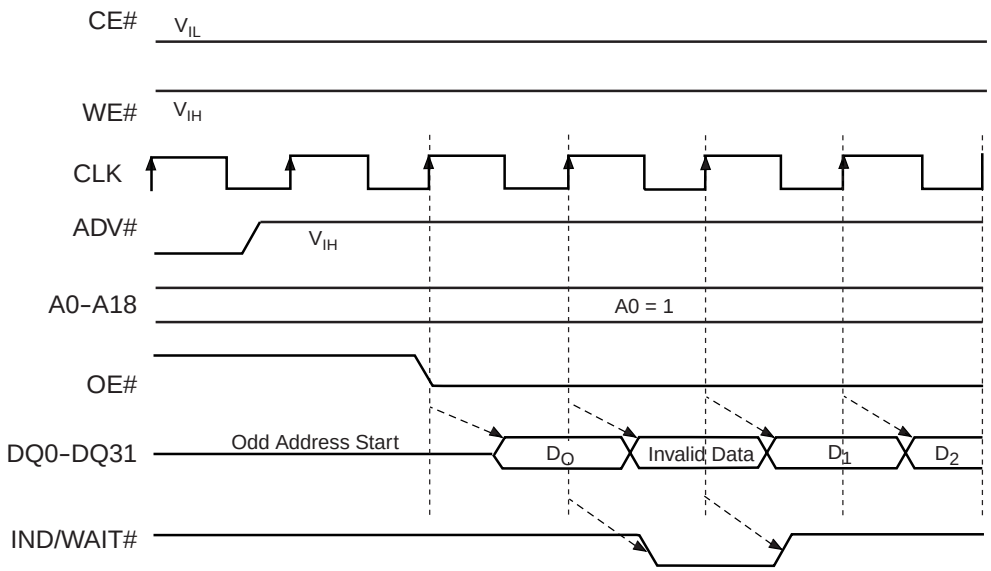


Figure 5. Odd Starting Address Continuous Burst Mode Alignment

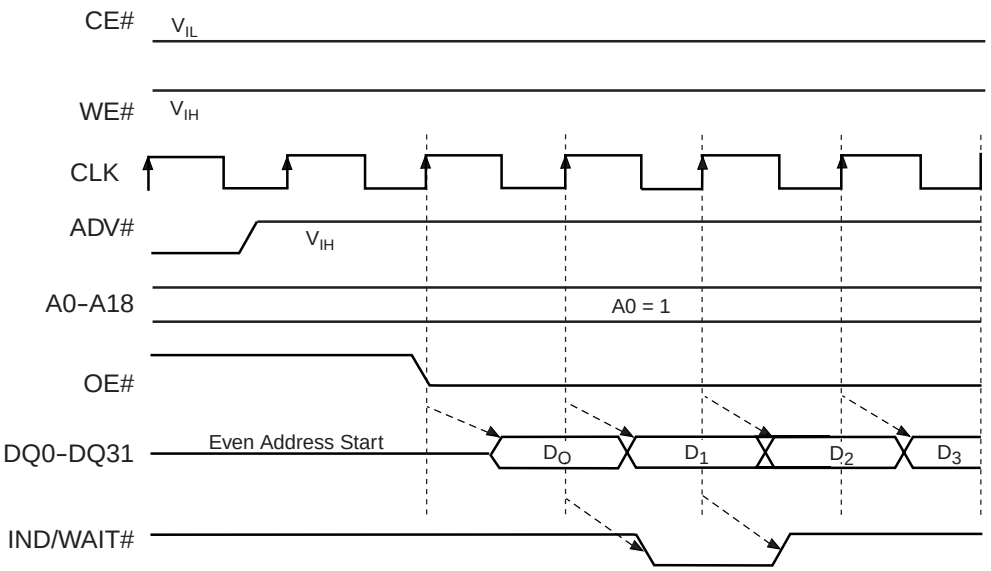


Figure 6. Even Starting Address Continuous Burst Mode Alignment

Burst Access Timing Control

In addition to the IND/WAIT# signal control, burst controls exist in the Control Register for initial access delay, delivery of data on the CLK edge, and the length of time data is held.

Burst Initial Access Delay Control

The Am29BDD160 contains options for initial access delay of a burst access. The initial access delay has no effect on asynchronous read operations. Below is a table describing the initial access delay definitions if the Clock Configuration bit in the Control Register (CR6 = 1):

Table 7. Burst Initial Access Delay Control

CR13	CR12	CR11	CR10	Setting #	Definition
0	0	0	0	0	Data is valid after the 2nd rising CLK edge after ADV# goes high
0	0	0	1	1	Data is valid after the 3rd rising CLK edge after ADV# goes high
0	0	1	0	2	Data is valid after the 4th rising CLK edge after ADV# goes high
0	0	1	1	3	Data is valid after the 5th rising CLK edge after ADV# goes high
0	1	0	0	4	Data is valid after the 6th rising CLK edge after ADV# goes high
0	1	0	1	5	Data is valid after the 7th rising CLK edge after ADV# goes high
0	1	1	0	6	Data is valid after the 8th rising CLK edge after ADV# goes high
0	1	1	1	7	Data is valid after the 9th rising CLK edge after ADV# goes high—Default

The burst access is initiated and the address is latched on the first rising CLK edge when ADV# is active or upon a rising ADV# edge, whichever comes first. If the Clock Configuration bit in the Control Register is set to falling edge (CR6 = 0), the definition remains the same for the initial delay setting with the exception that data is valid after the falling edge. For example, for Setting 0, data is valid after the 1st falling CLK edge after ADV# goes high. ADV# must still meet the rising edge timing of CLK.

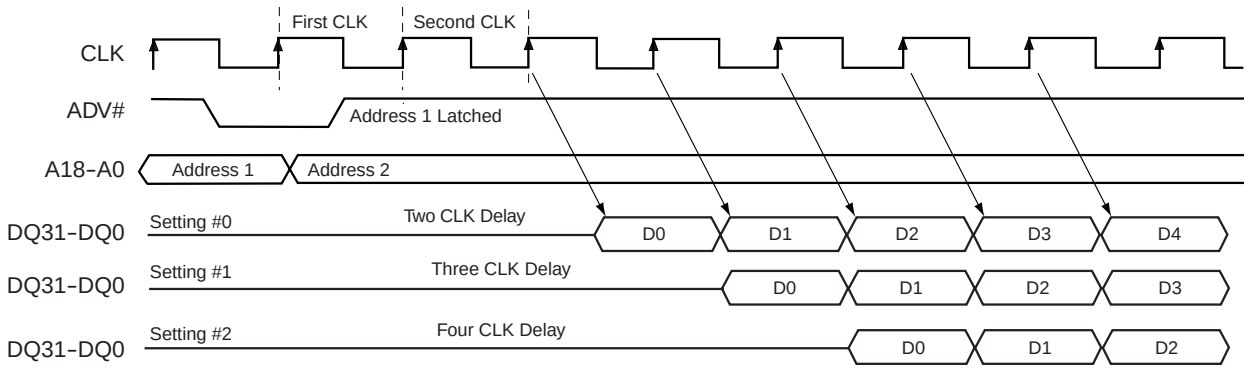


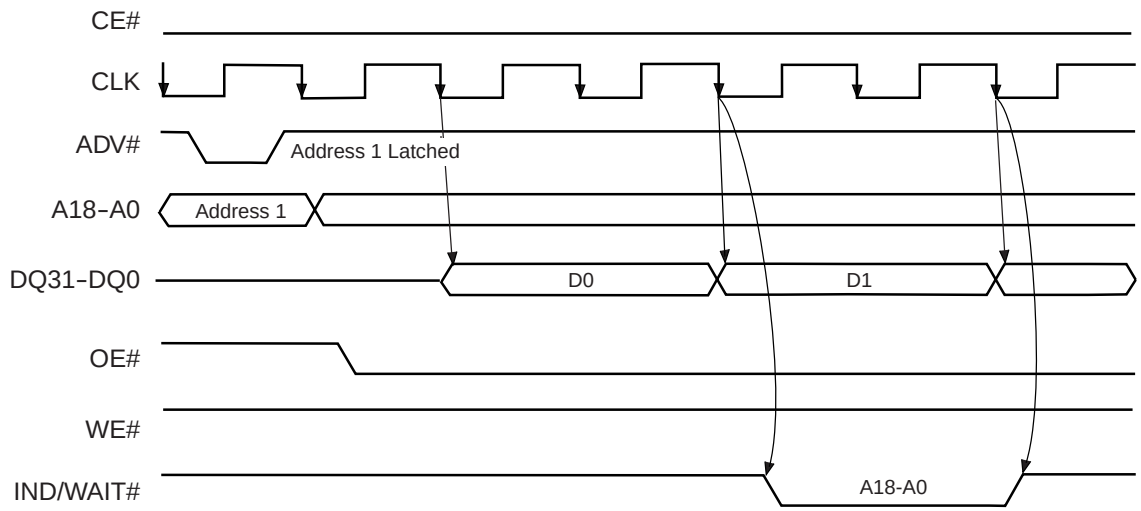
Figure 7. Initial Burst Delay Showing One and Two CLK Delays

Burst CLK Edge Data Delivery

The Am29BDD160 is capable of delivering data on either the rising or falling edge of CLK. To deliver data on the rising edge of CLK, bit 6 in the Control Register (CR6) is set to 1. To deliver data on the falling edge of CLK, bit 6 in the Control Register is cleared to 0. The default configuration is set to the rising edge.

Burst Data Hold Control

The device is capable of holding data for either one or two CLKs, depending upon the state of bit 9 in the Control Register (CR9). If bit 9 of the Control Register is cleared, data on DQ0–DQ31 (when WORD# = V_{IH}) is held for one CLK. If bit 9 is set to a 1, then data is held for two CLK cycles. The default configuration is to hold data for one CLK.



Note: *Operation is shown for the 32-bit data bus. For 16-bit data bus, A-1 is required. Figure shown with 1 CLK initial access delay configuration, linear address, 4-Word burst, output on falling CLK edge, Data hold for 2 CLK, IND/WAIT# asserted on last access before wrap-around. Also, the actual wait period is dependent upon the CLK frequency. The higher the CLK frequency, the greater the number of CLK cycles.*

Figure 8. Falling CLK Edge Output and Two-CLK Data Hold

Asserting RESET# During A Burst Access

If RESET# is asserted low during a burst access, the burst access is immediately terminated and the device defaults back to asynchronous read mode. Refer to RESET#: Hardware Reset Pin for more information on the RESET# function.

Configuration Register

The Am29BDD160 contains a Configuration Register for configuring read accesses. The Configuration Register is accessed by the Configuration Register Read and the Configuration Register Write commands. The Configuration Register does not occupy any addressable memory location, but rather, is accessed by the Configuration Register commands. The Configuration Register is readable any time, however, writing the Configuration Register is restricted to times when the Embedded Algorithm™ is not active. If the user attempts to write the Configuration Register while the Embedded Algorithm™ is active, the write operation is ignored and the contents of the Configuration Register remain unchanged.

The Configuration Register is a 16 bit data field which is accessed by DQ15–DQ0. Data on DQ31–DQ16 is ignored during a write operation when WORD# = V_{IL}. During a read operation, DQ31–DQ16 returns all zeroes. Table 8 shows the Configuration Register. Also, Configuration Register reads operate the same as Autoselect command reads. When the command is issued, the bank address is latched along with the command. Reads operations to the bank that was specified during the Configuration Register read command return Configuration Register contents. Read operations to the other bank return flash memory data. Either bank address is permitted when writing the Configuration Register read command.

Table 8. Configuration Register Definitions

CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
RM	Reserved	IAD3	IAD2	IAD1	IAD0	DOC	WC

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
BS	CC	Reserved	Reserved	Reserved	BL2	BL1	BL0

Configuration Register
CR15 = Read Mode (RM) 0 = Synchronous Burst Reads Enabled 1 = Asynchronous Reads Enabled (Default)
CR14 = Reserved for Future Enhancements These bits are reserved for future use. Set these bits to “0”.

Table 8. Configuration Register Definitions (Continued)

CR13–CR10 = Initial Access Delay Configuration (IAD3-IAD0)

Initial Access Delay (Rising Edge Data Delivery)

0000 = Data is valid after 2nd rising CLK edge after ADV# transitions to V_{IH}
0001 = Data is valid after 3rd rising CLK edge after ADV# transitions to V_{IH}
0010 = Data is valid after 4th rising CLK edge after ADV# transitions to V_{IH}
0011 = Data is valid after 5th rising CLK edge after ADV# transitions to V_{IH}
0100 = Data is valid after 6th rising CLK edge after ADV# transitions to V_{IH}
0101 = Data is valid after 7th rising CLK edge after ADV# transitions to V_{IH}
0110 = Data is valid after 8th rising CLK edge after ADV# transitions to V_{IH}
0111 = Data is valid after 9th rising CLK edge after ADV# transitions to V_{IH}—Default

Initial Access Delay (Falling Edge Data Delivery)

0000 = Data is valid after 2nd falling CLK edge after ADV# transitions to V_{IH}
0001 = Data is valid after 3rd falling CLK edge after ADV# transitions to V_{IH}
0010 = Data is valid after 4th falling CLK edge after ADV# transitions to V_{IH}
0011 = Data is valid after 5th falling CLK edge after ADV# transitions to V_{IH}
0100 = Data is valid after 6th falling CLK edge after ADV# transitions to V_{IH}
0101 = Data is valid after 7th falling CLK edge after ADV# transitions to V_{IH}
0110 = Data is valid after 8th falling CLK edge after ADV# transitions to V_{IH}
0111 = Data is valid after 9th falling CLK edge after ADV# transitions to V_{IH}—Default

CR9 = Data Output Configuration (DOC)
0 = Hold Data for 1-CLK cycle—Default
1 = Hold Data for 2-CLK cycles

CR8 = IND/WAIT# Configuration (WC)
0 = IND/WAIT# Asserted During Delay—Default
1 = IND/WAIT# Asserted One Data Cycle Before Delay

CR7 = Burst Sequence (BS)
0 = Interleaved Burst Order (x86) for 4 and 8 word (x16) and 2, 4, and 8 doubleword (x32) bursts
1 = Linear Burst Order—Default

CR6 = Clock Configuration (CC)
0 = Burst Starts and Data Output on Falling Clock Edge
1 = Burst Starts and Data Output on Rising Clock Edge—Default

CR5–CR3 = Reserved For Future Enhancements (R)
These bits are reserved for future use. Set these bits to “0.”

CR2–CR0 = Burst Length (BL2–BL0)
000 = Reserved, burst accesses disabled (asynchronous reads only)
001 = 64 bit (8-byte) Burst Data Transfer - x16 and x32 Linear and Interleave
010 = 128 bit (16-byte) Burst Data Transfer - x16 and x32 Linear and Interleave
011 = 256 bit (32-byte) Burst Data Transfer - x16 Linear Only and x32 Linear and Interleave
100 = 512 bit (64-byte) Burst Data Transfer - x16 and x32 Linear Only - Default
101 = Reserved, burst accesses disabled (asynchronous reads only)
110 = Reserved, burst accesses disabled (asynchronous reads only)
111 = Continuous Burst Operation - x16 and x32 Linear Only

Table 9. Configuration Register After Device Reset

CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
RM	Reserve	IAD3	IAD2	IAD1	IAD0	DOC	WC
1	0	0	1	1	1	0	0

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
BS	CC	Reserve	Reserve	Reserve	BL2	BL1	BL0
1	1	0	0	0	1	0	0

Initial Access Delay Configuration

The frequency configuration informs the device of the number of clocks that must elapse after ADV# is driven active before data will be available. This value is determined by the input clock frequency.

SECTOR PROTECTION

The Am29BDD160 features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

Persistent Sector Protection

A command sector protection method that replaces the old 12 V controlled protection method.

Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted

WP# Hardware Protection

A write protect pin that can prevent program or erase to the two outermost 8 Kbytes sectors in the 75% bank

All parts default to operate in the Persistent Sector Protection mode. The customer must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method will be used. If the customer decides to continue using the Persistent Sector Protection method, they must set the **Persistent Sector Protection Mode Locking Bit**. This will permanently set the part to operate only using Persistent Sector Protection. If the customer decides to use the password method, they must set the **Password Mode Locking Bit**. This will permanently set the part to operate only using password sector protection.

It is important to remember that setting either the **Persistent Sector Protection Mode Locking Bit** or the **Password Mode Locking Bit** permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit has been set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states:

- **Persistently Locked**—A sector is protected and cannot be changed.
- **Dynamically Locked**—The sector is protected and can be changed by a simple command
- **Unlocked**—The sector is unprotected and can be changed by a simple command

In order to achieve these states, three types of “bits” are going to be used:

Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum of four sectors (see the sector address tables for specific sector protection groupings). All 8 Kbyte boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the **PPB Write Command**.

Note: If a PPB requires erasure, all of the sector PPBs must first be preprogrammed prior to PPB erasing. All PPBs erase in parallel, unlike programming where in-

dividual PPBs are programmable. It is the responsibility of the user to perform the preprogramming operation. Otherwise, an already erased sector PPBs has the potential of being over-erased. There is no hardware mechanism to prevent sector PPBs over-erasure.

Persistent Protection Bit Lock (PPB Lock)

A global volatile bit. When set to “1”, the PPBs cannot be changed. When cleared (“0”), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is “0”. Each DYB is individually modifiable through the DYB Write Command.

When the parts are first shipped, the PPBs are cleared, the DYBs are cleared, and PPB Lock is defaulted to power up in the cleared state – meaning the PPBs are changeable.

When the device is first powered on the DYBs power up cleared (sectors not protected). The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPBs cleared, the DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Write command sequences, the DYBs will be set or cleared, thus placing each sector in the protected or unprotected state. These are the so-called **Dynamic Locked or Unlocked** states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

The PPBs allow for a more static, and difficult to change, level of protection. The PPBs retain their state across power cycles because they are Non-Volatile. Individual PPBs are set with a command but must all be cleared as a group through a complex sequence of program and erasing commands. The PPBs are limited to 100 erase cycles.

The PPB Lock bit adds an additional level of protection. Once all PPBs are programmed to the desired settings, the PPB Lock may be set to “1”. Setting the PPB Lock disables all program and erase commands to the Non-Volatile PPBs. In effect, the PPB Lock Bit locks the PPBs into their current state. The only way to clear the PPB Lock is to go through a power cycle. System boot code can determine if any changes to the PPB are needed e.g. to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock to disable any further changes to the PPBs during system operation.

The WP# write protect pin adds a final level of hardware protection to the two outermost 8 Kbytes sectors in the 75% bank. When this pin is low it is not possible to change the contents of these two sectors.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Write command sequence is all that is necessary. The DYB write command for the dynamic sectors switch the DYBs to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock bit must be disabled by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB lock bit once again will lock the PPBs, and the device operates normally again.

Note: to achieve the best protection, it’s recommended to execute the PPB lock bit set command early in the boot code, and protect the boot code by holding WP# = V_{IL}.

Table 10. Sector Protection Schemes

DYB	PPB	PPB Lock	Sector State
0	0	0	Unprotected—PPB and DYB are changeable
0	0	1	Unprotected—PPB not changeable, DYB is changeable
0	1	0	Protected—PPB and DYB are changeable
1	0	0	
1	1	0	
0	1	1	Protected—PPB not changeable, DYB is changeable
1	0	1	
1	1	1	

Table 10 contains all possible combinations of the DYB, PPB, and PPB lock relating to the status of the sector.

In summary, if the PPB is set, and the PPB lock is set, the sector is protected and the protection can not be removed until the next power cycle clears the PPB lock. If the PPB is cleared, the sector can be dynamically locked or unlocked. The DYB then controls whether or not the sector is protected or unprotected.

If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program command to a protected sector enables status polling for approximately 1 µs before the device returns to read mode without having modified the contents of the protected sector. An erase command to a protected sector enables status polling for approximately 50 µs after which the device returns to read mode without having erased the protected sector.

The programming of the DYB, PPB, and PPB lock for a given sector can be verified by writing a DYB/PPB/PPB lock verify command to the device.

Persistent Sector Protection Mode Locking Bit

Like the password mode locking bit, a Persistent Sector Protection mode locking bit exists to guarantee that the device remain in software sector protection. Once set, the Persistent Sector Protection locking bit prevents programming of the password protection mode locking bit. This guarantees that an unauthorized user could not place the device in password protection mode.

Password Protection Mode

The Password Sector Protection Mode method allows an even higher level of security than the Persistent Sector Protection Mode. There are two main differences between the Persistent Sector Protection and the Password Sector Protection Mode:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock bit set to the **locked state**, rather than cleared to the unlocked state.
- The only means to clear the PPB Lock bit is by writing a unique **64-bit Password** to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a **one-time programmable (OTP)** region of the flash memory. Once the Password Mode Locking Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear the PPB Lock bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock bit is cleared, and the PPBs can be altered. If they do not match, the flash device does nothing. There is a built-in 2 µs delay for each “password check.” This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

Password and Password Mode Locking Bit

In order to select the Password sector protection scheme, the customer must first program the password. One method of choosing a password would be to correlate it to the unique Electronic Serial Number (ESN) of the particular flash device. Another method could generate a database where all the passwords are stored, each of which correlates to a serial number on the device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Verify operations.

Once the desired password is programmed in, the customer must then set the Password Mode Locking Bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. It also disables *all further commands* to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Protection method is desired when setting the Password Mode Locking Bit. More importantly, the user must be sure that the password is correct when the Password Mode Locking Bit is set. Due to the fact that read operations are disabled, there is no means to verify what the password is afterwards. If the password is lost after setting the Password Mode Locking Bit, there will be no way to clear the PPB Lock bit.

The Password Mode Locking Bit, once set, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Mode Locking Bit is not erasable. Once Password Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

64-bit Password

The 64-bit Password is located in its own memory space and is accessible through the use of the Password Program and Verify commands (see Password Verify Command). The password function works in conjunction with the Password Mode Locking Bit, which when set, prevents the Password Verify command from reading the contents of the password on the pins of the device.

Write Protect (WP#)

The device features a hardware protection option using a write protect pin that prevents programming or erasing, regardless of the state of the sector's Persistent or Dynamic Protection Bits. The WP# pin is associated with the two outermost 8Kbytes sectors in the 75% bank. The WP# pin has no effect on any other sector. When WP# is taken to V_{IL}, programming and erase operations of the two outermost 8 Kbytes sectors in the 75% bank are disabled. By taking WP# back to V_{IH}, the two outermost 8 Kbytes sectors are enabled for program and erase operations, depending upon the status of the individual sector Persistent or Dynamic Protection Bits. If either of the two outermost sectors Persistent or Dynamic Protection Bits are programmed, program or erase operations are inhibited. If the sector Persistent or Dynamic Protection Bits are both erased, the two sectors are available for programming or erasing as long as WP# remains at V_{IH}. The user must hold the WP# pin at either V_{IH} or V_{IL} during the entire program or erase operation of the two outermost sectors in the 75% bank.

SecSi™ (Secured Silicon) Sector Protection

The SecSi Sector is a 256-byte flash memory area that is either programmable at the customer or by AMD at the request of the customer. The SecSi Sector Entry command enables the host system to address the SecSi Sector for programming or reading. The SecSi sector address range is 00000h–0003Fh for the top bootblock configuration and 7FFC0h–7FFFFh for the bottom bootblock configuration. Address range 00040h–007FFh for the top bootblock and 7F800h–7FFBFh return invalid data when addressed with the SecSi sector enabled.

Unlike previous flash memory devices, the Am29BDD160 allows simultaneous operation while the SecSi sector is enabled. However, there are a number of restrictions associated with simultaneous operation and device operation when the SecSi sector is enabled:

1. The SecSi sector is not available for reading while the Password Unlock, any PPB program/erase operation, or Password programming are in progress. Reading to any location in the small (25%) sector will return the status of these operations until these operations have completed execution.
2. Writing the corresponding DYB associated with the overlaid bootblock sector results in the DYB NOT being updated. This is only accomplished when the SecSi sector is not enabled.
3. Reading the corresponding DYB associated with the overlaid bootblock sector results in reading invalid data when the PPB Lock/DYB Verify command is issued. This function is only accomplished when the SecSi sector is not enabled.
4. All commands are available for execution when the SecSi sector is enabled except the following list. Issuing the following commands while the SecSi sector is enabled results in the command being ignored.

- All Unlock Bypass commands
- CFI
- Accelerated Program
- Program and Sector Erase Suspend
- Program and Sector Erase Resume

5. Executing the Sector Erase command is permitted when the SecSi sector is enabled, however, there is no provision for erasing the SecSi sector with the Sector Erase command, regardless of the protection status. The Sector Erase command will erase all other sectors when the SecSi sector is enabled.

6. Executing the Chip Erase command is permitted when the SecSi sector is enabled. The Chip Erase command erases all sectors in the memory array except for sector 0 in top-bootblock configuration and sector 45 in bottom-bootblock configuration. The SecSi Sector is a one-time programmable memory area that cannot be erased.
7. Executing the SecSi Sector Entry command during program or erase suspend mode is allowed. The Sector Erase/Program Resume command is disabled while the SecSi sector is enabled, and the user cannot resume programming of the memory array until the Exit SecSi Sector command is written.

SecSi Sector Protection Bit

The SecSi Sector Protection Bit prevents programming of the SecSi sector memory area. Once set, the SecSi sector memory area contents are non-modifiable.

Persistent Protection Bit Lock

The Persistent Protection Bit (PPB) Lock is a volatile bit that reflects the state of the Password Mode Locking Bit after power-up reset. If the Password Mode Locking Bit is set, which indicates the device is in Password Protection Mode, the PPB Lock Bit is also set after a hardware reset (RESET# asserted) or a power-up reset. The ONLY means for clearing the PPB Lock Bit in Password Protection Mode is to issue the Password Unlock command. Successful execution of the Password Unlock command clears the PPB Lock Bit, allowing for sector PPBs modifications. Asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit back to a “1”.

If the Password Mode Locking Bit is not set, indicating Persistent Sector Protection Mode, the PPB Lock Bit is cleared after power-up or hardware reset. The PPB Lock Bit is set by issuing the PPB Lock Bit Set command. Once set the only means for clearing the PPB Lock Bit is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Sector Protection Mode.

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal erase/program circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE#, or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH}, or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero (V_{IL}) while OE# is a logical one (V_{IH}).

Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power-up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

V_{CC} and V_{IO} Power-up And Power-down Sequencing

The device imposes no restrictions on V_{CC} and V_{IO} power-up or power-down sequencing. Asserting RESET# to V_{IL} is required during the entire V_{CC} and V_{IO} power sequence until the respective supplies reach their operating voltages. Once, V_{CC} and V_{IO} attain their respective operating voltages, de-assertion of RESET# to V_{IH} is permitted.

Table 11. Sector Addresses for Top Boot Sector Devices

	Sector	Sector Group	x16 Address Range (A18:A-1)	x32 Address Range (A18:A0)	Sector Size (Kwords)
Bank 1 (Note 2)	SA0 (Note 1)	SG0	00000h-00FFFh	00000h-007FFh	4
	SA1	SG1	01000h-01FFFh	00800h-00FFFh	4
	SA2	SG2	02000h-02FFFh	01000h-017FFh	4
	SA3	SG3	03000h-03FFFh	01800h-01FFFh	4
	SA4	SG4	04000h-04FFFh	02000h-027FFh	4
	SA5	SG5	05000h-05FFFh	02800h-02FFFh	4
	SA6	SG6	06000h-06FFFh	03000h-037FFh	4
	SA7	SG7	07000h-07FFFh	03800h-03FFFh	4
	SA8	SG8	08000h-0FFFFh	04000h-07FFFh	32
	SA9		10000h-17FFFh	08000h-0BFFFh	32
	SA10		18000h-1FFFFh	0C000h-0FFFFh	32
	SA11	SG9	20000h-27FFFh	10000h-13FFFh	32
	SA12		28000h-2FFFFh	14000h-17FFFh	32
	SA13		30000h-37FFFh	18000h-1BFFFh	32
	SA14		38000h-3FFFFh	1C000h-1FFFFh	32
Bank 2 (Note 2)	SA15	SG10	40000h-47FFFh	20000h-23FFFh	32
	SA16		48000h-4FFFFh	24000h-27FFFh	32
	SA17		50000h-57FFFh	28000h-2BFFFh	32
	SA18		58000h-5FFFFh	2C000h-2FFFFh	32
	SA19	SG11	60000h-67FFFh	30000h-33FFFh	32
	SA20		68000h-6FFFFh	34000h-37FFFh	32
	SA21		70000h-77FFFh	38000h-3BFFFh	32
	SA22		78000h-7FFFFh	3C000h-3FFFFh	32
	SA23	SG12	80000h-87FFFh	40000h-43FFFh	32
	SA24		88000h-8FFFFh	44000h-47FFFh	32
	SA25		90000h-97FFFh	48000h-4BFFFh	32
	SA26		98000h-9FFFFh	4C000h-4FFFFh	32
	SA27	SG13	A0000h-A7FFFh	50000h-53FFFh	32
	SA28		A8000h-AFFFFh	54000h-57FFFh	32
	SA29		B0000h-B7FFFh	58000h-5BFFFh	32
	SA30		B8000h-BFFFFh	5C000h-5FFFFh	32
	SA31	SG14	C0000h-C7FFFh	60000h-63FFFh	32
	SA32		C8000h-CFFFFh	64000h-67FFFh	32
	SA33		D0000h-D7FFFh	68000h-6BFFFh	32
	SA34		D8000h-DFFFFh	6C000h-6FFFFh	32
	SA35	SG15	E0000h-E7FFFh	70000h-73FFFh	32
	SA36		E8000h-EFFFFh	74000h-77FFFh	32
	SA37		F0000h-F7FFFh	78000h-7BFFFh	32
	SA38	SG16	F8000h-F8FFFh	7C000h-7C7FFh	4
	SA39	SG17	F9000h-F9FFFh	7C800h-7CFFFh	4
	SA40	SG18	FA000h-FAFFFh	7D000h-7D7FFh	4
	SA41	SG19	FB000h-FBFFFh	7D800h-7DFFFh	4
	SA42	SG20	FC000h-FCFFFh	7E000h-7E7FFh	4
	SA43	SG21	FD000h-FDFFFh	7E800h-7EFFFh	4
	SA44 (Note 3)	SG22	FE000h-FEFFFh	7F000h-7F7FFh	4
	SA45 (Note 3)	SG23	FF000h-FFFFFh	7F800h-7FFFFh	4

Notes:

1. *SecSi Sector overlays this sector when enabled.*
2. *The bank address is determined by A18 and A17. BA = 00 for Bank 1 and BA = 01, 10, or 11 for Bank 2.*
3. *This sector has the additional WP# pin sector protection feature.*

Table 12. Sector Addresses for Bottom Boot Sector Devices

	Sector	Sector Group	x16 Address Range (A18:A-1)	x32 Address Range (A18:A0)	Sector Size (Kwords)
Bank 1 (Note 2)	SA0 (Note 1)	SG0	00000h-00FFFh	00000h-007FFh	4
	SA1 (Note 1)	SG1	01000h-01FFFh	00800h-00FFFh	4
	SA2	SG2	02000h-02FFFh	01000h-017FFh	4
	SA3	SG3	03000h-03FFFh	01800h-01FFFh	4
	SA4	SG4	04000h-04FFFh	02000h-027FFh	4
	SA5	SG5	05000h-05FFFh	02800h-02FFFh	4
	SA6	SG6	06000h-06FFFh	03000h-037FFh	4
	SA7	SG7	07000h-07FFFh	03800h-03FFFh	4
	SA8	SG8	08000h-0FFFFh	04000h-07FFFh	32
	SA9		10000h-17FFFh	08000h-0BFFFh	32
	SA10		18000h-1FFFFh	0C000h-0FFFFh	32
	SA11	SG9	20000h-27FFFh	10000h-13FFFh	32
	SA12		28000h-2FFFFh	14000h-17FFFh	32
	SA13		30000h-37FFFh	18000h-1BFFFh	32
	SA14		38000h-3FFFFh	1C000h-1FFFFh	32
	SA15	SG10	40000h-47FFFh	20000h-23FFFh	32
	SA16		48000h-4FFFFh	24000h-27FFFh	32
	SA17		50000h-57FFFh	28000h-2BFFFh	32
	SA18		58000h-5FFFFh	2C000h-2FFFFh	32
	SA19	SG11	60000h-67FFFh	30000h-33FFFh	32
	SA20		68000h-6FFFFh	34000h-37FFFh	32
	SA21		70000h-77FFFh	38000h-3BFFFh	32
	SA22		78000h-7FFFFh	3C000h-3FFFFh	32
	SA23	SG12	80000h-87FFFh	40000h-43FFFh	32
	SA24		88000h-8FFFFh	44000h-47FFFh	32
	SA25		90000h-97FFFh	48000h-4BFFFh	32
	SA26		98000h-9FFFFh	4C000h-4FFFFh	32
	SA27	SG13	A0000h-A7FFFh	50000h-53FFFh	32
	SA28		A8000h-AFFFFh	54000h-57FFFh	32
	SA29		B0000h-B7FFFh	58000h-5BFFFh	32
	SA30		B8000h-BFFFFh	5C000h-5FFFFh	32
Bank 2 (Note 2)	SA31	SG14	C0000h-C7FFFh	60000h-63FFFh	32
	SA32		C8000h-CFFFFh	64000h-67FFFh	32
	SA33		D0000h-D7FFFh	68000h-6BFFFh	32
	SA34		D8000h-DFFFFh	6C000h-6FFFFh	32
	SA35	SG15	E0000h-E7FFFh	70000h-73FFFh	32
	SA36		E8000h-EFFFFh	74000h-77FFFh	32
	SA37		F0000h-F7FFFh	78000h-7BFFFh	32
	SA38	SG16	F8000h-F8FFFh	7C000h-7C7FFh	4
	SA39	SG17	F9000h-F9FFFh	7C800h-7CFFFh	4
	SA40	SG18	FA000h-FAFFFh	7D000h-7D7FFh	4
	SA41	SG19	FB000h-FBFFFh	7D800h-7DFFFh	4
	SA42	SG20	FC000h-FCFFFh	7E000h-7E7FFh	4
	SA43	SG21	FD000h-FDFFFh	7E800h-7EFFFh	4
	SA44	SG22	FE000h-FEFFFh	7F000h-7F7FFh	4
	SA45 (Note 3)	SG23	FF000h-FFFFFh	7F800h-7FFFFh	4

Notes:

1. *This sector has the additional WP# pin sector protection feature.*
2. *The bank address is determined by A18 and A17. BA = 00, 01, or 10 for Bank 1 and BA = 11 for Bank 2.*
3. *SecSi Sector overlays this sector when enabled.*

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 13–16. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 13–16. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/products/nvd/overview/cfi.html. Alternatively, contact an AMD representative for copies of these documents.

Table 13. CFI Query Identification String

Addresses (x32 Mode)	Addresses (x16 Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 14. CFI System Interface String

Addresses (x32 Mode)	Addresses (x16 Mode)	Data	Description
1Bh	36h	0023h	V_{CC} Min. (write/erase) DQ7–DQ4: volts, DQ3–DQ0: 100 millivolt
1Ch	38h	0027h	V_{CC} Max. (write/erase) DQ7–DQ4: volts, DQ3–DQ0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0004h	Typical timeout per single word/doubleword program 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer program 2^N µs (00h = not supported)
21h	42h	0009h	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for word/doubleword program 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0007h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 15. CFI Device Geometry Definition

Addresses (x32 Mode)	Addresses (x16 Mode)	Data	Description
27h	4Eh	0015h	Device Size = 2^N byte
28h 29h	50h 52h	0005h 0000h	Flash Device Interface description (for complete description, please refer to CFI publication 100) 0000 = x8-only asynchronous interface 0001 = x16-only asynchronous interface 0002 = supports x8 and x16 via BYTE# with asynchronous interface 0003 = x 32-only asynchronous interface 0005 = supports x16 and x32 via WORD# with asynchronous interface
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte program = 2^N (00h = not supported)
2Ch	58h	0004h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	001Dh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 16. CFI Primary Vendor-Specific Extended Query

Addresses (x32 Mode)	Addresses (x16 Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	88h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	8Ah	0004h	Address Sensitive Unlock (DQ1, DQ0) 00 = Required, 01 = Not Required Silicon Revision Number (DQ5–DQ2 0000 = CS49 0001 = CS59 0010 = CS99 0011 = CS69 0100 = CS119

Table 16. CFI Primary Vendor-Specific Extended Query (Continued)

Addresses (x32 Mode)	Addresses (x16 Mode)	Data	Description
46h	8Ch	0002h	Erase Suspend (1 byte) 00 = Not Supported 01 = To Read Only 02 = To Read and Write
47h	8Eh	0001h	Sector Protect (1 byte) 00 = Not Supported, X = Number of sectors in per group
48h	90h	0000h	Temporary Sector Unprotect 00h = Not Supported, 01h = Supported
49h	92h	0006h	Sector Protect/Unprotect scheme (1 byte) 01 =29F040 mode, 02 = 29F016 mode 03 = 29F400 mode, 04 = 29LV800 mode 05 = 29BDS640 mode (Software Command Locking) 06 = BDD160 mode (New Sector Protect) 07 = 29LV800 + PDL128 (New Sector Protect) mode
4Ah	94h	001Fh	Simultaneous Operation (1 byte) 00h = Not Supported, X = Number of sectors in all banks except Bank 1
4Bh	96h	0001h	Burst Mode Type 00h = Not Supported, 01h = Supported
4Ch	98h	0000h	Page Mode Type 00h = Not Supported, 01h = 4 Word Page, 02h = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported (DQ7-DQ4: volt in hex, DQ3-DQ0: 100 mV in BCD)
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, (DQ7-DQ4: volt in hex, DQ3-DQ0: 100 mV in BCD)
4Fh	9Eh	0001h	Top/Bottom Boot Sector Flag (1 byte) 00h = Uniform device, no WP# control, 01h = 8 x 8 Kb sectors at top and bottom with WP# control 02h = Bottom boot device 03h = Top boot device 04h = Uniform, Bottom WP# Protect 05h = Uniform, Top WP# Protect If the number of erase block regions = 1, then ignore this field
50h	A0h	0001h	Program Suspend 00 = Not Supported 01 = Supported
51h	A2h	0000h	Write Buffer Size $2^{(N+1)}$ word(s)
57h	AEh	0002h	Bank Organization (1 byte) 00 = If data at 4Ah is zero XX = Number of banks
58h	B0h	000Fh	Bank 1 Region Information (1 byte) XX = Number of Sectors in Bank 1
59h	B2h	001Fh	Bank 2 Region Information (1 byte) XX = Number of Sectors in Bank 2
5Ah	B4h	0000h	Bank 3 Region Information (1 byte) XX = Number of Sectors in Bank 3
5Bh	B6h	0000h	Bank 4 Region Information (1 byte) XX = Number of Sectors in Bank 4

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Tables 18-21 define the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data in Non-burst Mode

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Sector Erase and Program Suspend Command for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device. section.

See also Asynchronous Read Operation (Non-Burst) in the Key to Switching Waveforms section for more information. See the Sector Erase and Program Resume Command sections for more information on this mode.

Reading Array Data in Burst Mode

The device is capable of very fast Burst mode read operations. The configuration register sets the read configuration, burst order, frequency configuration, and burst length.

Upon power on, the device defaults to the asynchronous mode. In this mode, CLK, and ADV# are ignored. The device operates like a conventional Flash device. Data is available t_{ACC}/t_{CE} nanoseconds after address becomes stable, CE# become asserted. The device enters the burst mode by enabling synchronous burst reads in the configuration register. The device exits burst mode by disabling synchronous burst reads in the configuration register. (See Command Definitions).

The RESET# command will not terminate the Burst mode. System reset (power on reset) will terminate the Burst mode.

The device has the regular control pins, i.e. Chip Enable (CE#), Write Enable (WE#), and Output Enable (OE#) to control normal read and write operations. Moreover, three additional control pins have been added to allow easy interface with minimal glue logic to a wide range of microprocessors / microcontrollers for high performance Burst read capability. These additional pins are Address Valid (ADV#) and Clock (CLK). CE#, OE#, and WE# are asynchronous (relative to CLK). The Burst mode read operation is a synchronous operation tied to the edge of the clock. The microprocessor / microcontroller supplies only the initial address, all subsequent addresses are automatically generated by the device with a timing defined by the Configuration Register definition. The Burst read cycle consists of an address phase and a corresponding data phase.

During the address phase, the Address Valid (ADV#) pin is asserted (taken Low) for one clock period. Together with the edge of the CLK, the starting burst address is loaded into the internal Burst Address Counter. The internal Burst Address Counter can be configured to either the Linear or Interleaved modes (See “Initial Access Delay Configuration”).

During the data phase, the first burst data is available after the initial access time delay defined in the Configuration Register. For subsequent burst data, every rising (or falling) edge of the CLK will trigger the output data with the burst output delay and sequence defined in the Configuration Register.

Tables 17–20 show all the commands executed by the device. The device automatically powers up in the read/reset state. It is not necessary to issue a read/reset command after power-up or hardware reset.

Read/Reset Command

After power-up or hardware reset, the Am29BDD160 automatically enter the read state. It is not necessary to issue the reset command after power-up or hardware reset. Standard microprocessor cycles retrieve array data, however, after power-up, only asynchronous accesses are permitted since the Configuration Register is at its reset state with burst accesses disabled.

The Reset command is executed when the user needs to exit any of the other user command sequences (such as autoselect, program, chip erase, etc.) to return to reading array data. There is no latency between executing the Reset command and reading array data.

The Reset command does not disable the SecSi sector if it is enabled. This function is only accomplished by issuing the SecSi Sector Exit command.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to V_{ID}. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The Am29BDD160 contains an Autoselect Command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register. The bank address (BA) is latched during the autoselect command sequence write operation to distinguish which bank the Autoselect command references. Reading the other bank after the Autoselect command is written results in reading array data from the other bank and the specified address. Following the command write, a read cycle from address (BA)XX00h retrieves the manufacturer code of (BA)XX01h. Three sequential read cycles at addresses (BA) XX01h, (BA) XX0Eh, and (BA) XX0Fh read the three-byte device ID (see Tables 19 and 20). All manufacturer and device codes exhibit odd parity with the MSB of the lower byte (DQ7) defined as the parity bit.

(The Autoselect Command requires the user to execute the Read/Reset command to return the device back to reading the array contents.)

Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Tables 18 and 20 shows the address and data requirements for the program command sequence.

During the Embedded Program algorithm, the system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. (See Write Operation Status for information on these status bits.) When the Embedded Program algorithm is complete, the device returns to reading array data and addresses are no longer latched. Note that an address change is required to begin read valid array data.

Except for Program Suspend, any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a “0” back to a “1”.** Attempting to do so may halt the operation and set DQ5 to “1,” or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.

Accelerated Program Command

The Accelerated Chip Program mode is designed to improve the Word or Double Word programming speed. Improving the programming speed is accomplished by using the ACC pin to supply both the wordline voltage and the bitline current instead of using the V_{PP} pump and drain pump, which is limited to 2.5 mA. Because the external ACC pin is capable of supplying significantly large amounts of current compared to the drain pump, all 32 bits are available for programming with a single programming pulse. This is an enormous improvement over the standard 5-bit programming. If the user is able to supply an external power supply and connect it to the ACC pin, significant time savings are realized.

In order to enter the Accelerated Program mode, the ACC pin must first be taken to V_{HH} (12 V ± 0.5 V) and followed by the one-cycle command with the program address and data to follow. The Accelerated Chip Program command is only executed when the device is in Unlock Bypass mode and during normal read/reset operating mode.

In this mode, the write protection function is bypassed unless the PPB Lock Bit = 1.

The Accelerated Program command is not permitted if the SecSi sector is enabled.

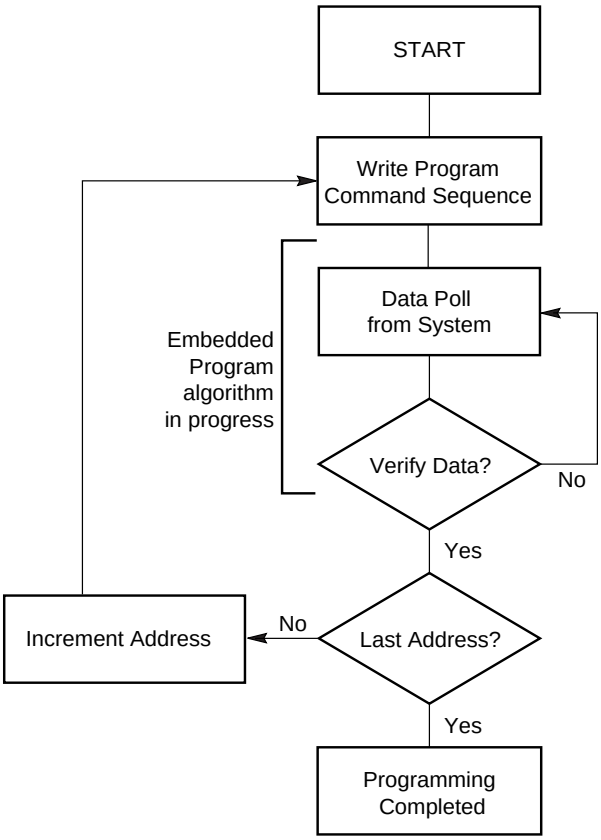
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in

the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Tables 18 and 20 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

Figure 9 illustrates the algorithm for the program operation. See the Erase/Program Operations table in AC Characteristics for parameters, and to Figure 26 for timing diagrams.



Note: *See Tables 18 and 20 for program command sequence.*

Figure 9. Program Operation

Unlock Bypass Entry Command

The Unlock Bypass command, once issued, is used to bypass the "unlock" sequence for program, chip erase, and CFI commands. This feature permits slow PROM programmers to significantly improve programming/erase throughput since the command sequence often requires microseconds to execute a single write operation. Therefore, once the Unlock Bypass command is issued, only the two-cycle program and erase bypass commands are required. The Unlock Bypass Command is ignored if the SecSi sector is enabled. To return back to normal operation, the Unlock Bypass Reset Command must be issued.

The following four sections describe the commands that may be executed within the unlock bypass mode.

Unlock Bypass Program Command

The Unlock Bypass Program command is a two-cycle command that consists of the actual program command (A0h) and the program address/data combination. This command does not require the two-cycle "unlock" sequence since the Unlock Bypass command was previously issued. As with the standard program command, multiple Unlock Bypass Program commands can be issued once the Unlock Bypass command is issued.

To return back to standard read operations, the Unlock Bypass Reset command must be issued.

The Unlock Bypass Program Command is ignored if the SecSi sector is enabled.

Unlock Bypass Chip Erase Command

The Unlock Bypass Chip Erase command is a 2-cycle command that consists of the erase setup command (80h) and the actual chip erase command (10h). This command does not require the two-cycle "unlock" sequence since the Unlock Bypass command was previously issued. Unlike the standard erase command, there is no Unlock Bypass Erase Suspend or Erase Resume commands.

To return back to standard read operations, the Unlock Bypass Reset command must be issued.

The Unlock Bypass Program Command is ignored if the SecSi sector is enabled.

Unlock Bypass CFI Command

The Unlock Bypass CFI command is available for PROM programmers and target systems to read the CFI codes while in Unlock Bypass mode. See Common Flash Memory Interface (CFI) for specific CFI codes.

To return back to standard read operations, the Unlock Bypass Reset command must be issued.

The Unlock Bypass Program Command is ignored if the SecSi sector is enabled.

Unlock Bypass Reset Command

The Unlock Bypass Reset command places the device in standard read/reset operating mode. Once executed, normal read operations and user command sequences are available for execution.

The Unlock Bypass Program Command is ignored if the SecSi sector is enabled.

Chip Erase Command

The Chip Erase command is used to erase the entire flash memory contents of the chip by issuing a single command. Chip erase is a six-bus cycle operation. There are two “unlock” write cycles, followed by writing the erase “set up” command. Two more “unlock” write cycles are followed by the chip erase command. Chip erase does not erase protected sectors.

The chip erase operation initiates the Embedded Erase algorithm, which automatically preprograms and verifies the entire memory to an all zero pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Note that a **hardware reset** immediately terminates the programming operation. The command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

The Embedded Erase algorithm erase begins on the rising edge of the last WE# or CE# pulse (whichever occurs first) in the command sequence. The status of the erase operation is determined three ways:

- Data# polling of the DQ7 pin (see DQ7: Data# Polling)
- Checking the status of the toggle bit DQ6 (see DQ6: Toggle Bit I)
- Checking the status of the RY/BY# pin (see RY/BY#: Ready/Busy#)

Once erasure has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data, and addresses are no longer latched. Note that an address change is required to begin read valid array data.

Figure 10 illustrates the Embedded Erase Algorithm. See the Erase/Program Operations tables in AC Characteristics for parameters, and to Figure 27 for timing diagrams.

Sector Erase Command

The Sector Erase command is used to erase individual sectors or the entire flash memory contents. Sector erase is a six-bus cycle operation. There are two “unlock” write cycles, followed by writing the erase “set up” command. Two more “unlock” write cycles are then followed by the erase command (30h). The sector address (any address location within the desired sector) is latched on the falling edge of WE# or CE# (whichever occurs last) while the command (30h) is latched on the rising edge of WE# or CE# (whichever occurs first).

Specifying multiple sectors for erase is accomplished by writing the six bus cycle operation, as described above, and then following it by additional writes of only the last cycle of the Sector Erase command to addresses or other sectors to be erased. The time between Sector Erase command writes must be less than 80 µs, otherwise the command is rejected. It is recommended that processor interrupts be disabled during this time to guarantee this critical timing condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last WE# (or CE#) will initiate the execution of the Sector Erase command(s). If another falling edge of the WE# (or CE#) occurs within the 80 µs time-out window, the timer is reset. Once the 80 µs window has timed out and erasure has begun, only the Erase Suspend command is recognized (see Sector Erase and Program Suspend Command and Sector Erase and Program Resume Command sections). If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity. Loading the sector erase registers may be done in any sequence and with any number of sectors.

Sector erase does not require the user to program the device prior to erase. The device automatically preprograms all memory locations, within sectors to be erased, prior to electrical erase. When erasing a sector or sectors, the remaining unselected sectors or the write protected sectors are unaffected. The system is not required to provide any controls or timings during sector erase operations. The Erase Suspend and Erase Resume commands may be written as often as required during a sector erase operation.

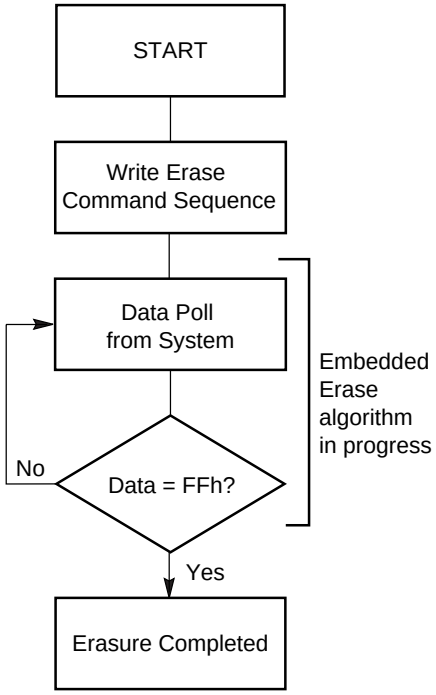
Automatic sector erase operations begin on the rising edge of the WE# or CE# pulse of the last sector erase command issued, and once the 80 µs time-out window has expired. The status of the sector erase operation is determined three ways:

- Data# polling of the DQ7 pin
- Checking the status of the toggle bit DQ6
- Checking the status of the RY/BY# pin

Further status of device activity during the sector erase operation is determined using toggle bit DQ2 (refer to DQ2: Toggle Bit II).

When the Embedded Erase algorithm is complete, the device returns to reading array data, and addresses are no longer latched. Note that an address change is required to begin read valid array data.

Figure 10 illustrates the Embedded™ Erase Algorithm, using a typical command sequence and bus operation. Refer to the Erase/Program Operations tables in the AC Characteristics section for parameters, and to Figure 27 for timing diagrams.



Notes:

1. *See Tables 18 and 20 for erase command sequence.*
2. *See DQ3: Sector Erase Timer for more information.*

Figure 10. Erase Operation

Sector Erase and Program Suspend Command

The Sector Erase and Program Suspend command allows the user to interrupt a Sector Erase or Program operation and perform data read or programs in a sector that is not being erased or to the sector where a programming operation was initiated. This command is applicable only during the Sector Erase and Programming operation, which includes the time-out period for Sector Erase. The Sector Erase and Program Suspend command is ignored if written during the execution of the Chip Erase operation or Embedded Program Algorithm (but will reset the chip if written improperly during the command sequences). Writing the Sector Erase and Program command during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation. Once in Erase Suspend, the device is available for reading (note that in the Erase Suspend mode, the Reset command is not required for read operations and is ignored) or program operations in sectors not being erased. Any other command written during the Erase Suspend mode is ignored, except for the Sector Erase and Program Resume command. Writing the Erase and Program Resume command resumes the sector erase operation. The bank address of the erase suspended bank is required when writing this command

If the Sector Erase and Program Suspend command is written during a programming operation, the device suspends programming operations and allows only read operations in sectors not selected for programming. Further nesting of either erase or programming operations is not permitted. Table 17 summarizes permissible operations during Erase and Program Suspend. (A busy sector is one that is selected for programming or erasure.):

Table 17. Allowed Operations During Erase/Program Suspend

Sector	Program Suspend	Erase Suspend
Busy Sector	Program Resume	Erase Resume
Non-busy sectors	Read Only	Read or Program

When the Sector Erase and Program Suspend command is written during a Sector Erase operation, the chip will take between 0.1 µs and 20 µs to actually suspend the operation and go into the erase suspended read mode (pseudo-read mode), at which time the user can read or program from a sector that is not erase suspended. Reading data in this mode is the same as reading from the standard read mode, except that the data must be read from sectors that have not been erase suspended.

Polling DQ6 on successive reads from a given address provides the system with the ability to determine if the device is in Erase or Program Suspend. Before the device enters Erase or Program Suspend, the DQ6 pin toggles between successive reads from the same address. After the device has entered Erase suspend, DQ6 stops toggling between successive reads to the same address. During the Sector Erase operation and also in Erase suspend mode, successively reading from the erase-suspended sector causes DQ2 to toggle. DQ2 does not toggle if reading from a non-busy (non-erasing) sector (stored data is read). No bits are toggled during program suspend mode. Software must keep track of the fact that the device is in a suspended mode.

After entering the erase-suspend-read mode, the system may read or program within any non-suspended sector:

- A read operation from the erase-suspended bank returns polling data during the first 8 µs after the erase suspend command is issued; read operations

thereafter return array data. Read operations from the other bank return array data with no latency.

- A program operation while in the erase suspend mode is the same as programming in the regular program mode, except that the data must be programmed to a sector that is not erase suspended. Write operation status is obtained in the same manner as a normal program operation.

Sector Erase and Program Resume Command

The Sector Erase and Program Resume command (30h) resumes a Sector Erase or Program operation that has been suspended. Any further writes of the Sector Erase and Program Resume command ignored. However, another Sector Erase and Program Suspend command can be written after the device has resumed sector erase operations. Note that until a suspended program or erase operation has resumed, the contents of that sector are unknown.

The Sector Erase and Program Resume Command is ignored if the SecSi sector is enabled.

Configuration Register Read Command

The Configuration Register Read command is used to verify the contents of the Configuration Register. Execution of this command is only allowed while in user mode and is not available during Unlock Bypass mode or during Security mode. The Configuration Register Read command is preceded by the standard two-cycle "unlock" sequence, followed by the Configuration Register Read command (C6h), and finally followed by performing a read operation to the bank address specified when the C6h command was written. Reading the other bank results in reading the flash memory contents. The contents of the Configuration Register are place on DQ15–DQ0. If WORD# is at V_{IH} (32-bit DQ Bus), the contents of DQ31–DQ16 are XXXXh and should be ignored. The user should execute the Read/Reset command to place the device back in standard user operation after executing the Configuration Register Read command.

The Configuration Register Read Command is fully operational if the SecSi sector is enabled.

Configuration Register Write Command

The Configuration Register Write command is used to modify the contents of the Configuration Register. Execution of this command is only allowed while in user mode and is not available during Unlock Bypass mode or during Security mode. The Configuration Register Write command is preceded by the standard two-cycle "unlock" sequence, followed by the Configuration Register Write command (D0h), and finally followed by writing the contents of the Configuration Register to any address. The contents of the Configuration Register are place on DQ15–DQ0. If WORD# is at V_{IH} (32-bit DQ Bus), the contents of DQ31–DQ16 are XXXXh and are ignored. Writing the Configuration Register while an Embedded Algorithm™ or Erase Suspend modes are executing results in the contents of the Configuration Register not being updated.

The Configuration Register Read Command is fully operational if the SecSi sector is enabled.

Common Flash Interface (CFI) Command

The Common Flash Interface (CFI) command provides device size, geometry, and capability information directly to the users system. Flash devices that support CFI, have a "Query Command" that returns information about the device to the system. The Query structure contents are read at the specific address locations following a single system write cycle where:

- A 98h query command code is written to 55h address location within the device's address space
- The device is initially in any valid read state, such as "Read Array" or "Read ID Data"

Other device statistics may exist within a long sequence of commands or data input; such sequences must first be completed or terminated before writing of the 98H Query command, otherwise invalid Query data structure output may result.

Note that for data bus bits greater than DQ7 (DQ31–DQ8), the valid Query access code has all zeroes ("0"s) in the upper DQ bus locations. Thus, the 16-bit Query command code is 0098h and the 32-bit Query command code is 00000098h.

To terminate the CFI operation, it is necessary to execute the Read/Reset command.

The CFI command is not permitted if the SecSi sector is enabled and Simultaneous Operation is disabled once the command is entered.

See Common Flash Memory Interface (CFI) for the specific CFI command codes.

SecSi Sector Entry Command

The SecSi Sector Entry command enables the SecSi (OTP) sector to overlay the 8 KB outermost sector in the small (25%) bank. The SecSi sector overlays 00000h–0003Fh for the top bootblock configuration and 7FFC0h–7FFFFh for the bottom bootblock confiuration. Address range 00040h–007FFh for the top bootblock and 7F800h–7FFBFh return invalid data when addressed with the SecSi sector enabled. The following commands are permitted after issuing the SecSi Sector Entry command:

1. Autoselect
2. Password Program (x16 and x32)
3. Password Verify
4. Password Unlock (x16 and x32)
5. Read/Reset
6. Program
7. Chip and Sector Erase
8. SecSi Sector Protection Bit Program
9. PPB Program
10. All PPB Erase
11. PPB Lock Bit Set
12. DYB Write
13. DYB/PPB/PPB Lock Bit Verify
14. Security Reset
15. Configuration Register Write
16. Configuration Register Read

The following commands are unavailable when the SecSi sector is enabled. Issuing the following commands while the SecSi sector is enabled results in the command being ignored.

1. Unlock Bypass
2. CFI
3. Accelerated Program
4. Program and Sector Erase Suspend
5. Program and Sector Erase Resume

The SecSi Sector Entry command is allowed when the device is in either program or erase suspend modes. If the SecSi sector is enabled, the program or erase suspend command is ignored. This prevents resuming either programming or erasure on the SecSi sector if the overlayed sector was undergoing programming or erasure. **The host system must ensure that the device resume any suspended program or erase operation after exiting the SecSi sector**.

Executing any of the PPB program/erase commands, or Password Unlock command results in the small bank (25% bank) returning the status of these operations while they are in progress, thus making the SecSi sector unavailable for reading. If the SecSi sector is enabled while the DYB command is issued, the DYB for the overlayed sector is NOT updated. Reading the DYB status using the PPB Lock Bit/DYBDYB verify command when the SecSi sector is enabled returns invalid data.

Password Program Command

The Password Program Command permits programming the password that is used as part of the hardware protection scheme. The actual password is 64-bits long. Depending upon the state of the WORD# pin, multiple Password Program Commands are required. For a x16 bit data bus, 4 Password Program commands are required to program the password. For a x32 bit data bus, 2 Password Program commands are required. The user must enter the unlock cycle, password program command (38h) and the program address/data for each portion of the password when programming. There are no provisions for entering the 2-cycle unlock cycle, the password program command, and all the password data. There is no special addressing order required for programming the password. Also, when the password is undergoing programming, Simultaneous Operation is disabled. Read operations to any memory location will return the programming status. Once programming is complete, the user must issue a Read/Reset command to return the device to normal operation. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent verification. The Password Program Command is only capable of programming “0”s. Programming a “1” after a cell is programmed as a “0” results in a time-out by the Embedded Program Algorithm™ with the cell remaining as a “0”. The password is all F’s when shipped from the factory. All 64-bit password combinations are valid as a password.

Password Programming is permitted if the SecSi sector is enabled.

Password Verify Command

The Password Verify Command is used to verify the Password. The Password is verifiable only when the Password Mode Locking Bit is not programmed. If the Password Mode Locking Bit is programmed and the user attempts to verify the Password, the device will always drive all F’s onto the DQ data bus.

The Password Verify command is permitted if the SecSi sector is enabled. Also, the device will not operate in Simultaneous Operation when the Password Verify command is executed. Only the password is returned regardless of the bank address. The lower two address bits (A0:A-1) are valid during the Password

Verify. Writing the Read/Reset command returns the device back to normal operation.

Password Protection Mode Locking Bit Program Command

The Password Protection Mode Locking Bit Program Command programs the Password Protection Mode Locking Bit, which prevents further verifies or updates to the Password. Once programmed, the Password Protection Mode Locking Bit cannot be erased! If the Password Protection Mode Locking Bit is verified as program without margin, the Password Protection Mode Locking Bit Program command can be executed to improve the program margin. Once the Password Protection Mode Locking Bit is programmed, the Persistent Sector Protection Locking Bit program circuitry is disabled, thereby forcing the device to remain in the Password Protection mode. Exiting the Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

The Password Protection Mode Locking Bit Program command is permitted if the SecSi sector is enabled.

Persistent Sector Protection Mode Locking Bit Program Command

The Persistent Sector Protection Mode Locking Bit Program Command programs the Persistent Sector Protection Mode Locking Bit, which prevents the Password Mode Locking Bit from ever being programmed. If the Persistent Sector Protection Mode Locking Bit is verified as programmed without margin, the Persistent Sector Protection Mode Locking Bit Program Command should be reissued to improve program margin. By disabling the program circuitry of the Password Mode Locking Bit, the device is forced to remain in the Persistent Sector Protection mode of operation, once this bit is set. Exiting the Persistent Protection Mode Locking Bit Program command is accomplished by writing the Read/Reset command.

The Persistent Sector Protection Mode Locking Bit Program command is permitted if the SecSi sector is enabled.

SecSi Sector Protection Bit Program Command

The SecSi Sector Protection Bit Program Command programs the SecSi Sector Protection Bit, which prevents the SecSi sector memory from being cleared. If the SecSi Sector Protection Bit is verified as programmed without margin, the SecSi Sector Protection Bit Program Command should be reissued to improve program margin. Exiting the V_{CC}-level SecSi Sector Protection Bit Program Command is accomplished by writing the Read/Reset command.

The SecSi Sector Protection Bit Program command is permitted if the SecSi sector is enabled.

PPB Lock Bit Set Command

The PPB Lock Bit Set command is used to set the PPB Lock bit if it is cleared either at reset or if the Password Unlock command was successfully executed. There is no PPB Lock Bit Clear command. Once the PPB Lock Bit is set, it cannot be cleared unless the device is taken through a power-on clear or the Password Unlock command is executed. Upon setting the PPB Lock Bit, the PPBs are latched into the DYBs. If the Password Mode Locking Bit is set, the PPB Lock Bit status is reflected as set, even after a power-on reset cycle. Exiting the PPB Lock Bit Set command is accomplished by writing the Read/Reset command.

The PPB Lock Bit Set command is permitted if the SecSi sector is enabled.

DYB Write Command

The DYB Write command is used to set or clear a DYB for a given sector. The high order address bits (A18–A11) are issued at the same time as the code 01h or 00h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are cleared at power-up or hardware reset.Exiting the DYB Write command is accomplished by writing the Read/Reset command.

The DYB Write command is permitted if the SecSi sector is enabled.

Password Unlock Command

The Password Unlock command is used to clear the PPB Lock Bit so that the PPBs can be unlocked for modification, thereby allowing the PPBs to become accessible for modification. The exact password must be entered in order for the unlocking function to occur. This command cannot be issued any faster than 2 µs at a time to prevent a hacker from running through the all 64-bit combinations in an attempt to correctly match a password. If the command is issued before the 2 µs execution window for each portion of the unlock, the command will be ignored.

The Password Unlock function is accomplished by writing Password Unlock command and data to the device to perform the clearing of the PPB Lock Bit. The password is 64 bits long, so the user must write the Password Unlock command 2 times for a x32 bit data bus and 4 times for a x16 data bus. A0 is used to determine whether the 32 bit data quantity is used to match the upper 32 bits or lower 32 bits. A0 and A_{-1} is used for matching when the x16 bit data bus is se-

lected (WORD# = 0). Writing the Password Unlock command is address order specific. In other words, for the x32 data bus configuration, the lower 32 bits of the password are written first and then the upper 32 bits of the password are written. For the x16 data bus configuration, the lower address A0:A_{-1}= 00, the next Password Unlock command is to A0:A_{-1}= 01, then to A0:A_{-1}= 10, and finally to A0:A_{-1}= 11. Writing out of sequence results in the Password Unlock not returning a match with the password and the PPB Lock Bit remains set.

Once the Password Unlock command is entered, the RDY/BSY# pin goes LOW indicating that the device is busy. Also, reading the small bank (25% bank) results in the DQ6 pin toggling, indicating that the Password Unlock function is in progress. Reading the large bank (75% bank) returns actual array data. Approximately 1uSec is required for each portion of the unlock. Once the first portion of the password unlock completes (RDY/BSY# is not driven and DQ6 does not toggle when read), the Password Unlock command is issued again, only this time with the next part of the password. If WORD# = 1, the second Password Unlock command is the final command before the PPB Lock Bit is cleared (assuming a valid password). If WORD# = 0, this is the fourth Password Unlock command. In x16 mode, four Password Unlock commands are required to successfully clear the PPB Lock Bit. As with the first Password Unlock command, the RY/BY# signal goes LOW and reading the device results in the DQ6 pin toggling on successive read operations until complete. It is the responsibility of the microprocessor to keep track of the number of Password Unlock commands (2 for x32 bus and 4 for x16 bus), the order, and when to read the PPB Lock bit to confirm successful password unlock

The Password Unlock command is permitted if the SecSi sector is enabled.

PPB Program Command

The PPB Program command is used to program, or set, a given PPB. Each PPB is individually programmed (but is bulk erased with the other PPBs). The specific sector address (A18–A11) are written at the same time as the program command 60h with A6 = 0. If the PPB Lock Bit is set and the corresponding PPB is set for the sector, the PPB Program command will not execute and the command will time-out without programming the PPB.

The host system must determine whether a PPB has been fully programmed by noting the status of DQ0 in the sixth cycle of the PPB Program command. If DQ0 = 0, the entire six-cycle PPB Program command sequence must be reissued until DQ0 = 1.

All PPB Erase Command

The All PPB Erase command is used to erase all PPBs in bulk. There is no means for individually erasing a specific PPB. Unlike the PPB program, no specific sector address is required. However, when the PPB erase command is written (60h) and A6 = 1, all Sector PPBs are erased in parallel. If the PPB Lock Bit is set the ALL PPB Erase command will not execute and the command will time-out without erasing the PPBs. The host system must determine whether all PPB has been fully erased by noting the status of DQ0 in the sixth cycle of the All PPB Erase command. If DQ0 = 1, the entire six-cycle All PPB Erase command sequence must be reissued until DQ0 = 1.

It is the responsibility of the user to preprogram all PPBs prior to issuing the All PPB Erase command. If the user attempts to erase a cleared PPB, over-erasure may occur making it difficult to program the PPB at a later time. Also note that the total number of PPB program/erase cycles is limited to 100 cycles. Cycling the PPBs beyond 100 cycles is not guaranteed.

The All PPB Erase command is permitted if the SecSi sector is enabled.

DYB Write

The DYB Write command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

The DYB Write command is permitted if the SecSi sector is enabled.

PPB Lock Bit Set

The PPB Lock Bit set command is used for setting the DYB, which is a volatile bit that is cleared at reset. There is one DYB per sector. If the PPB is set, the sector is protected regardless of the value of the DYB. If the PPB is cleared, setting the DYB to a 1 protects the sector from programs or erases. Since this is a volatile bit, removing power or resetting the device will clear the DYBs. The bank address is latched when the command is written.

The PPB Lock command is permitted if the SecSi sector is enabled.

DYB Status

The programming of the DYB for a given sector can be verified by writing a DYB status verify command to the device.

PPB Status

The programming of the PPB for a given sector can be verified by writing a PPB status verify command to the device.

PPB Lock Bit Status

The programming of the PPB Lock Bit for a given sector can be verified by writing a PPB Lock Bit status verify command to the device.

Non-volatile Protection Bit Program And Erase Flow

The device uses a standard command sequence for programming or erasing the SecSi Sector Protection, Password Locking, Persistent Sector Protection Mode Locking, or Persistent Protection Bits. Unlike devices that have the Single High Voltage Sector Unprotect/Protect feature, the Am29BDD160 has the standard two-cycle unlock followed by 60h, which places the device into non-volatile bit program or erase mode. Once the mode is entered, the specific non-volatile bit status is read on DQ0. Figure 9 shows a typical flow for programming the non-volatile bit and Figure 10 shows a typical flow for erasing the non-volatile bits. The SecSi Sector Protection, Password Locking, Persistent Sector Protection Mode Locking bits are **not erasable** after they are programmed. However, the PPBs are both erasable and programmable (depending upon device security).

Unlike Single High Voltage Sector Protect/Unprotect, the A6 pin no longer functions as the program/erase selector nor the program/erase margin enable. Instead, this function is accomplished by issuing the specific command for either program (68h) or erase (60h).

In asynchronous mode, the DQ6 toggle bit indicates whether the program or erase sequence is active. (In synchronous mode, ADV# indicates the status.) If the DQ6 toggle bit toggles with either OE# or CE#, the non-volatile bit program or erase operation is in progress. When DQ6 stops toggling, the value of the non-volatile bit is available on DQ0.

Table 18. Memory Array Command Definitions (x32 Mode)

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)		1	RA	RD										
Reset (6)		1	XXX	F0										
Autoselect (7)	Manufacturer ID	4	555	AA	2AA	55	555	90	(BA)X00	01				
	Device ID (11)	6	555	AA	2AA	55	555	90	(BA)X01	7E	(BA)X0E	08	(BA)X0F	00/01
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (12)		1	BA	B0										
Program/Erase Resume (13)		1	BA	30										
CFI Query (14, 15)		1	55	98										
Accelerated Program (16)		2	XX	A0	PA	PD								
Configuration Register Verify (15)		3	555	AA	2AA	55	(BA)555	C6	(BA)XX	RD				
Configuration Register Write (17)		4	555	AA	2AA	55	555	D0	XX	WD				
Unlock Bypass Entry (18)		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (18)		2	XX	A0	PA	PD								
Unlock Bypass Erase (18)		2	XX	80	XX	10								
Unlock Bypass CFI (14, 18)		1	XX	98										
Unlock Bypass Reset (18)		2	XX	90	XX	00								

Legend:

BA = Address of the bank that is being switched to autoselect mode, is in bypass mode, or is being erased. Determined by A18 and A17, see Tables 11 and 12 for more detail.

PA = Program Address (A18:A0). Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data (DQ31:DQ0) written to location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

RA = Read Address (A18:A0).

RD = Read Data (DQ31:DQ0) from location RA.

SA = Sector Address (A18:A11) for verifying (in autoselect mode), erasing, or applying security commands.

WD = Write Data. See "Configuration Register" definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock cycles, (lower address bits are 555 or 2AAh as shown in table) address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when bank is reading array data.*
6. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).*
7. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacturer ID or device ID information. See the Autoselect Command section for more information.*
8. *This command cannot be executed until The Unlock Bypass command must be executed before writing this command sequence. The Unlock Bypass Reset command must be executed to return to normal operation.*
9. *This command is ignored during any embedded program, erase or suspended operation.*
10. *Valid read operations include asynchronous and burst read mode operations.*
11. *The device ID must be read across the fourth, fifth, and sixth cycles. 00h in the sixth cycle indicates top boot block, 01h indicates bottom boot block.*
12. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Program/Erase Suspend mode. The Program/Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
13. *The Program/Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
14. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
15. *Asynchronous read operations.*
16. *ACC must be at V_{ID} during the entire operation of this command.*
17. *Command is ignored during any Embedded Program, Embedded Erase, or Suspend operation.*
18. *The Unlock Bypass Entry command is required prior to any Unlock Bypass operation. The Unlock Bypass Reset command is required to return to the read mode.*

Table 19. Sector Protection Command Definitions (x32 Mode)

Command (Notes)	Cycles	Bus Cycles (Notes 1-4)											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0										
SecSi Sector Entry	3	555	AA	2AA	55	555	88						
SecSi Sector Exit	4	555	AA	2AA	55	555	90	XX	00				
SecSi Protection Bit Program (5, 6)	6	555	AA	2AA	55	555	60	OW	68	OW	48	OW	RD(0)
SecSi Protection Bit Status	6	555	AA	2AA	55	555	60	OW	RD(0)				
Password Program (5, 7, 8)	4	555	AA	2AA	55	555	38	PWA[0-1]	PWD[0-1]				
Password Verify	4	555	AA	2AA	55	555	C8	PWA[0-1]	PWD[0-1]				
Password Unlock (7, 8)	5	555	AA	2AA	55	555	28	PWA[0-1]	PWD[0-1]				
PPB Program (5, 6)	6	555	AA	2AA	55	555	60	(SA)WP	68	(SA)WP	48	(SA)WP	RD(0)
All PPB Erase (5, 9, 10)	6	555	AA	2AA	55	555	60	WP	60	(SA)WP	40	(SA)WP	RD(0)
PPB Status (11, 12)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
PPB Lock Bit Set	3	555	AA	2AA	55	555	78						
PPB Lock Bit Status	4	555	AA	2AA	55	(BA) 555	58	SA	RD(1)				
DYB Write (7)	4	555	AA	2AA	55	555	48	SA	X1				
DYB Erase (7)	4	555	AA	2AA	55	555	48	SA	X0				
DYB Status (12)	4	555	AA	2AA	55	(BA) 555	58	SA	RD(0)				
PPMLB Program (5,6)	6	555	AA	2AA	55	555	60	PL	68	PL	48	PL	RD(0)
PPMLB Status (5)	6	555	AA	2AA	55	555	60	PL	RD(0)				
SPMLB Program (5, 6)	6	555	AA	2AA	55	555	60	SL	68	SL	48	SL	RD(0)
SPMLB Status (5)	6	555	AA	2AA	55	555	60	SL	RD(0)				

DYB = Dynamic Protection Bit
OW = Address (A5–A0) is (001X10).
PPB = Persistent Protection Bit
PWA = Password Address. A0 selects between the low and high 32-bit portions of the 64-bit Password
PWD = Password Data. Must be written over two cycles.
PL = Password Protection Mode Lock Address (A5–A0) is (001X10)
RD(0) = Read Data DQ0 protection indicator bit. If protected, DQ0= 1, if unprotected, DQ0 = 0.
RD(1) = Read Data DQ1 protection indicator bit. If protected, DQ1 = 1, if unprotected, DQ1 = 0.
SA = Sector Address where security command applies. Address bits A18:A11 uniquely select any sector.
SL = Persistent Protection Mode Lock Address (A5–A0) is (010X10)
WP = PPB Address (A5–A0) is (111X10)
X = Don't care
PPMLB = Password Protection Mode Locking Bit
SPMLB = Persistent Protection Mode Locking Bit

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock cycles, (lower address bits are 555 or 2AAh as shown in table) address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *The reset command returns the device to reading the array.*
6. *The fourth cycle programs the addressed locking bit. The fifth and sixth cycles are used to validate whether the bit has been fully programmed. If DQ0 (in the sixth cycle) reads 0, the program command must be issued and verified again.*
7. *Data is latched on the rising edge of WE#.*
8. *The entire four bus-cycle sequence must be entered for each portion of the password.*
9. *The fourth cycle erases all PPBs. The fifth and sixth cycles are used to validate whether the bits have been fully erased. If DQ0 (in the sixth cycle) reads 1, the erase command must be issued and verified again.*
10. *Before issuing the erase command, all PPBs should be programmed in order to prevent over-erasure of PPBs.*
11. *In the fourth cycle, 00h indicates PPB set; 01h indicates PPB not set.*
12. *The status of additional PPBs and DYBs may be read (following the fourth cycle) without reissuing the entire command sequence.*

Table 20. Memory Array Command Definitions (x16 Mode)

Command (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (5)		1	RA	RD										
Reset (6)		1	XXX	F0										
Autoselect (7)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	(BA)X00	01				
	Device ID (11)	6	AAA	AA	555	55	AAA	90	(BA)X02	7E	(BA)X1C	08	(BA)X1E	00/01
Program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	555	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Program/Erase Suspend (12)		1	BA	B0										
Program/Erase Resume (13)		1	BA	30										
CFI Query (14, 15)		1	AA	98										
Accelerated Program (16)		2	XX	A0	PA	PD								
Configuration Register Verify (15)		3	AAA	AA	555	55	(BA)555	C6	(BA)XX	RD				
Configuration Register Write (17)		4	AAA	AA	555	55	AAA	D0	XX	WD				
Unlock Bypass Entry (18)		3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (18)		2	XX	A0	PA	PD								
Unlock Bypass Erase (18)		2	XX	80	XX	10								
Unlock Bypass CFI (14, 18)		1	XX	98										
Unlock Bypass Reset (18)		2	XX	90	XX	00								

Legend:

BA = Address of the bank that is being switched to autoselect mode, is in bypass mode, or is being erased. Determined by A18 and A17, see Tables 11 and 12 for more detail.

PA = Program Address (A18:A-1). Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data (DQ15:DQ0) written to location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

RA = Read Address (A18:A-1).

RD = Read Data (DQ15:DQ0) from location RA.

SA = Sector Address (A18:A11) for verifying (in autoselect mode), erasing, or applying security commands.

WD = Write Data. See "Configuration Register" definition for specific write data. Data latched on rising edge of WE#.

X = Don't care

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock cycles, (lower address bits are AAA or 555h as shown in table) address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when bank is reading array data.*
6. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).*
7. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacturer ID or device ID information. See the Autoselect Command section for more information.*
8. *This command cannot be executed until The Unlock Bypass command must be executed before writing this command sequence. The Unlock Bypass Reset command must be executed to return to normal operation.*
9. *This command is ignored during any embedded program, erase or suspended operation.*
10. *Valid read operations include asynchronous and burst read mode operations.*
11. *The device ID must be read across the fourth, fifth, and sixth cycles. 00h in the sixth cycle indicates top boot block, 01h indicates bottom boot block.*
12. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Program/Erase Suspend mode. The Program/Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
13. *The Program/Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
14. *Command is valid when device is ready to read array data or when device is in autoselect mode.*
15. *Asynchronous read operations.*
16. *ACC must be at V_{ID} during the entire operation of this command.*
17. *Command is ignored during any Embedded Program, Embedded Erase, or Suspend operation.*
18. *The Unlock Bypass Entry command is required prior to any Unlock Bypass operation. The Unlock Bypass Reset command is required to return to the read mode.*

Table 21. Sector Protection Command Definitions (x16 Mode)

Command (Notes)	Cycles	Bus Cycles (Notes 1-4)											
		First		Second		Third		Fourth		Fifth		Sixth	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	XXX	F0										
SecSi Sector Entry	3	AAA	AA	555	55	AAA	88						
SecSi Sector Exit	4	AAA	AA	555	55	AAA	90	XX	00				
SecSi Protection Bit Program (5, 6)	6	AAA	AA	555	55	AAA	60	OW	68	OW	48	OW	RD(0)
SecSi Protection Bit Status	6	AAA	AA	555	55	AAA	60	OW	RD(0)				
Password Program (5, 7, 8)	5	AAA	AA	555	55	AAA	38	PWA[0–3]	PWD[0–3]				
Password Verify	4	AAA	AA	555	55	AAA	C8	PWA[0–3]	PWD[0–3]				
Password Unlock (7, 8)	5	AAA	AA	555	55	AAA	28	PWA[0–3]	PWD[0–3]				
PPB Program (5, 6)	6	AAA	AA	555	55	AAA	60	(SA)WP	68	(SA)WP	48	(SA)WP	RD(0)
All PPB Erase (5, 9, 10)	6	AAA	AA	555	55	AAA	60	WP	60	(SA)WP	40	(SA)WP	RD(0)
PPB Status (11, 12)	4	AAA	AA	555	55	AAA	90	(SA)X04	00/01				
PPB Lock Bit Set	3	AAA	AA	555	55	AAA	78						
PPB Lock Bit Status	4	AAA	AA	555	55	(BA) AAA	58	SA	RD(1)				
DYB Write (7)	4	AAA	AA	555	55	AAA	48	SA	X1				
DYB Erase (7)	4	AAA	AA	555	55	AAA	48	SA	X0				
DYB Status (12)	4	AAA	AA	555	55	(BA) AAA	58	SA	RD(0)				
PPMLB Program (5, 6)	6	AAA	AA	555	55	AAA	60	PL	68	PL	48	PL	RD(0)
PPMLB Status (5)	6	AAA	AA	555	55	AAA	60	PL	RD(0)				
SPMLB Program (5, 6)	6	AAA	AA	555	55	AAA	60	SL	68	SL	48	SL	RD(0)
SPMLB Status (5)	6	AAA	AA	555	55	AAA	60	SL	RD(0)				

Legend:

DYB = Dynamic Protection Bit

OW = Address (A5–A0) is (011X10).

PD3:0 = Four 32-bit quantities representing the password.

PPB = Persistent Protection Bit

PWA = Password Address. A1:A0 selects between the low and high 16-bit portions of the 64-bit Password

PWD = Password Data.Must be written over four cycles.

PL = Password Protection Mode Lock Address (A5-A0) is (001X10)

RD(0) = Read Data DQ0 protection indicator bit. If protected, DQ0 = 1, if unprotected, DQ0 = 0.

RD(1) = Read Data DQ1 protection indicator bit. If protected, DQ1 = 1, if unprotected, DQ1 = 0.

SA = Sector Address where security command applies. Address bits A18:A11 uniquely select any sector.

SL = Persistent Protection Mode Lock Address (A5–A0) is (010X10)

WP = PPB Address (A5–A0) is (111X10)

X = Don't care

PPMLB = Password Protection Mode Locking Bit

SPMLB = Persistent Protection Mode Locking Bit

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells in table denote read cycles. All other cycles are write operations.*
4. *During unlock cycles, (lower address bits are AAA or 555h as shown in table) address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *The reset command returns the device to reading the array.*
6. *The fourth cycle programs the addressed locking bit. The fifth and sixth cycles are used to validate whether the bit has been fully programmed. If DQ0 (in the sixth cycle) reads 0, the program command must be issued and verified again.*
7. *Data is latched on the rising edge of WE#.*
8. *The entire four bus-cycle sequence must be entered for each portion of the password. PWA[0–3] represent the four addresses over which the password is stored. PWD[0–3] represent the four word data that comprise the password.*
9. *The fourth cycle erases all PPBs. The fifth and sixth cycles are used to validate whether the bits have been fully erased. If DQ0 (in the sixth cycle) reads 1, the erase command must be issued and verified again.*
10. *Before issuing the erase command, all PPBs should be programmed in order to prevent over-erasure of PPBs.*
11. *In the fourth cycle, 00h indicates PPB set; 01h indicates PPB not set.*
12. *The status of additional PPBs and DYBs may be read (following the fourth cycle) without reissuing the entire command sequence.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: DQ2, DQ3, DQ5, DQ6, DQ7, and RY/BY#. Table 22 and the following subsections describe the functions of these bits. DQ7, RY/BY#, and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

DQ7: Data# Polling

The Am29BDD160 features a Data# polling flag as a method to indicate to the host system whether the embedded algorithms are in progress or are complete. During the Embedded Program Algorithm an attempt to read the bank in which programming was initiated will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true last data written to DQ7. Note that DATA# polling returns invalid data for the address being programmed or erased.

For example, the data read for an address programmed as 0000 0000 1000 0000b will return XXXX XXXX 0XXX XXXXb during an Embedded Program operation. Once the Embedded Program Algorithm is complete, the true data is read back on DQ7. Note that at the instant when DQ7 switches to true data, the other bits may not yet be true. However, they will all be true data on the next read from the device. Please note that Data# polling may give misleading status when an attempt is made to write to a protected sector.

For chip erase, the Data# polling flag is valid after the rising edge of the sixth WE# pulse in the six write pulse sequence. For sector erase, the Data# polling is valid after the last rising edge of the sector erase WE# pulse. Data# polling must be performed at sector addresses within any of the sectors being erased and not a sector that is a protected sector. Otherwise, the status may not be valid. DQ7 = 0 during an Embedded Erase Algorithm (chip erase or sector erase operation) but will return a “1” after the operation completes because it will have dropped back into read mode.

In asynchronous mode, just prior to the completion of the Embedded Algorithm operations, DQ7 may change asynchronously while OE# is asserted low. (In synchronous mode, ADV# exhibits this behavior.) The status information may be invalid during the instance of transition from status information to array (memory) data. An extra validity check is therefore specified in the data polling algorithm. The valid array data on DQ31–DQ0 (DQ15–DQ0 when WORD# = 0) is available for reading on the next successive read attempt.

The Data# polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, Erase Suspend, Erase Suspend-Program mode, or sector erase time-out.

If the user attempts to write to a protected sector, Data# polling will be activated for about 1 µs: the device will then return to read mode, with the data from the protected sector unchanged. If the user attempts to erase a protected sector, Toggle Bit (DQ6) will be activated for about 150 µs; the device will then return to read mode, without having erased the protected sector.

Table 22 shows the outputs for Data# Polling on DQ7. Figure 11 shows the Data# Polling algorithm.

RY/BY#: Ready/Busy#

The device provides a RY/BY# open drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or have been completed. If the output is low, the device is busy with either a program, erase, or reset operation. If the output is floating, the device is ready to accept any read/write or erase operation. When the RY/BY# pin is low, the device will not accept any additional program or erase commands with the exception of the Erase suspend command. If the device has entered Erase Suspend mode, the RY/BY# output will be floating. For programming, the RY/BY# is valid (RY/BY# = 0) after the rising edge of the fourth WE# pulse in the four write pulse sequence. For chip erase, the RY/BY# is valid after the rising edge of the sixth WE# pulse in the six write pulse sequence. For sector erase, the RY/BY# is also valid after the rising edge of the sixth WE# pulse.

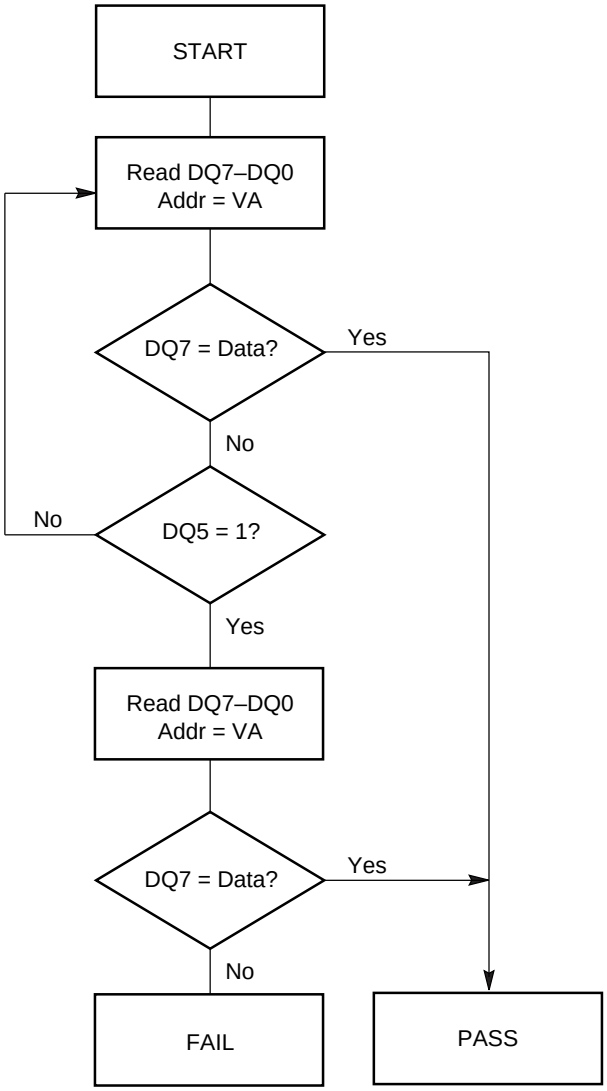
If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “floating”), the reset operation is completed in a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Since the RY/BY# pin is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}. An external pull-up resistor is required to take RY/BY# to a V_{IH} level since the output is an open drain.

Table 22 shows the outputs for RY/BY#. Figures 20, 24, 26 and 27 shows RY/BY# for read, reset, program, and erase operations, respectively.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete,



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is an address within any sector selected for erasure. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 11. Data# Polling Algorithm

or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. When the operation is complete, DQ6 stops toggling. For asynchronous mode, either OE# or CE# can be used to control the read cycles. For synchronous mode, ADV# is used.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 22 shows the outputs for Toggle Bit I on DQ6. Figure 12 shows the toggle bit algorithm in flowchart form, and the section Reading Toggle Bits DQ6/DQ2 explains the algorithm. Figure 30 in the AC Characteristics section shows the toggle bit timing diagrams. Figure 31 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (For asynchronous mode, either OE# or CE# can be used to control the read cycles. For synchronous mode, ADV# is used.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 22 to compare outputs for DQ2 and DQ6.

Figure 12 shows the toggle bit algorithm in flowchart form, and the section Reading Toggle Bits DQ6/DQ2 explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 30 shows the toggle bit timing diagram. Figure 31 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 12 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

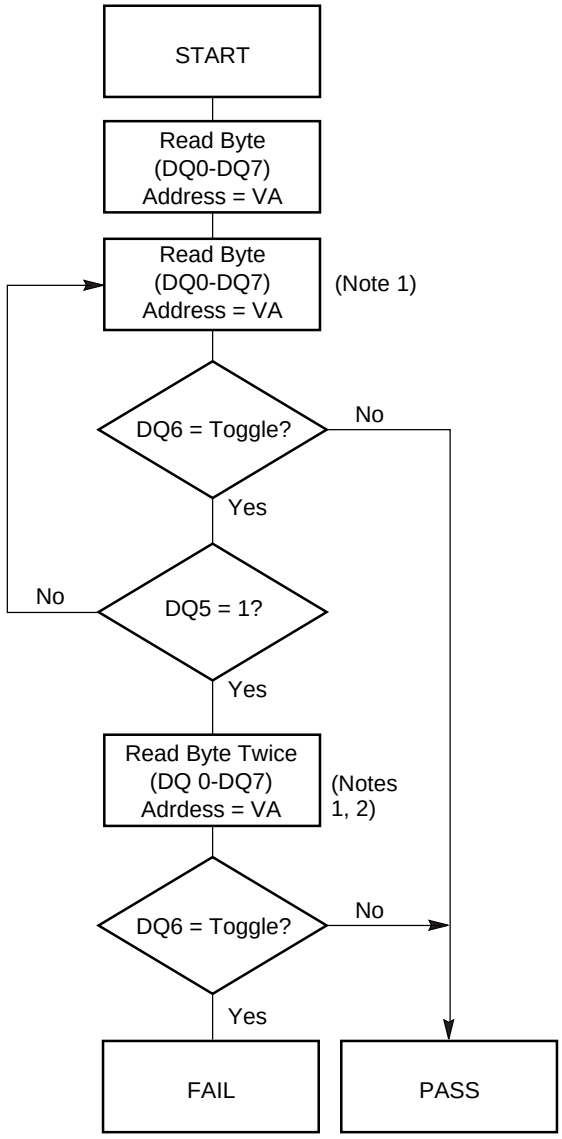
However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 12).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed.

The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.”



Notes:

1. *Read toggle bit twice to determine whether or not it is toggling. See text.*
2. *Recheck toggle bit because it may stop toggling as DQ5 changes to “1”. See text.*

Figure 12. Toggle Bit Algorithm

Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also

applies after each additional sector erase command. When the time-out is complete, DQ3 switches from “0” to “1.” The system may ignore DQ3 if the system can guarantee that the time between additional sector erase commands will always be less than 50 µs. See also the Sector Erase Command section.

After the sector erase command sequence is written, the system should read the status on DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure the device has accepted the command sequence, and then read DQ3. If DQ3 is “1”, the internally controlled erase cycle has begun; all further commands (other than Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0”, the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 22 shows the outputs for DQ3.

Table 22. Write Operation Status

Operation		DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	RY/BY#
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program	DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to ‘1’ when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. See DQ5: Exceeded Timing Limits for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +145°C

Voltage with Respect to Ground (Note 1)
. . . . . –0.5 V to +V_{IO} + 0.5 V

V_{CC} (Note 1) . . . . . –0.5 V to + 2.75 V

A9, OE#, and RESET# (Note 2) . . –0.5 V to +13.0 V

Address, Data, Control Signals
(with the exception of CLK) . . . . . 1.65 V to 3.6 V

All other pins (Note 1). . . . . –0.5 V to +5.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input at I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 13. Maximum DC voltage on output and I/O pins is 3.6 V. During voltage transitions output pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 14.*
2. *Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 13. Maximum DC input voltage on pin A9 and OE# is +13.0 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

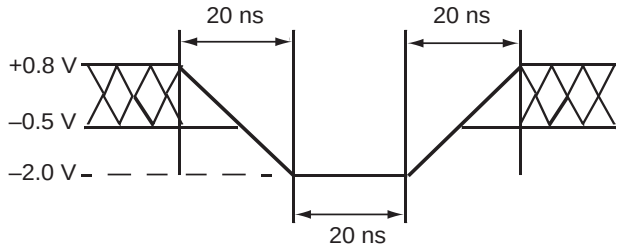


Figure 13. Maximum Negative Overshoot Waveform

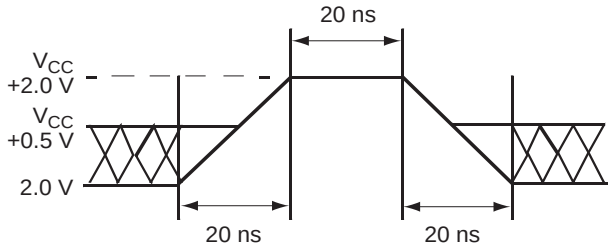


Figure 14. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Extended (E) Devices

Ambient Temperature (T_A) . . . . . –40°C to +125°C

V_{CC} Supply Voltages

V_{CC} for regulated voltage range . . . . . 2.3 V to 2.75 V

V_{IO} Supply Voltages

V_{IO} . . . . . 1.65 V to 2.75 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

CMOS Compatible

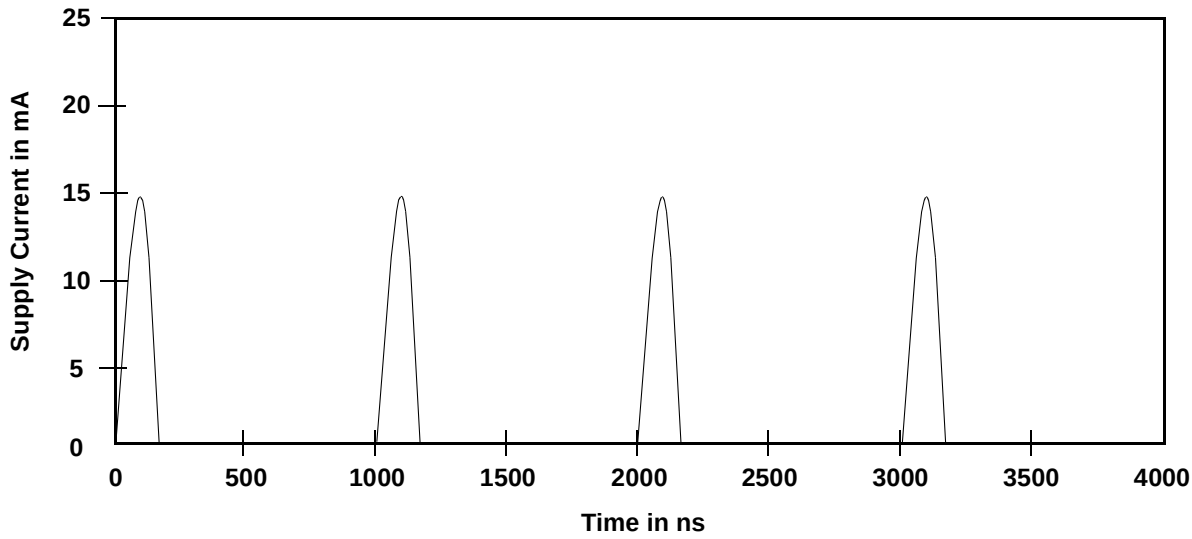
Parameter	Description	Test Conditions			Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{IO}, $V_{IO} = V_{IO\ max}$					±1.0	µA
I_{LIWP}	Input Load Current, WP#	$V_{IN} = V_{SS}$ to V_{IO}, $V_{IO} = V_{IO\ max}$					–25	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$					±1.0	µA
I_{CCB}	V_{CC} Active Burst Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IL}	56 MHz	8 Double-Word		70	90	mA
			66 MHz	Continuous Burst				
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 1)	CE# = V_{IL}, OE# = V_{IL}		1 MHz			4	mA
I_{CC3}	V_{CC} Active Program Current (Notes 2, 4)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}				40	50	mA
I_{CC4}	V_{CC} Active Erase Current (Notes 2, 4)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}				20	50	mA
I_{CC5}	V_{CC} Standby Current (CMOS)	V_{CC}= $V_{CC\ max}$, CE# = V_{CC} ± 0.3 V					9	µA
I_{CC6}	V_{CC} Active Current (Read While Write)	CE# = V_{IL}, OE# = V_{IL}		16-bit		30		
				32-bit				
I_{CC7}	V_{CC} Reset Current	RESET# = V_{IL}					9	µA
I_{CC8}	Automatic Sleep Mode	$V_{IH} = V_{CC}$ ± 0.3 V, $V_{IL} = V_{SS}$ ± 0.3 V					9	µA
I_{PP}	Accelerated Program Current	CE# = V_{IL}, OE# = V_{IH}, V_{PP} = 12.0 ± 0.5 V						
V_{IL}	Input Low Voltage				–0.5		0.3 x V_{IO}	V
V_{IH}	Input High Voltage				0.7 x V_{IO}		3.6	V
V_{ILCLK}	CLK Input Low Voltage				–0.2		0.3 x V_{IO}	V
V_{IHCLK}	CLK Input High Voltage				0.7 x V_{CC}		2.75	V
V_{ID}	Voltage for Autoselect	V_{CC} = 2.5 V			11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min}$					0.45	V
I_{OLRB}	RY/BY#, Output Low Current	V_{OL} = 0.4 V			8			mA
V_{HH}	Accelerated (ACC pin) High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min}$			0.85 x V_{CC}			V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$			V_{IO} –0.1		V_{IO}	V
V_{LKO}	Low V_{CC} Lock-Out Voltage (Note 3)				1.6		2.0	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component.*
2. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
3. *Not 100% tested.*
4. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CCmax}$.*

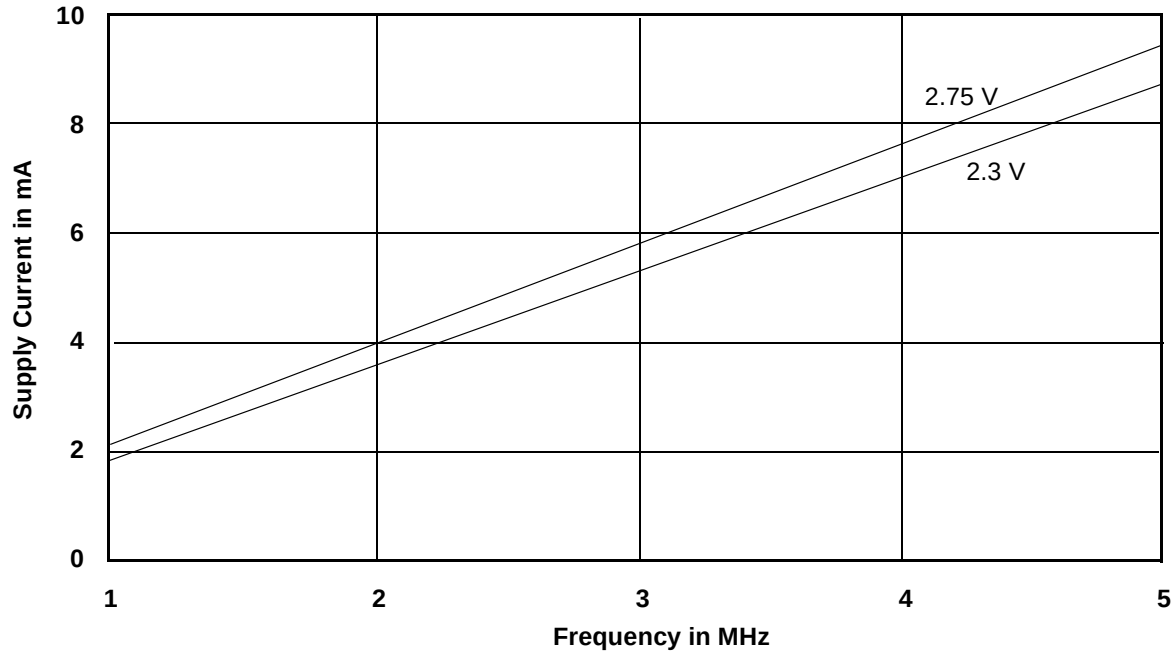
DC CHARACTERISTICS (Continued)

Zero Power Flash



Note: *Addresses are switching at 1 MHz*

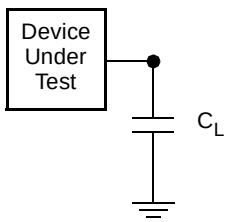
Figure 15. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 16. Typical I_{CC1} vs. Frequency

TEST CONDITIONS



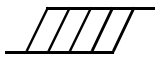
Note: *Diodes are IN3064 or equivalent*

Figure 17. Test Setup

Table 23. Test Specifications

Test Condition	54D, 65D, 64C, 80C	65A, 90A	Unit
Output Load	1 TTL gate		
Output Load Capacitance, C_L (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0.0 V – V_{IO}		V
Input timing measurement reference levels	$V_{IO}/2$		V
Output timing measurement reference levels	$V_{IO}/2$		V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

SWITCHING WAVEFORMS

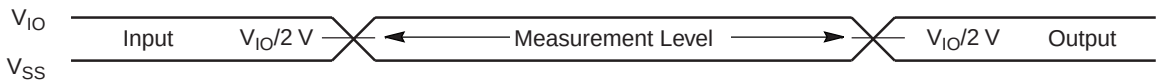


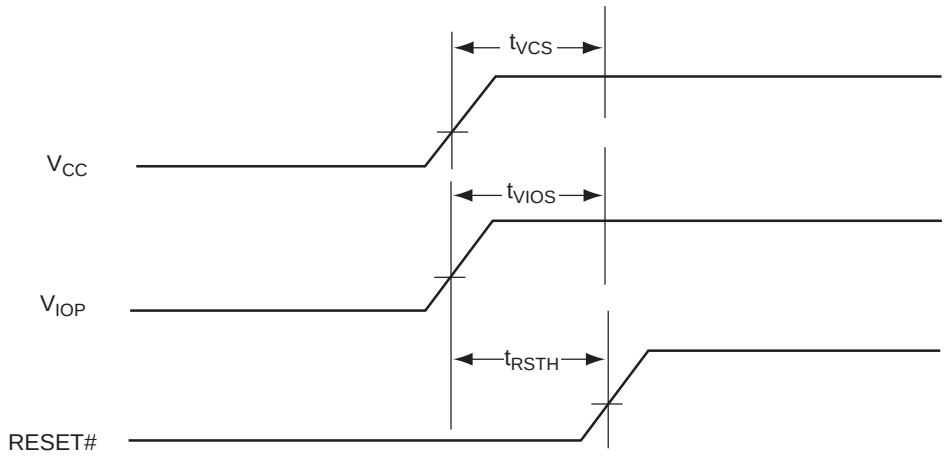
Figure 18. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

V_{CC} and V_{IO} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	50	µs
t_{VIOS}	V_{IO} Setup Time	Min	50	µs
t_{RSTH}	RESET# Low Hold Time	Min	50	µs

Figure 19. V_{CC} and V_{IO} Power-up Diagram



AC CHARACTERISTICS

Asynchronous Read Operations

Parameter		Description		Test Setup		Speed Options						Unit
JEDEC	Std.					54D	65D	64C	80C	65A	90A	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Max	54	65	64	80	65	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE# = V_{IL} OE# = V_{IL}	Max	54	65	64	80	65	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	54	65	64	80	65	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	20						ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	10						ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Min	2						ns
					Max	10						ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0						ns
			Toggle and Data# Polling		Min	10						ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (Note 1)			Min	2						ns

Notes:

1. *Not 100% tested.*
2. *See Figure 17 and Table 23 for test specifications*

AC CHARACTERISTICS

Burst Mode Read

Parameter		Description		Speed Options						Unit
JEDEC	Std.			54D	65D	64C	80C	68A	90A	
	t_{IACC}	Asynchronous Access Time ADV# Valid Clock to Output Delay (See Note)	Max	54	65	64	80	68	90	ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	8		10		17		ns
	t_{ADVCS}	ADV# Setup Time to Rising (Falling) Edge of CLK	Min	4		5		7		ns
	t_{ADVCH}	ADV# Hold Time	Min	2						ns
	t_{ADVP}	ADV# Pulse Width	Min	15		15		18		ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Max	4						ns
	t_{BACC}	CLK to Valid Data Out Delay	Max	8		10		17		ns
	t_{DVCH}	Valid Data Hold from CLK	Min	2		3		3		ns
	t_{DIND}	CLK to Valid IND/WAIT#	Max	8		10		17		ns
	t_{INDH}	IND/WAIT# Hold from CLK	Min	2		3		3		ns
	t_{IACC}	CLK to Valid Data Out, Initial Burst Access	Max	54		60		68		ns
	t_{CLK}	CLK Period	Min	15		18		25		ns
			Max	60						
	t_{CR}	CLK Rise Time	Max	3						ns
	t_{CF}	CLK Fall Time	Max	3						ns
	t_{CH}	CLK High Time	Min	2.5		2.5		3		ns
	t_{CL}	CLK Low Time	Min	2.5		2.5		3		ns
	t_{DS}	Data Setup to WE# Rising Edge	Min	15		15		16		ns
	t_{DH}	Data Hold from WE# Rising Edge	Min	0						ns
	t_{AS}	Address Setup to Falling Edge of WE#	Min	0						ns
	t_{AH}	Address Hold from Falling Edge of WE#	Min	25		30		33		ns
	t_{CS}	CE# Setup Time	Min	3						ns
	t_{CH}	CE# Hold Time	Min	3						ns
	t_{ACS}	Address Setup Time to CLK (See Note)	Min	5		6		7		ns
	t_{ACH}	Address Hold Time from ADV# Rising Edge (See Note)	Min	1		2		2		ns
	t_{OE}	Output Enable to Output Valid	Max	20						ns
t_{DF}	t_{OEZ}	Output Enable to Output High Z	Min	2		3		3		ns
			Max	10		15		17		
t_{EHQZ}	t_{CEZ}	Chip Enable to Output High Z	Max	10		15		17		ns
	t_{CES}	CE# Setup Time to Clock	Min	4		5		6		ns

Note: *See Product Selector Guide for minimum initial clock delay prior to initial valid data. t_{IACC} may also be calculated using the following formula: t_{IACC} = (clock delays) x (clock period) + t_{BACC}.*

AC CHARACTERISTICS

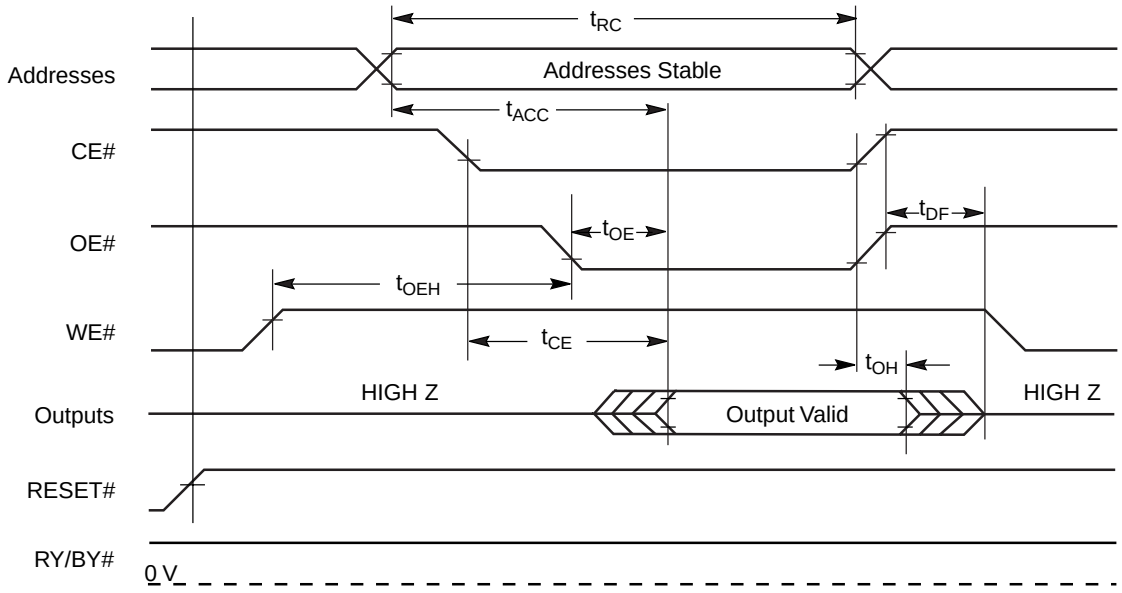


Figure 20. Conventional Read Operations Timings

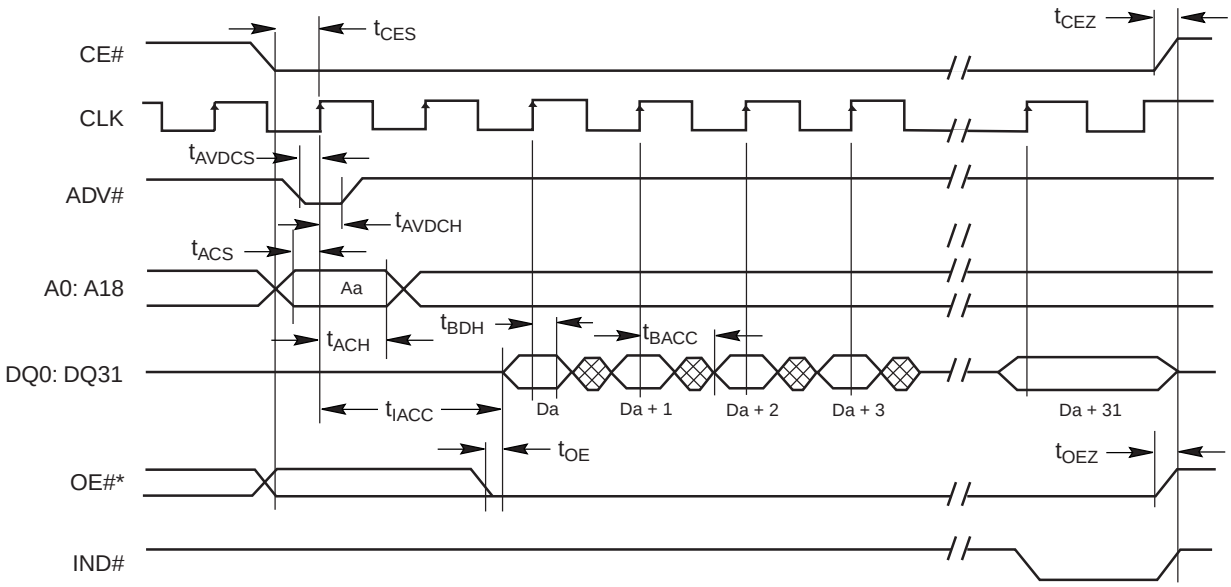


Figure 21. Burst Mode Read (x32 Mode)

AC CHARACTERISTICS

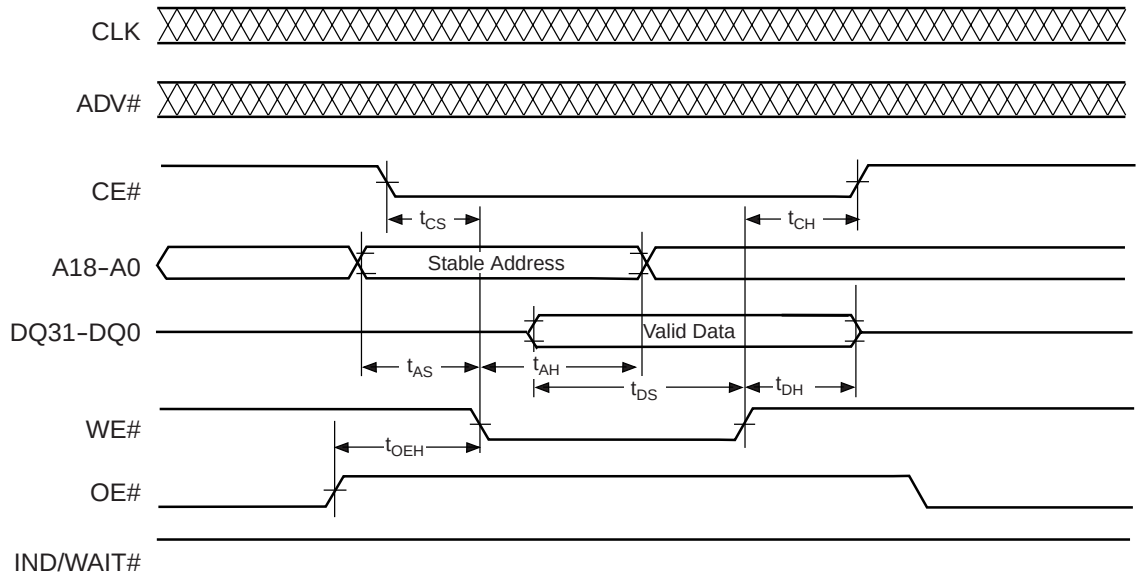


Figure 22. Asynchronous Command Write Timing

Note: *All commands have the same number of cycles in both asynchronous and synchronous modes, including the READ/RESET command. Only a single array access occurs after the F0h command is entered. All subsequent accesses are burst mode when the burst mode option is enabled in the Configuration Register.*

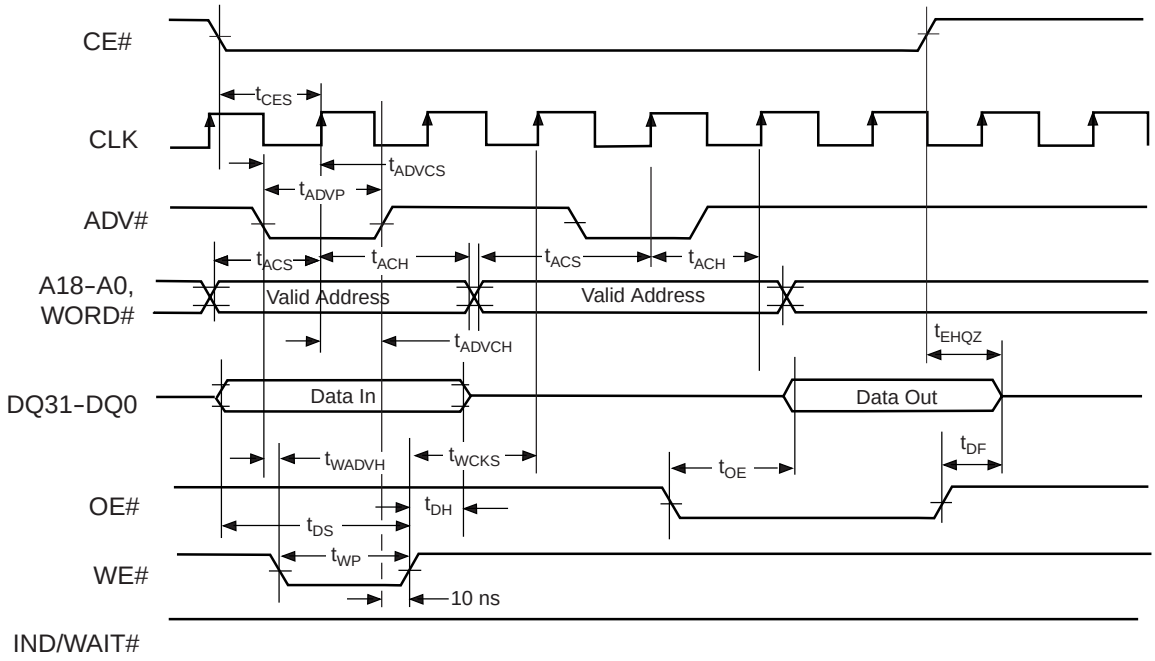


Figure 23. Synchronous Command Write/Read Timing

Note: *All commands have the same number of cycles in both asynchronous and synchronous modes, including the READ/RESET command. Only a single array access occurs after the F0h command is entered. All subsequent accesses are burst mode when the burst mode option is enabled in the Configuration Register.*

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description	Test Setup		All Speed Options	Unit
JEDEC	Std.					
	t_{READY}	RESET# Pin Low (During Embedded Algorithms) to Read or Write (See Note)		Max	20	µs
	t_{READY}	RESET# Pin Low (NOT During Embedded Algorithms) to Read or Write (See Note)		Max	500	ns
	t_{RP}	RESET# Pulse Width		Min	500	ns
	t_{RH}	RESET# High Time Before Read (See Note)		Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode		Min	20	µs
	t_{RB}	RY/BY# Recovery Time		Min	0	ns
	t_{READY}	RESET# Active for Bank NOT Executing Embedded Algorithm		Max	500	ns
	t_{RH}	RESET# High Time before Read		Max	50	ns
	t_{READY}	RESET# Active for Bank Executing Embedded Algorithm		Max	20	µs
	t_{DRNE}	RESET# Delay to Read Mode During Normal Erase		Max	7	µs
	t_{RMX}	RESET# Delay to Read Mode if RESET# is held active for maximum delay (see previous two parameters)		Max	50	ns

Note: *Not 100% tested.*

AC CHARACTERISTICS

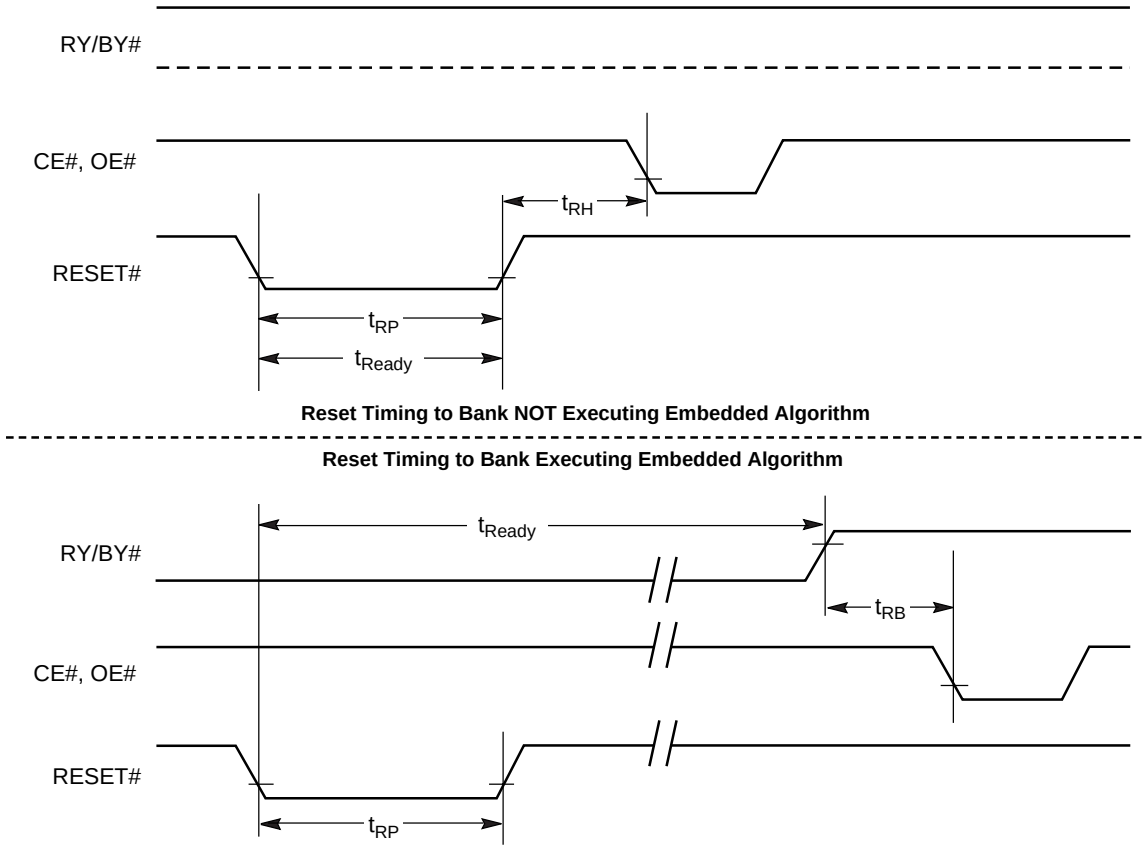


Figure 24. RESET# Timings

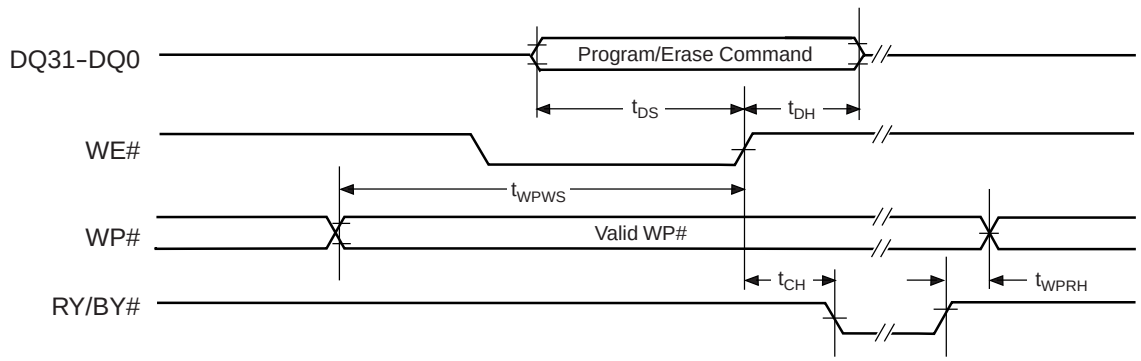


Figure 25. WP# Timing

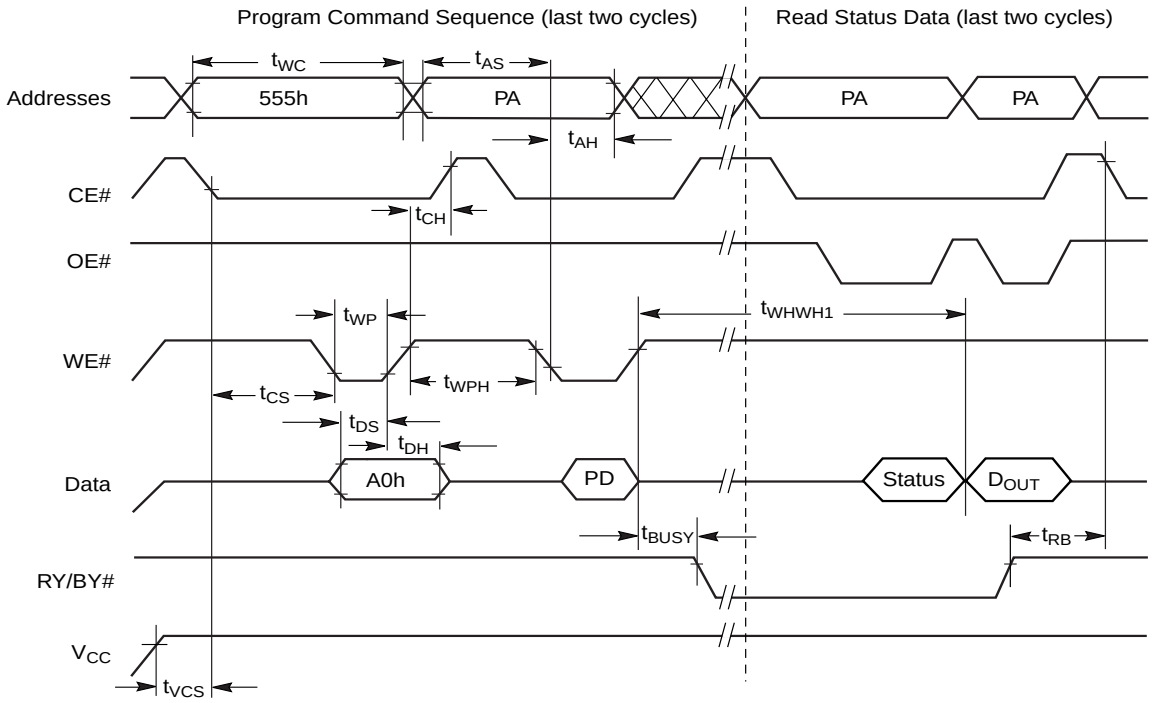
AC CHARACTERISTICS
Erase/Program Operations

Parameter					
JEDEC	Std.	Description		All Speed Options	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	60	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	25	ns
t_{DVWH}	t_{DS}	Data Setup to WE# Rising Edge	Min	15	ns
t_{WHDX}	t_{DH}	Data Hold from WE# Rising Edge	Min	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time	Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time	Min	0	ns
		CE# Setup to CLK	Min	7	
t_{WLWH}	t_{WP}	WE# Width	Min	25	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5	sec.
	t_{VCS}	V_{CC} Setup Time (Note 1)	Min	50	µs
	t_{RB}	Recovery Time from RY/BY#	Min	0	ns
	t_{BUSY}	RY/BY# Delay After WE# Rising Edge	Max	90	ns
	t_{WPWS}	WP# Setup to WE# Rising Edge with Command	Min	20	ns
	t_{WPRH}	WP# Hold after RY/BY# Rising Edge	Max	2	ns

Notes:

1. *Not 100% tested.*
2. *See the section for more information.*

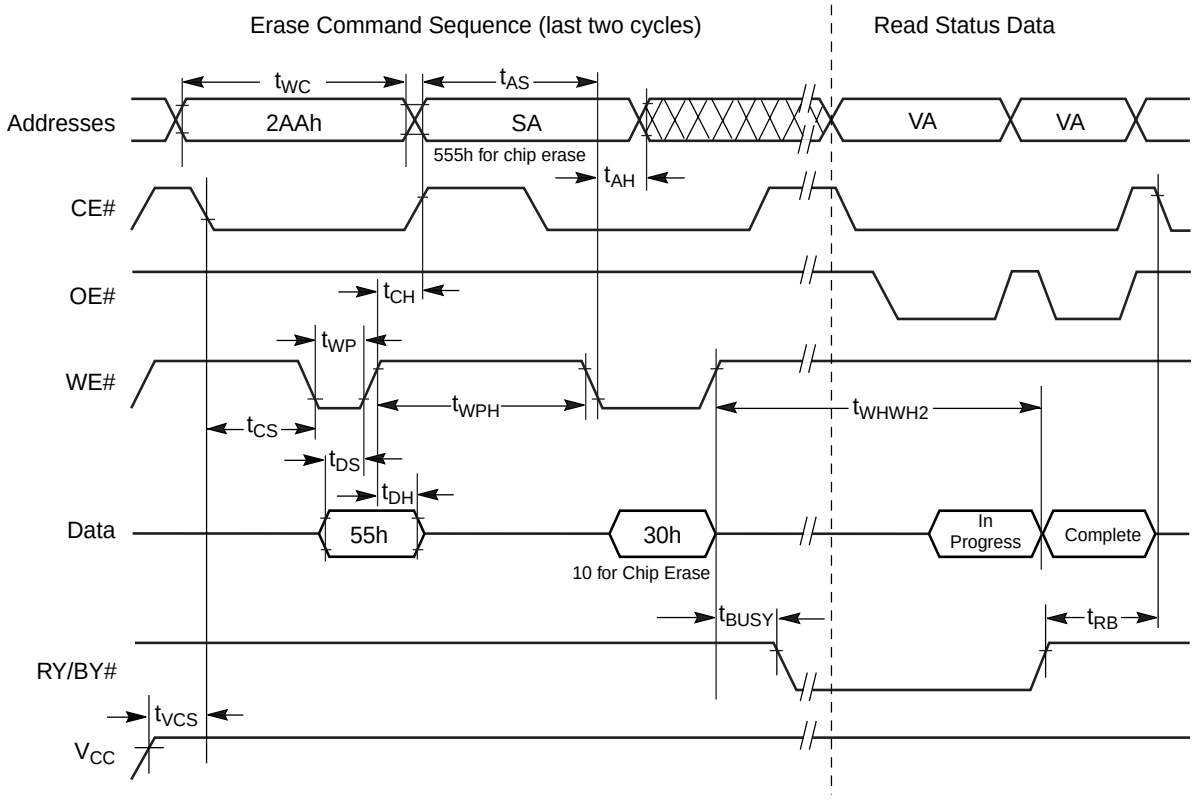
AC CHARACTERISTICS



Note: *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*

Figure 26. Program Operation Timings

AC CHARACTERISTICS



Note: *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status).*

Figure 27. Chip/Sector Erase Operation Timings

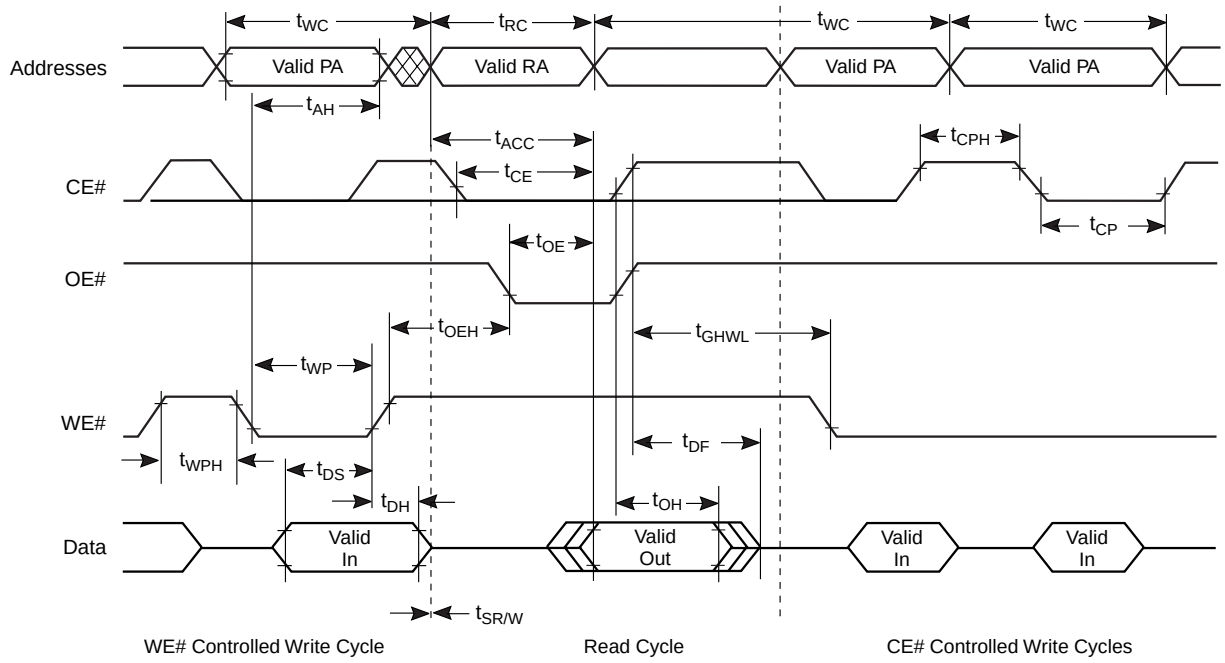
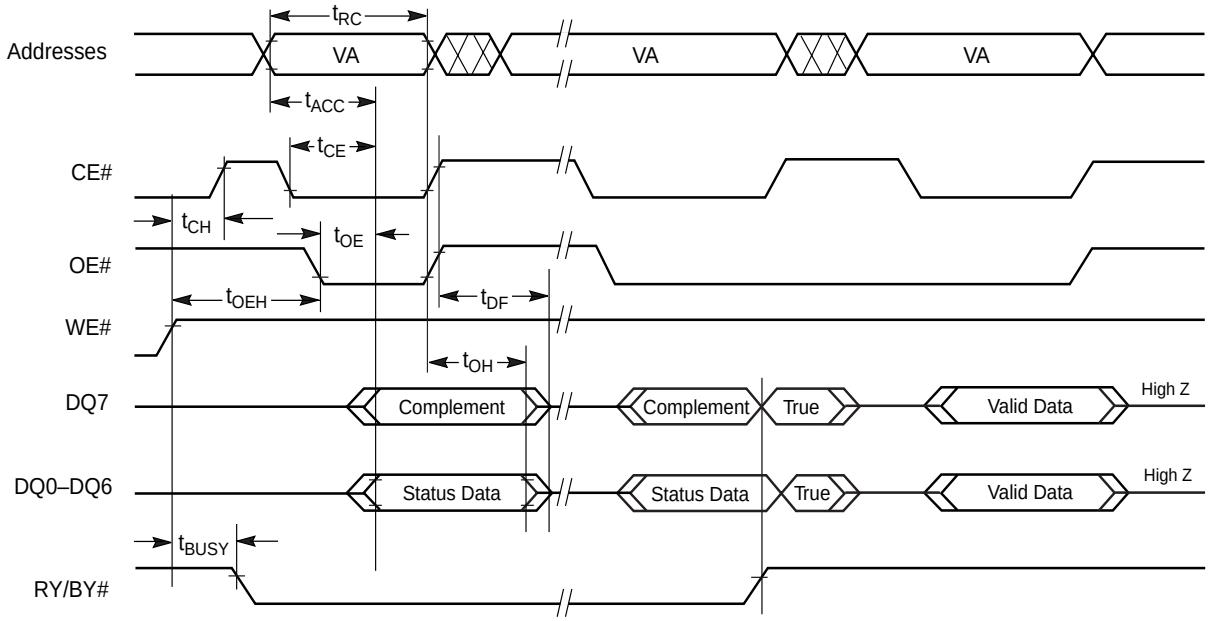


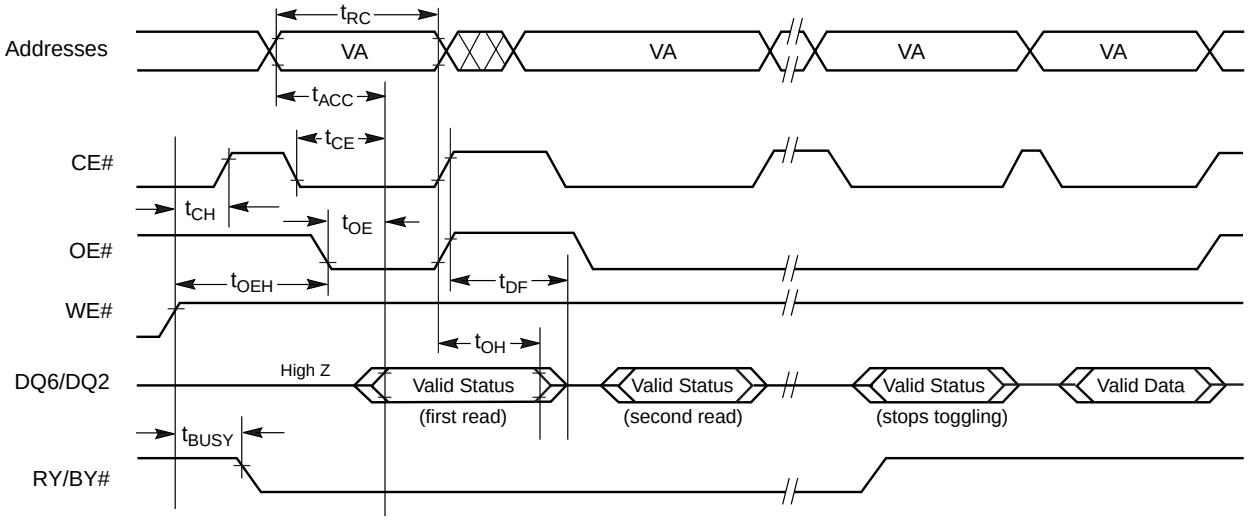
Figure 28. Back-to-back Cycle Timings

AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

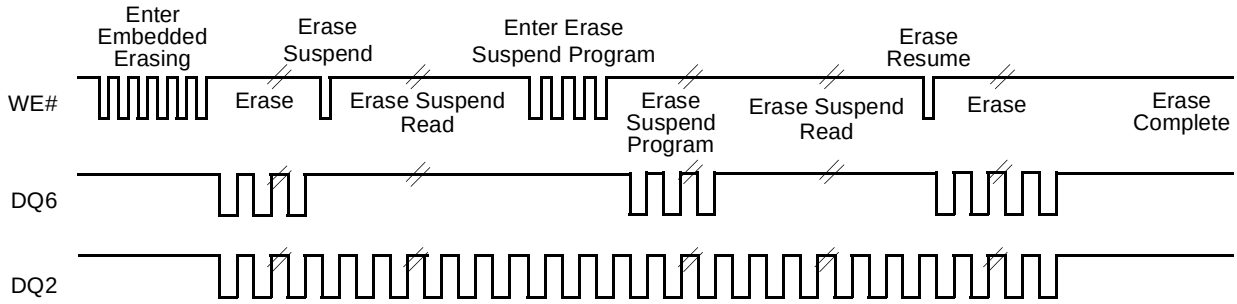
Figure 29. Data# Polling Timings (During Embedded Algorithms)



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

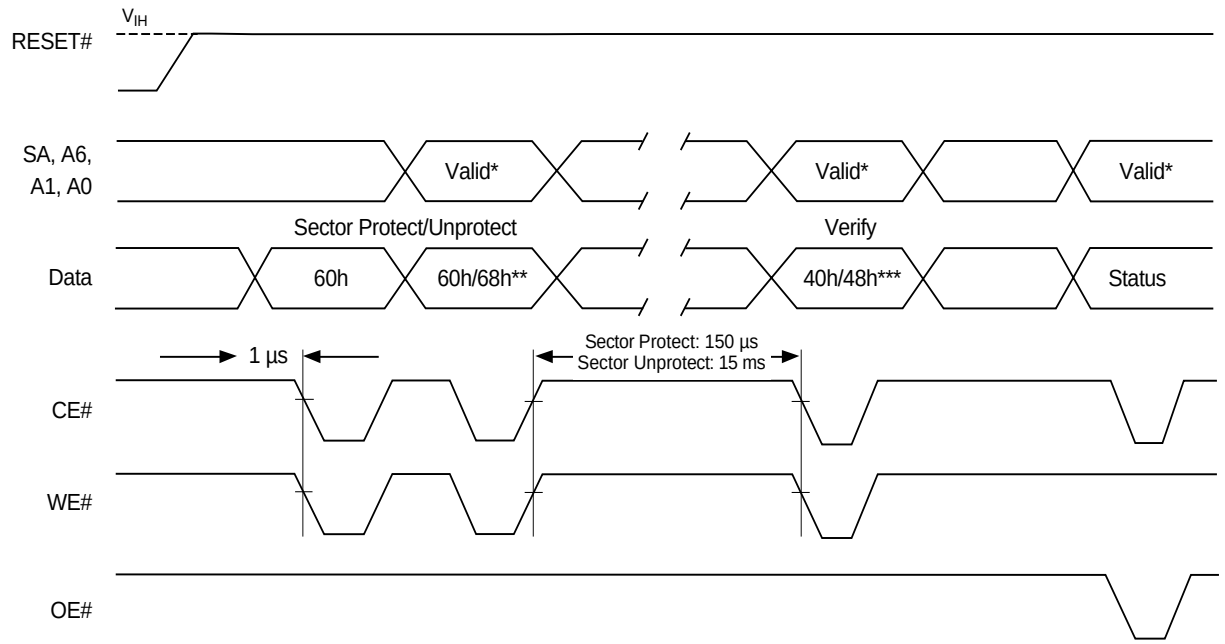
Figure 30. Toggle Bit Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *The system may use CE# or OE# to toggle DQ2 and DQ6. DQ2 toggles only when read at an address within an erase-suspended sector.*

Figure 31. DQ2 vs. DQ6 for Erase and Erase Suspend Operations



** Valid address for sector protect: A6 = 0, A1 = 1, A0 = 0. Valid address for sector unprotect:A6 = 1, A1 = 1, A0 = 0.*

*** Command for sector protect is 68h. Command for sector unprotect is 60h.*

**** Command for sector protect verify is 48h. Command for sector unprotect verify is 40h.*

Figure 32. Sector Protect/Unprotect Timing Diagram

AC CHARACTERISTICS

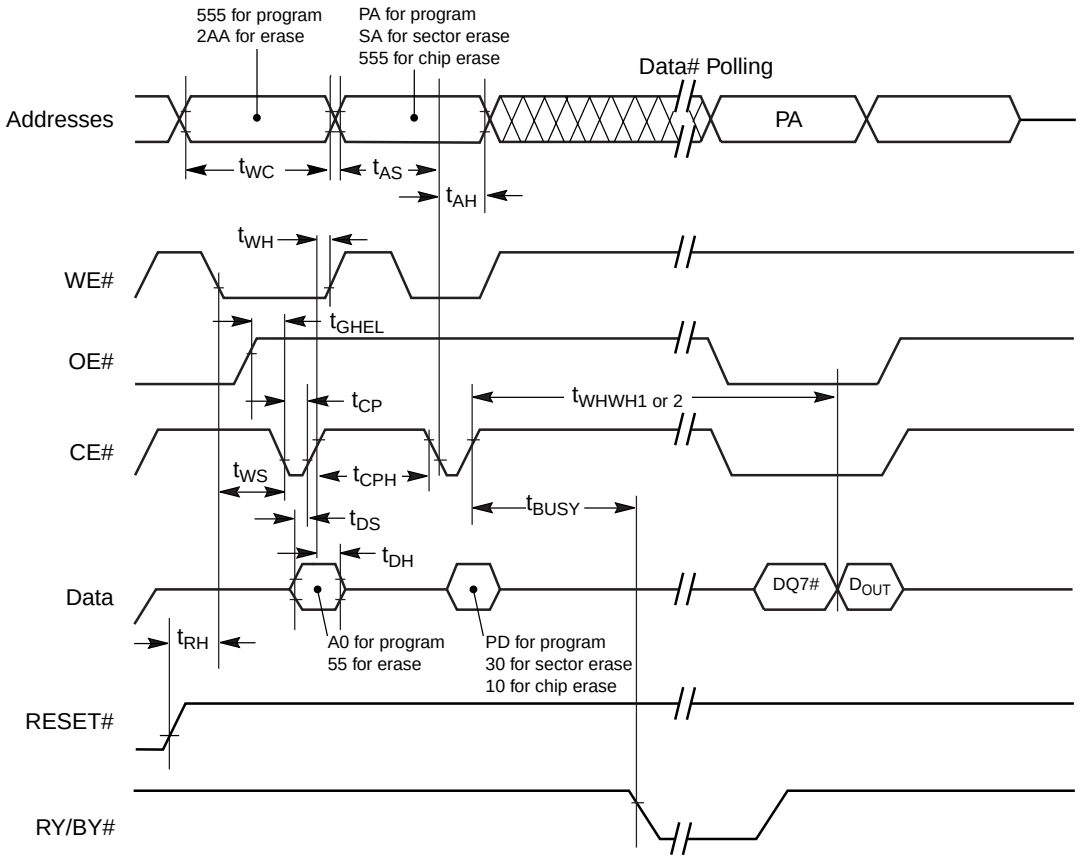
Alternate CE# Controlled Erase/Program Operations

Parameter					
JEDEC	Std.	Description		All Speed Options	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	65	ns
t_{AVEL}	t_{AS}	Address Setup Time	Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min	45	ns
t_{DVEH}	t_{DS}	Data Setup Time	Min	35	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time	Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time	Min	0	ns
	t_{WADVS}	WE# Rising Edge Setup to ADV# Falling Edge	Min	5	ns
	t_{WP}	WE# Width	Min	15	ns
	t_{WADVH}	WE# Falling Edge After ADV# Falling Edge	Min	0	ns
	t_{WCKS}	WE# Rising Edge Setup to CLK Rising Edge	Min	5	ns
t_{ELEH}	t_{CP}	CE# Pulse Width	Min	35	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High	Min	30	ns
t_{WHWsH1}	t_{WHWH1}	Programming Operation (Note 2)	Typ	9	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)	Typ	0.5	sec.

Notes:

1. *Not 100% tested.*
2. *See the section for more information.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, DQ7# = complement of the data written to the device, D_{OUT} = data written to the device.*
2. *Figure indicates the last two bus cycles of the command sequence.*

Figure 33. Alternate CE# Controlled Write Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	5	s	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		23	230	s	
Double Word Program Time		18	250	µs	Excludes system level overhead (Note 5)
Word (x16) Program Time		15	210	µs	
Accelerated Double Word Program Time		8	130	µs	
Accelerated Chip Program Time		5	50	s	
Chip Program Time (Note 3)	x16	10	100	s	
	x32	12	120		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 2.5 V V_{CC}, 1M cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 145°C, V_{CC} = 2.5 V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Tables 19 and 20 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1M cycles.*
7. *PPBs have a minimum program/erase cycle endurance of 100 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, ACC, and WP#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.

PQFP AND FORTIFIED BGA PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

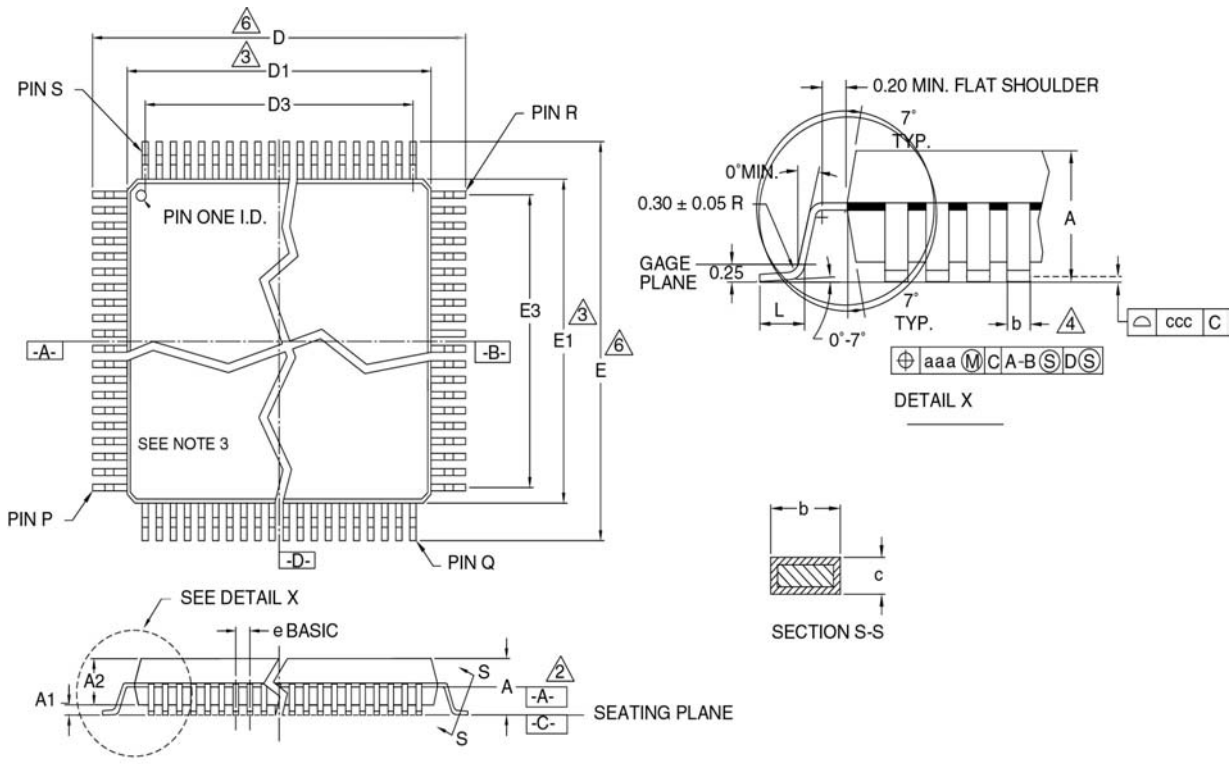
1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PHYSICAL DIMENSIONS

PQR080–80-Lead Plastic Quad Flat Package



PACKAGE	PQR 080			NOTES
JEDEC	MO-108(B)CB-1			
SYMBOL	MIN	NOM	MAX	
A	--	--	3.35	
A1	0.25	--	--	
A2	2.70	2.80	2.90	
b	0.30	--	0.45	SEE NOTE 4
c	0.15	--	0.23	
D	17.00	17.20	17.40	
D1	13.90	14.00	14.10	SEE NOTE 3
D3	--	12.0	--	REFERENCE
e	--	0.80	--	BASIC, SEE NOTE 7
E	23.00	23.20	23.40	
E1	19.90	20.00	20.10	SEE NOTE 3
E3	--	18.40	--	REFERENCE
aaa	---	0.20	---	
ccc		0.10		
L	0.73	0.88	1.03	
P		24		
Q		40		
R		64		
S		80		

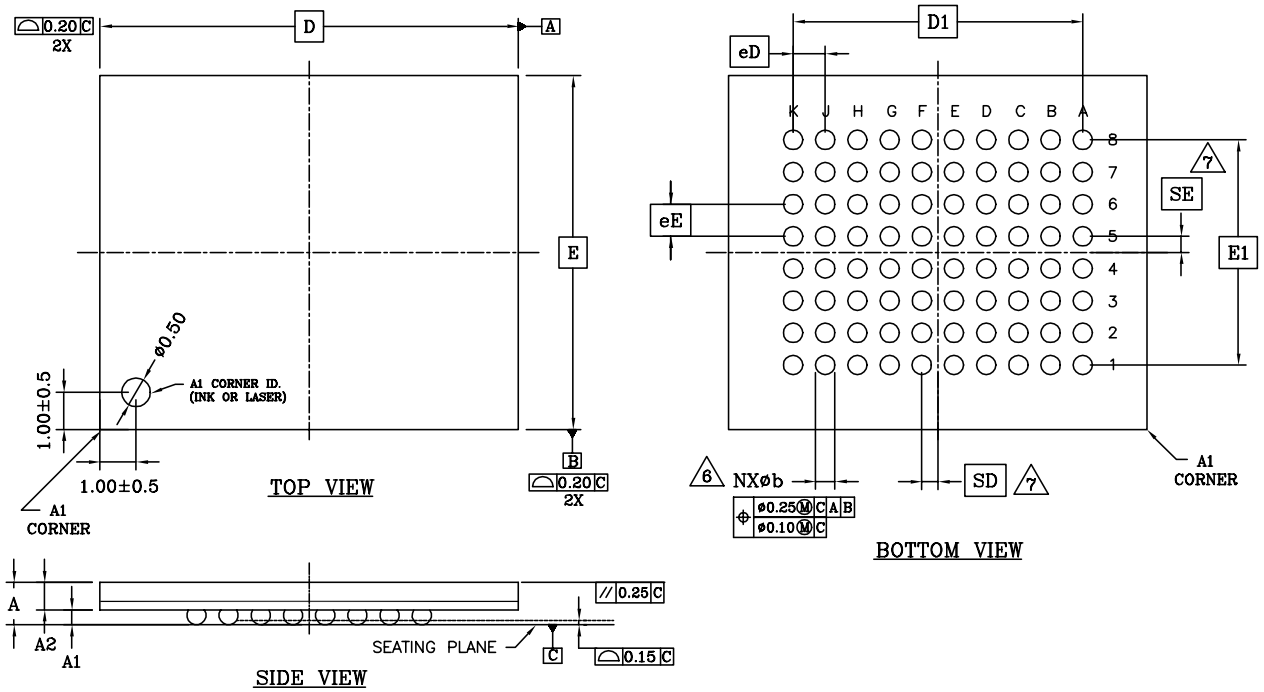
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -A- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUD MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -A-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD-TIP TRUE POSITION SHALL BE WITHIN ±0.0076 mm FOR PITCH > 0.5 mm AND WITHIN ±0.04 FOR PITCH ≤ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06-500)
   1 - 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65 - 0.80 mm
   2 - 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06-500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE WITHIN ±0.0085".

3213\38.4C

PHYSICAL DIMENSIONS

LAA 080–80-ball Fortified Ball Grid Array (13 x 11 mm)



PACKAGE	XLAA 080		
JEDEC	N/A		
	13.00x11.00 mm PACKAGE		
SYMBOL	MIN.	NOM.	MAX.
A	–	–	1.40
A1	0.40	–	–
A2	0.60	–	–
D	13.00 BSC.		
E	11.00 BSC.		
D1	9.00 BSC.		
E1	7.00 BSC.		
MD	10		
ME	8		
N	80		
øb	0.50	0.60	0.70
eD	1.00 BSC.		
eE	1.00 BSC.		
SD/SE	0.50 BSC.		
–			
	A		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME .

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C .

7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

REVISION SUMMARY

Revision B (September 30, 2002)

Initial public release.

Revision B+1 (October 7, 2002)

Distinctive Characteristics

Changed maximum power consumption on burst mode read, program/erase operations, and standby mode.

Burst Mode Read table

Changed t_{CES} specification from 7, 8, and 9 ns to 4, 5, and 6 ns, respectively.

DC Characteristics table

Deleted I_{CC2} specification. Changed I_{CCB} OE# test condition from V_{IH} to V_{IL}. Added 1 MHz test condition to I_{CC1}; changed OE# test condition from V_{IH} to V_{IL}. Changed I_{CC3} and I_{CC4} maximum values and added typical values. Changed maximum values for I_{CC5}, I_{CC7}, and I_{CC8}. Added Note 4 to table.

AC Characteristics

Erase and Program Operations table: Replaced TBDs for t_{AH} and t_{WP} with values.

Erase and Programming Performance table

Replaced TBDs and existing typical and maximum values with new values.