SONY

CXP878P60

CMOS 8-bit Single Chip Microcomputer

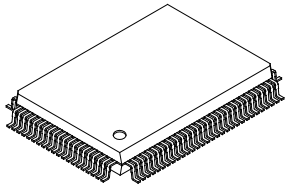
Description

The CXP878P60 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, high precision timing pattern generation circuit, PWM output, VISS/VASS circuit, 32kHz timer/counter, remote control reception circuit, HSYNC counter, VSYNC separator and the measurement circuit which measures signals of capstan FG and drum FG/PG and other servo systems, as well as basic configurations like 8-bit CPU, PROM, RAM and I/O port. They are integrated into a single chip.

Also the CXP878P60 provides sleep/stop functions which enable to lower power consumption.

The CXP878P60 is the PROM-incorporated version of the CXP87860 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system developement and for small-quantity production.

100 pin QFP (PIastic)



Structure

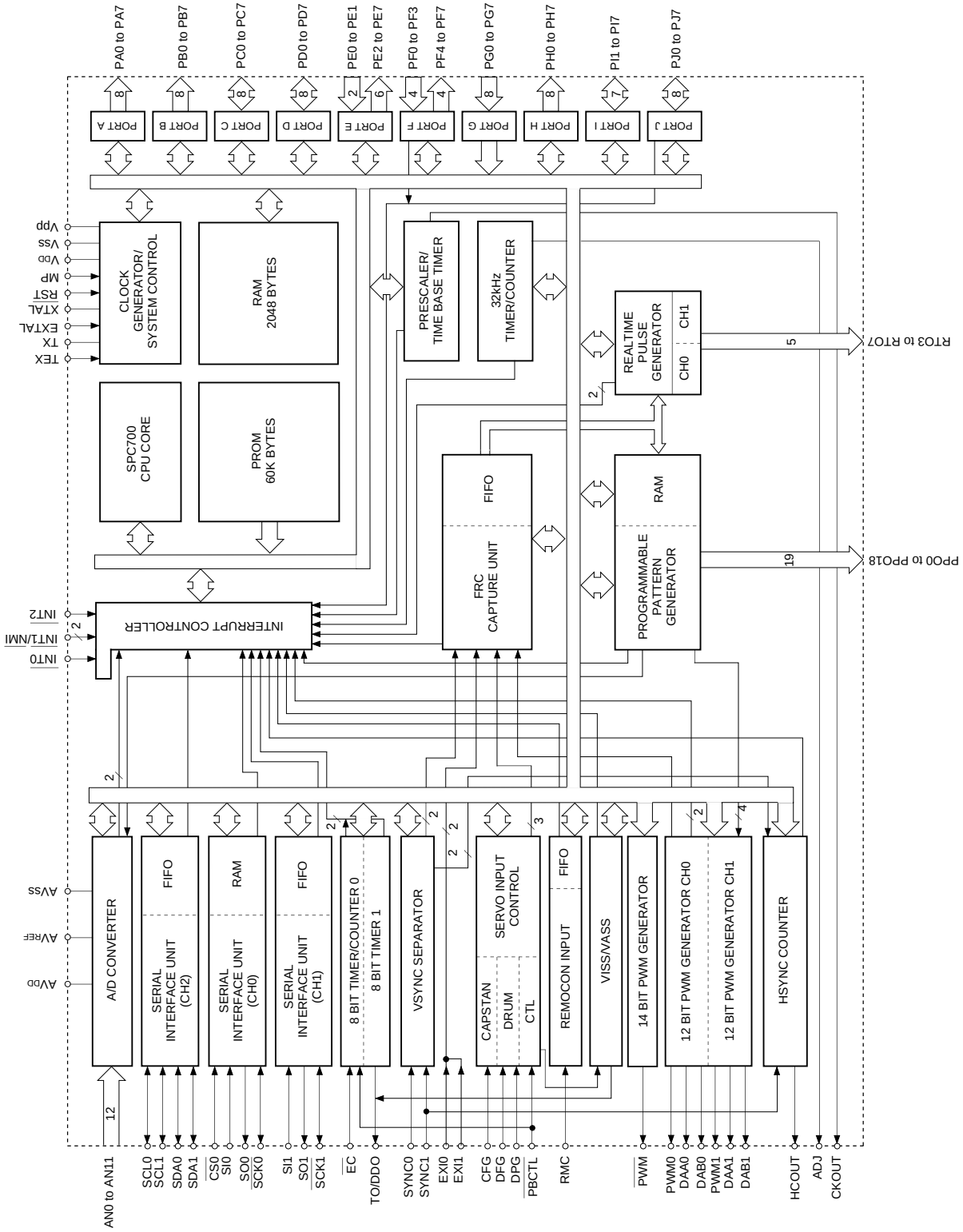
Silicon gate CMOS IC

Features

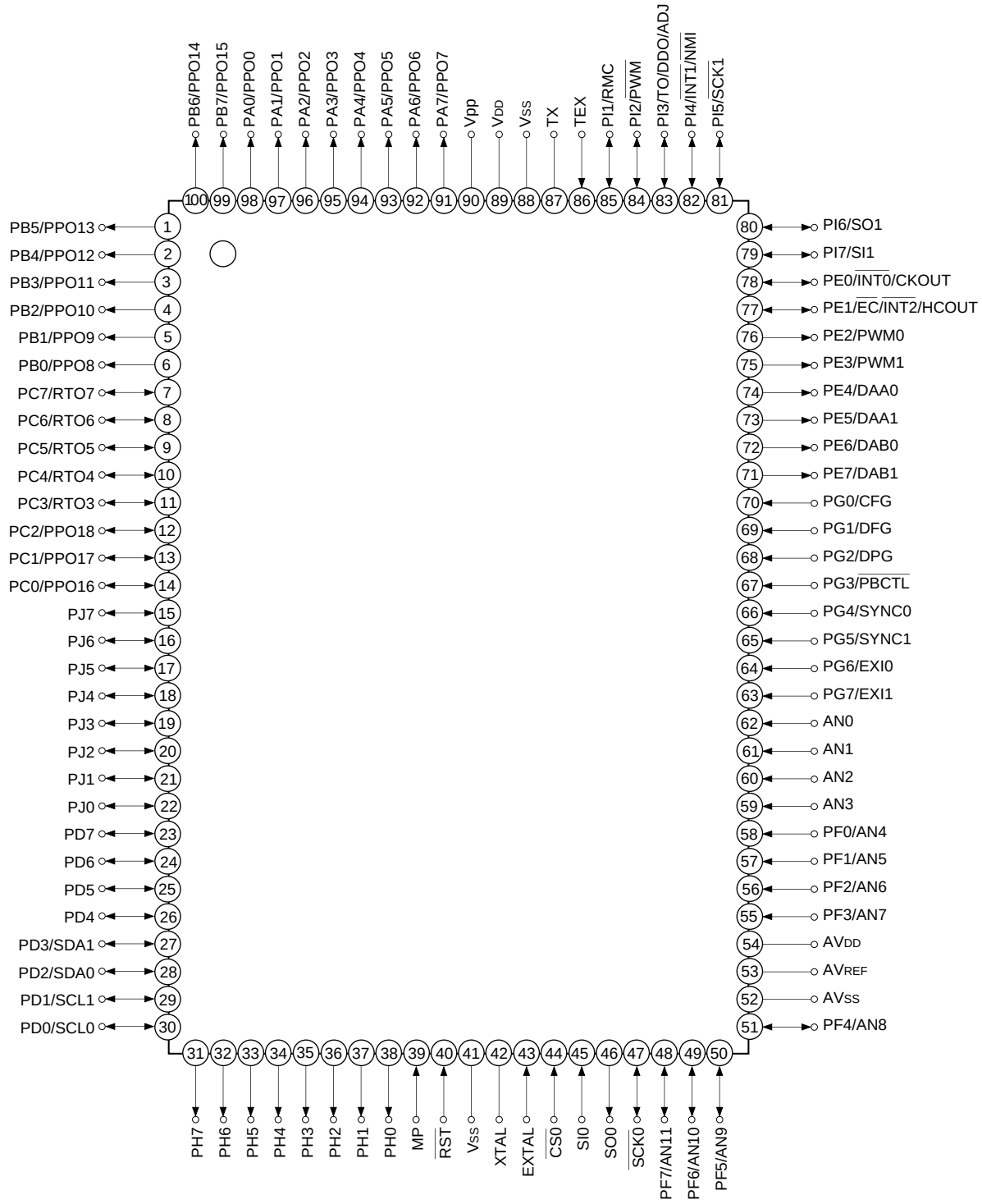
- A wide instruction set (213 instructions) which covers various types of data
  — 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle 250ns at 16MHz operation (4.5V to 5.5V)
  122µs at 32kHz operation
- Incorporated PROM capacity 60K bytes
- Incorporated RAM capacity 2048 bytes
- Peripheral functions
  - — A/D converter: 8 bits, 12 channels, successive approximation system (Conversion time of 20.0µs at 16MHz)
  - — Serial interface: Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 1 channel
    Incorporated 8-bit and 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel
    Incorporated two-wire 8-bit and 8-stage FIFO (Auto transfer for 1 to 8 bytes), 1 channel
  - — Timer: 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 32kHz timer/counter
  - — High precision timing pattern generator: PPG: maximum of 19 pins, 32 stages programmable
    RTG: 5 pins, 2 channels
  - — PWM/DA gate output: PWM: 12 bits, 2 channels (Repetitive frequency of 62kHz at 16MHz)
    DA gate pulse output: 13 bits, 4 channels
  - — Servo input control: Capstan FG, drum FG/PG, CTL input
  - — VSYNC separator
  - — FRC capture unit: Incorporated 26-bit and 8-stage FIFO
  - — PWM output: 14 bits
  - — VISS/VASS circuit: Pulse duty auto detection circuit
  - — Remote control reception circuit: 8-bit pulse measurement counter with on-chip, 6-stage FIFO
  - — HSYNC counter: 12-bit event counter (Counts SYNC1 input.)
- Interruption: 23 factors, 15 vectors, multi-interruption possible
- Standby mode: Sleep/stop
- Package: 100-pin plastic QFP

E96214-PS

Block Diagram



Pin Assignment (Top View)



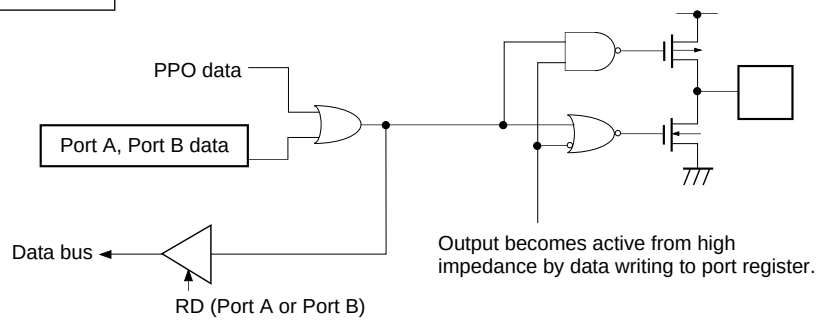
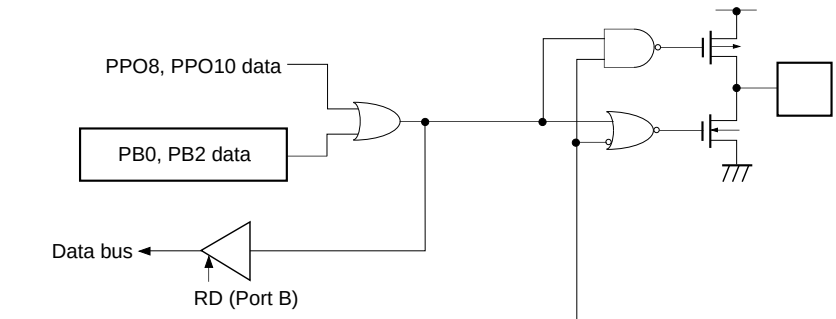
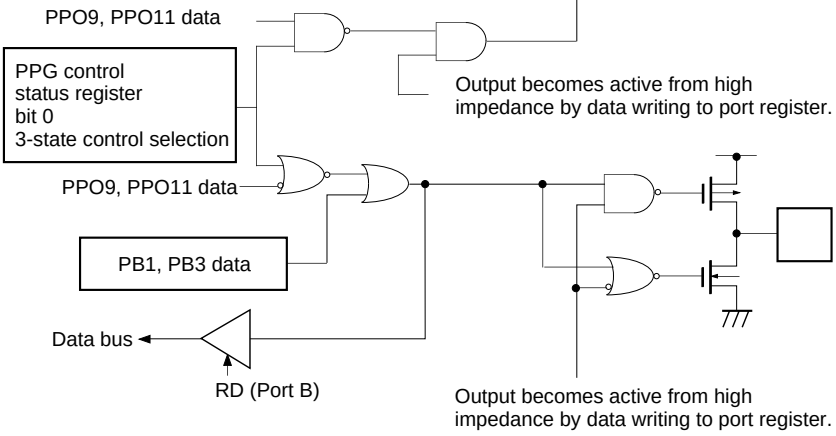
Note) 1. Vpp (Pin 90) is always connected to V_{DD}.
2. Vss (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) is always connected to GND.

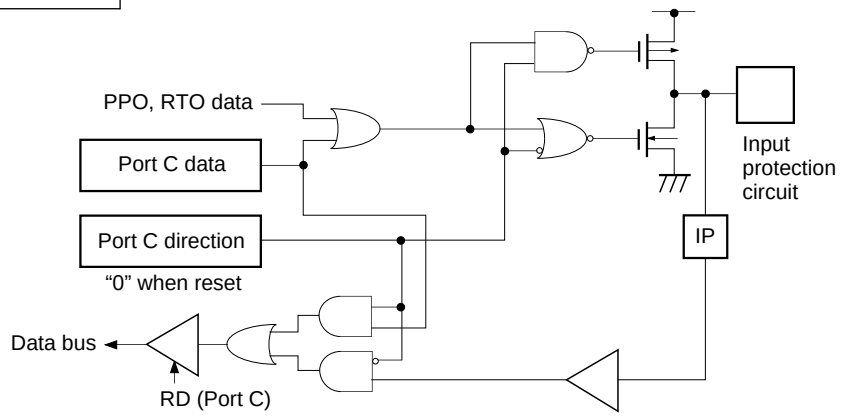
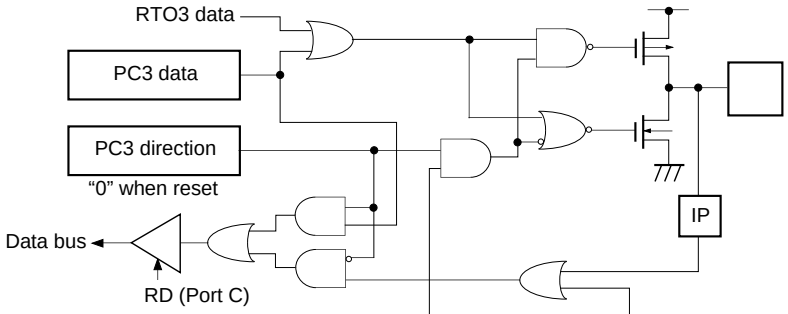
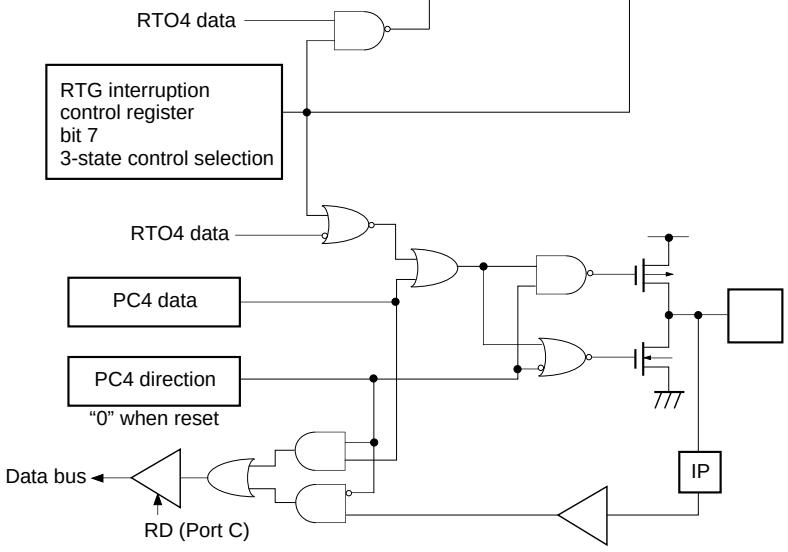
Pin Description

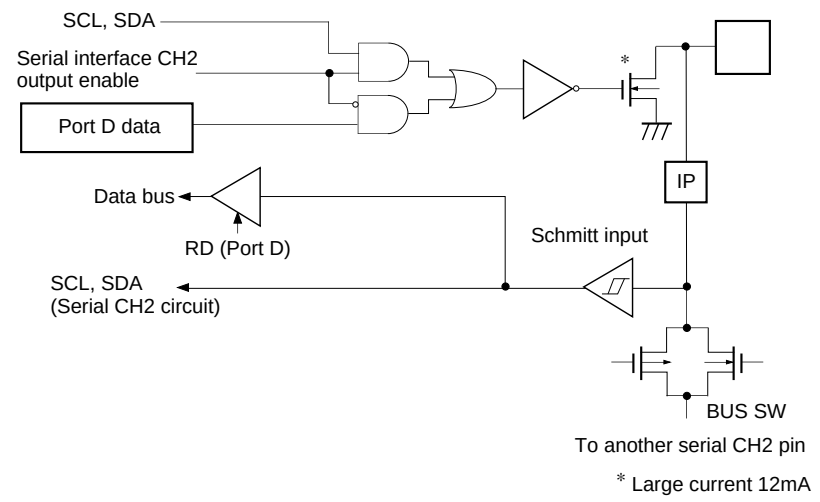
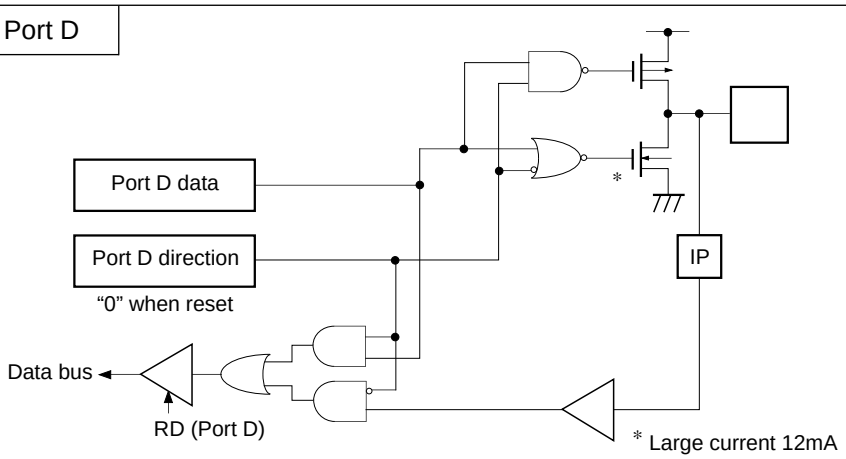
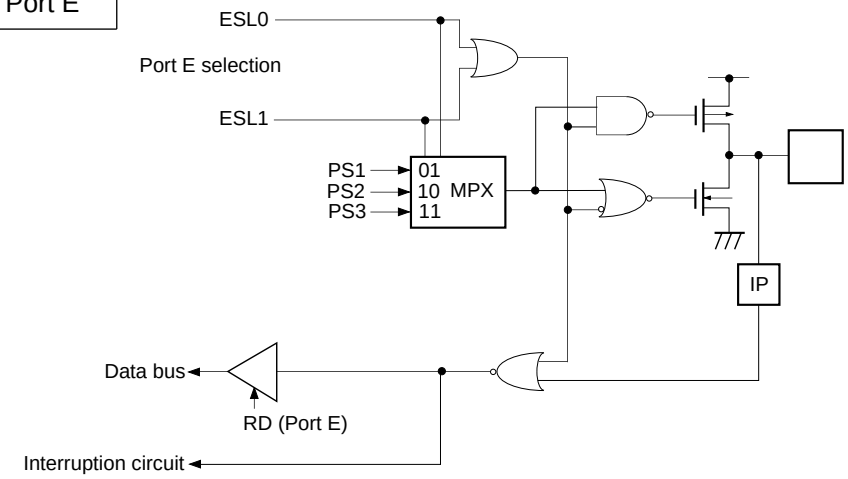
<table>
<tr><th>Symbol</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td>PA0/PPO0
to
PA7/PPO7</td><td>Output/
Real-time
output</td><td colspan="2">(Port A)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td><td colspan="2" rowspan="3">Programmable pattern generator (PPG) output.
Functions as high precision real-time pulse output port.
PB0 and PB2 can be 3-state controlled with PPG.
(19 pins)</td></tr>
<tr><td>PB0/PPO8
to
PB7/PPO15</td><td>Output/
Real-time
output</td><td colspan="2">(Port B)
8-bit output port. Data is gated with PPO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC0/PPO16
to
PC2/PPO18</td><td>I/O/
Real-time
output</td><td colspan="2" rowspan="2">(Port C)
8-bit I/O port. I/O can be set in a unit of single bits.
Data is gated with PPO or RTO contents by OR-gate and they are output.
(8 pins)</td></tr>
<tr><td>PC3/RTO3
to
PC7/RTO7</td><td>I/O/
Real-time
output</td><td colspan="2">Real-time pulse generator (RTG) output.
Functions as high precision real-time pulse output port. PC3 can be 3-state controlled with RTG. (5 pins)</td></tr>
<tr><td>PD0/SCL0
PD1/SCL1</td><td rowspan="3">I/O</td><td colspan="3" rowspan="3">(Port D)
8-bit I/O port. I/O can be set in a unit of single bits for upper 4 bits.
Can drive 12mA sink current.
Lower 4-bit output is N-ch open drain. (8 pins)</td><td>Serial clock (CH2) I/O. (2 pins)</td></tr>
<tr><td>PD2/SDA0
PD3/SDA1</td><td>Serial data (CH2) I/O. (2 pins)</td></tr>
<tr><td>PD4 to PD7</td></tr>
<tr><td>PE0/$\overline{\text{INT0}}$/
CKOUT</td><td>Input/Input/Output</td><td rowspan="8">(Port E)
8-bit port.
Lower 2 bits are for inputs; upper 6 bits are for outputs.
(8 pins)</td><td colspan="2">Input to request external interruption.
Active at the falling edge.</td><td>System clock frequency dividing output.</td></tr>
<tr><td>PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$/
HCOUT</td><td>Input/Input/Input/
Output</td><td>External event input for timer/counter.</td><td>Input to request external interruption.
Active at the falling edge.</td><td>Coinsidence signal output of HSYNC counter.</td></tr>
<tr><td>PE2/PWM0</td><td>Output/Output</td><td colspan="3" rowspan="2">PWM outputs.
(2 pins)</td></tr>
<tr><td>PE3/PWM1</td><td>Output/Output</td></tr>
<tr><td>PE4/DAA0</td><td>Output/Output</td><td colspan="3" rowspan="4">DA gate pulse outputs.
(4 pins)</td></tr>
<tr><td>PE5/DAA1</td><td>Output/Output</td></tr>
<tr><td>PE6/DAB0</td><td>Output/Output</td></tr>
<tr><td>PE7/DAB1</td><td>Output/Output</td></tr>
<tr><td>AN0 to AN3</td><td>Input</td><td colspan="4">Analog input to A/D converter. (12 pins)</td></tr>
<tr><td>PF0/AN4
to
PF3/AN7</td><td>Input/Input</td><td colspan="3" rowspan="2">(Port F)
8-bit port. Lower 4 bits are for inputs; upper 4 bits are for outputs.
Lower 4 bits also serve as standby release input pin.
(8 pins)</td></tr>
<tr><td>PF4/AN8
to
PF7/AN11</td><td>Output/Input</td></tr>
<tr><td>$\overline{\text{SCK0}}$</td><td>I/O</td><td colspan="4">Serial clock (CH0) I/O.</td></tr>
<tr><td>SO0</td><td>Ouput</td><td colspan="4">Serial data (CH0) output.</td></tr>
<tr><td>SI0</td><td>Input</td><td colspan="4">Serial data (CH0) input.</td></tr>
<tr><td>$\overline{\text{CS0}}$</td><td>Input</td><td colspan="4">Serial chip select (CH0) input.</td></tr>
</table>

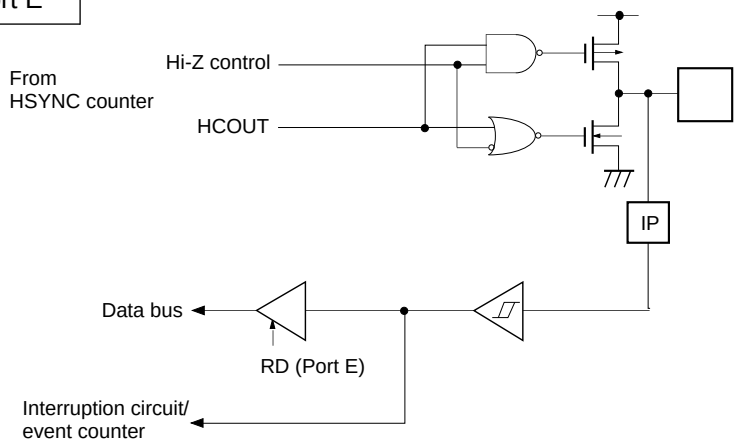
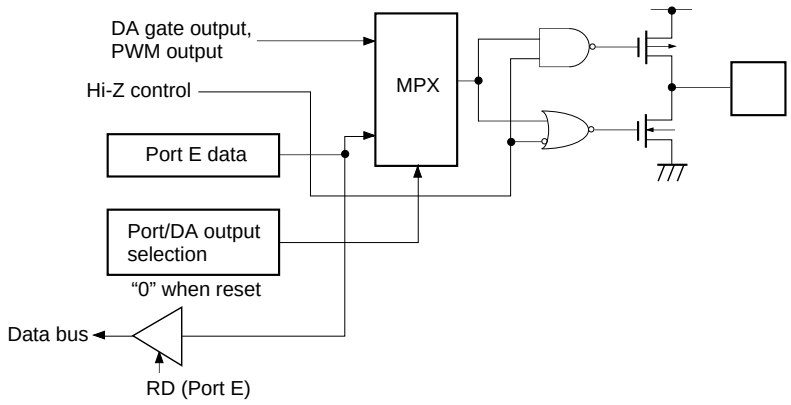
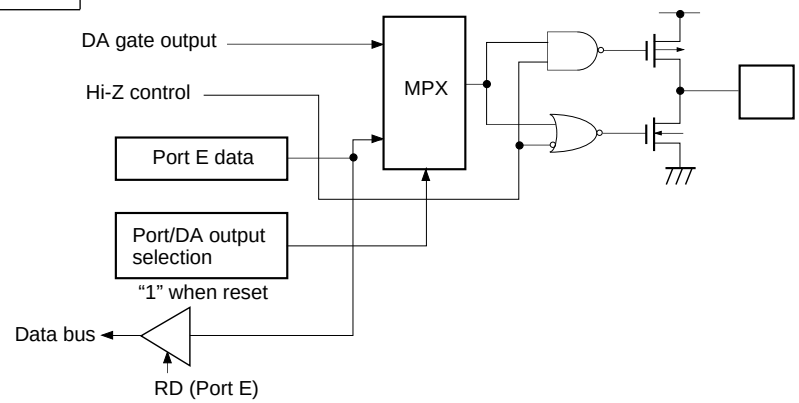
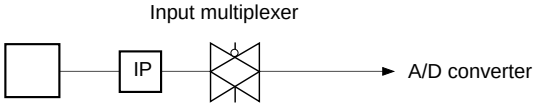
Symbol	I/O	Description	
PG0/CFG	Input/Input	(Port G) 8-bit input port. (8 pins)	Capstan FG input.
PG1/DFG	Input/Input		Drum FG input.
PG2/DPG	Input/Input		Drum PG input.
PG3/$\overline{\text{PBCTL}}$	Input/Input		Playback CTL pulse input. External event input for timer/counter.
PG4/SYNC0	Input/Input		Composite sync signal input. (2 pins)
PG5/SYNC1	Input/Input		
PG6/EXI0	Input/Input		External input to FRC capture unit. (2 pins)
PG7/EXI1	Input/Input		
PH0 to PH7	Output	(Port H) 8-bit output port ; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	
PI1/RMC	I/O/Input	(Port I) 7-bit I/O port. I/O port can be set in a unit of single bits. (7 pins)	Remote control reception circuit input.
PI2/$\overline{\text{PWM}}$	I/O/Output		14-bit PWM output.
PI3/TO/ DDO/ADJ	I/O/Output/ Output/Output		Timer/counter, CTL duty detection, 32kHz oscillation adjustment output.
PI4/$\overline{\text{INT1}}$/ $\overline{\text{NMI}}$	I/O/Input/Input		Input to request external interruption and non-maskable interruption. Active at the falling edge.
PI5/$\overline{\text{SCK1}}$	I/O/I/O		Serial clock (CH1) I/O.
PI6/SO1	I/O/Output		Serial data (CH1) output.
PI7/SI1	I/O/Input		Serial data (CH1) input.
PJ0 to PJ7	I/O	(Port J) 8-bit I/O port. I/O and standby release input function can be set in a unit of single bits.	
EXTAL	Input	Connects a crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL and input the opposite phase clock to XTAL.	
XTAL	Output		
TEX	Input	Connects a crystal oscillator for 32kHz timer/counter clock. The 32kHz crystal oscillator is inserted between TEX and TX. When used as event counter, connect the clock source to TEX and leave TX open.	
TX	Output		
$\overline{\text{RST}}$	Input	System reset; active at Low level.	
MP	Input	Test mode input. Always connect to GND.	
AV_{DD}		Positive power supply of A/D converter.	
AV_{REF}	Input	Reference voltage input of A/D converter.	
AVss		GND of A/D converter.	
V_{DD}		Positive power supply. Connect V_{DD} pin to V_{DD}.	
Vpp		Positive power supply for incorporated PROM writing. In normal operation, connect to V_{DD}.	
Vss		GND. Connect both Vss pins to GND.	

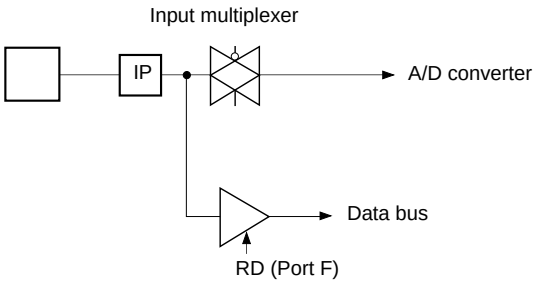
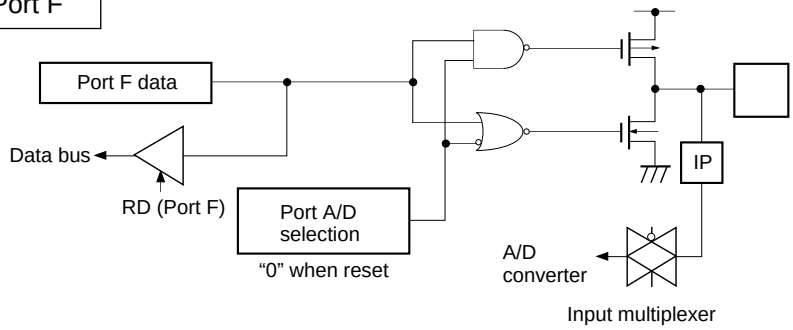
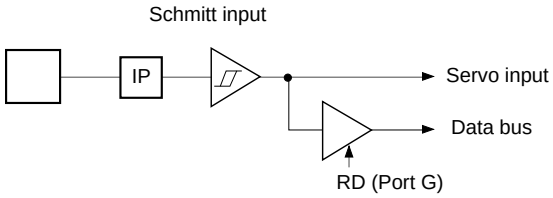
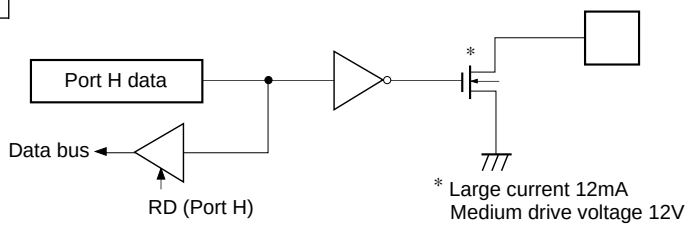
Input/Output Circuit Formats for Pins

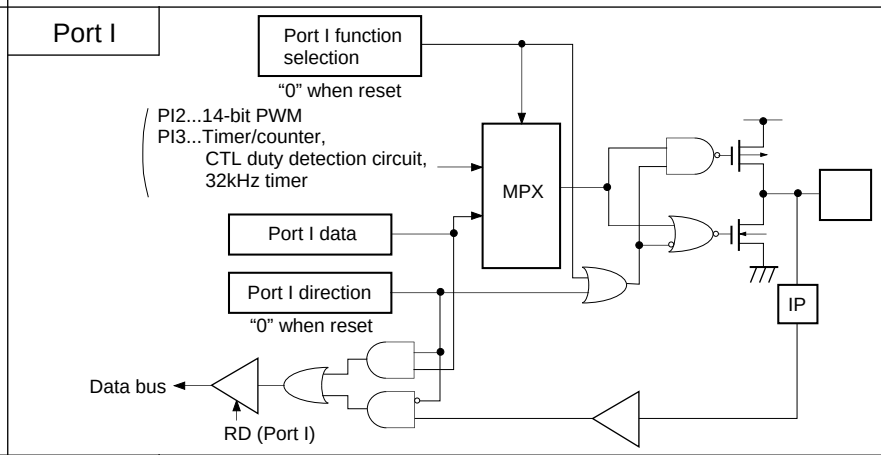
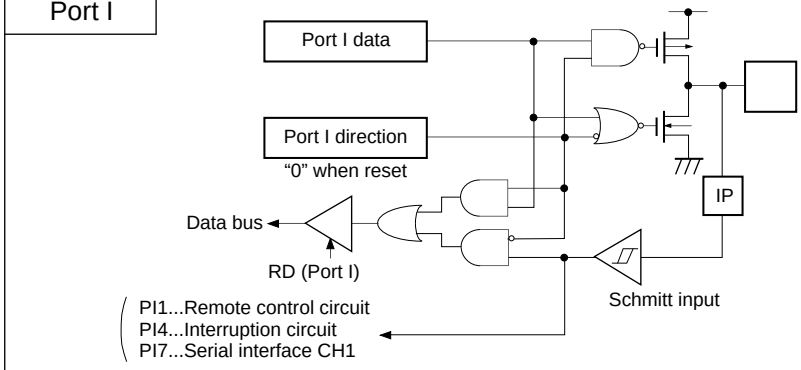
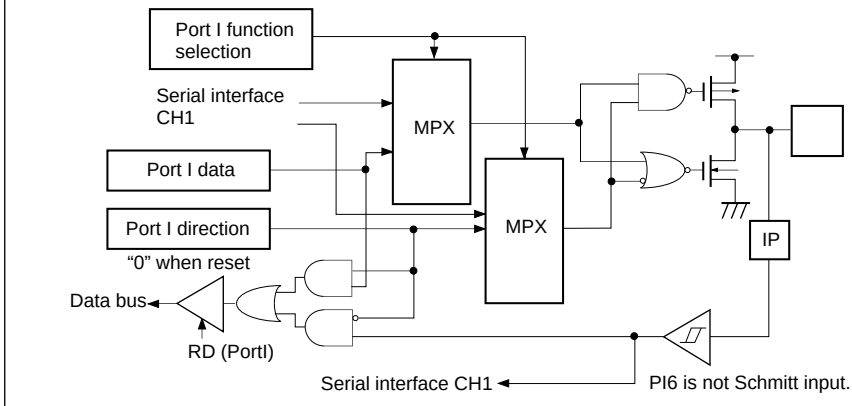
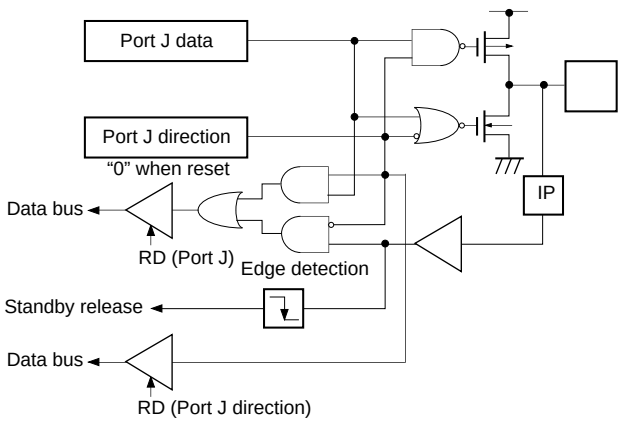
Pin	Circuit format	When reset
PA0 /PPO0 to PA7/PPO7 PB4/PPO12 to PB7/PPO15 12 pins	Port A Port B 	Hi-Z
PB0 /PPO8 PB2/PPO10 2 pins		Hi-Z
PB1/PPO9 PB3/PPO11 2 pins		Hi-Z

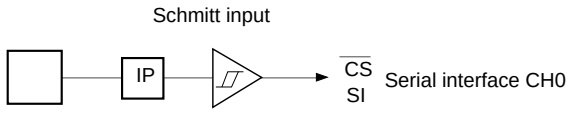
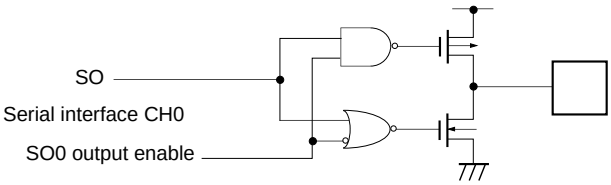
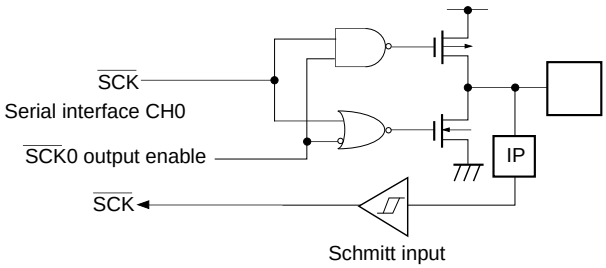
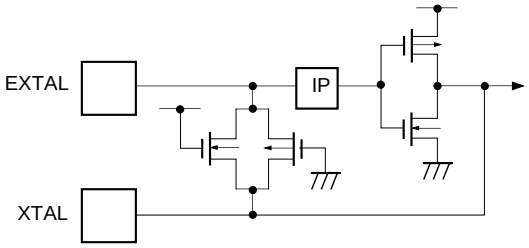
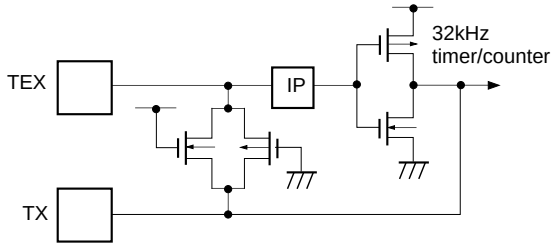
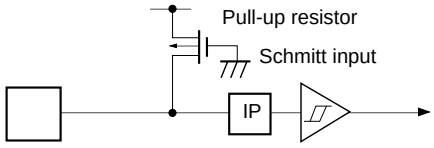
Pin	Circuit format	When reset
PC0/PPO16 to PC2/PPO18 PC5/RTO5 to PC7/RTO7 6 pins	Port C 	Hi-Z
PC3/RTO3 1 pin		Hi-Z
PC4/RTO4 1 pin	 RTO data is OR-gate data of CH0 and CH1.	Hi-Z

Pin	Circuit format	When reset
PD0/SCL0 PD1/SCL1 PD2/SDA0 PD3/SDA1 4 pins	Port D 	Hi-Z
PD4 to PD7 4 pins	Port D 	Hi-Z
PE0/$\overline{\text{INT0}}$/ CKOUT 1 pin	Port E 	Hi-Z

Pin	Circuit format	When reset
PE1/$\overline{EC}$/$\overline{INT2}$ /HCOUT 1 pin	Port E 	Hi-Z
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E 	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E 	High level
AN0 to AN3 4 pins		Hi-Z

Pin	Circuit format	When reset
PF0/AN4 to PF3/AN7 4 pins	Port F 	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	Port F 	Hi-Z
PG0/CFG PG1/DFG PG2/$\overline{\text{DPG}}$ PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G  Note) For PG4 and PG5 input format, there is TTL Schmitt input with product.	Hi-Z
PH0 to PH7 8 pins	Port H 	Hi-Z

Pin	Circuit format	When reset
PI2/$\overline{\text{PWM}}$ PI3/TO/ DDO/ADJ 2 pins	Port I 	Hi-Z
PI1/RMC PI4/$\overline{\text{INT1}}$/$\overline{\text{NMI}}$ PI7/SI1 3 pins	Port I 	Hi-Z
PI5/$\overline{\text{SCK1}}$ PI6/SO1 2 pins	Port I 	Hi-Z
PJ0 to PJ7 8 pins	Port J 	Hi-Z

Pin	Circuit format	When reset
$\overline{CS0}$ SI0 2 pins		Hi-Z
SO0 1 pin		Hi-Z
$\overline{SCK0}$ 1 pin		Hi-Z
EXTAL XTAL 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode.	Oscillation
TEX TX 2 pins	 • Shows the circuit composition during oscillation. • Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time TEX pin outputs Low level and TX pin outputs High level.	Oscillation
$\overline{RST}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13	V	Incorporated PROM
	AV_{DD}	AVss to +7.0*1	V	
	AV_{SS}	–0.3 to +0.3	V	
Input voltage	V_{IN}	–0.3 to +7.0*2	V	
Output voltage	V_{OUT}	–0.3 to +7.0*2	V	
Medium drive output voltage	V_{OUTP}	–0.3 to +15.0	V	Port H pin
High level output current	I_{OH}	–5	mA	
High level total output current	$\sum I_{OH}$	–50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Ports excluding large current output (value per pin)
	I_{OLC}	20	mA	Large current output port (value per pin*3)
Low level total output current	$\sum I_{OL}$	130	mA	Total of output pins
Operating temperature	Topr	–10 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP

*1 AV_{DD} should not exceed V_{DD} + 0.3V.

*2 V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*3 The large current drive transistors are the N-CH transistors of the Port D (PD) and Port H (PH).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing modes
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing mode or during sleep mode
		2.7	5.5	V	Guaranteed operation range by TEX clock
		2.0	5.5	V	Guaranteed data hold range during stop mode
Analog supply voltage	AV_{DD}	4.5	5.5	V	*1
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	Includes the serial CH2 input*2
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	CMOS Schmitt input*3 and PE0/$\overline{INT0}$ pin
			5.5	V	CMOS Schmitt input*7
	V_{IHTS}	2.2	5.5	V	TTL Schmitt input*4
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL pin*5 and TEX pin*6
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	Includes the serial CH2 input*2
	V_{ILS}	0	$0.2V_{DD}$	V	CMOS Schmitt input*3 and PE0/$\overline{INT0}$ pin
	V_{ILTS}	0	0.8	V	TTL Schmitt input*4
	V_{ILEX}	–0.3	0.4	V	EXTAL pin*5 and TEX pin*6
Operating temperature	Topr	–10	+75	°C	

*1 AV_{DD} and V_{DD} should be set to the same voltage.

*2 Normal input port (PC, PD4 to PD7, PF0 to PF3, PG, PI and PJ), MP pin

*3 $\overline{SCK0}$, $\overline{RST}$, $\overline{EC}$/$\overline{INT2}$, RMC, $\overline{INT1}$/$\overline{NMI}$, $\overline{SCK1}$ and SI1

*4 PG4 and PG5 (When TTL Schmitt input is selected for the product)

*5 Specifies only when the external clock is input.

*6 Specifies only when the external event count clock is input.

*7 $\overline{CS0}$, SI0, and PG (For PG4 and PG5, when CMOS Schmitt input is selected for the product.)

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta = –10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PC, PD4 to PD7, PE2 to PE7, PF4 to PF7, PH (V_{OL} only) PI1 to PI7 PJ, SO0, $\overline{SCK0}$	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
		PD0 to PD3 (SCL0, SCL1 SDA0, SDA1)	V_{DD} = 4.5V, I_{OL} = 3.0mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 6.0mA			0.6	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$		–1.5		–400	µA
I/O leakage current	I_{IZ}	PA to PG, PI, PJ, MP $\overline{AN0}$ to $\overline{AN3}$, $\overline{CS0}$, SI0, SO0 $\overline{SCK0}$	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (in N-CH Tr off state)	I_{LOH}	PH	V_{DD} = 5.5V, V_{OH} = 12V			50	µA
		PD0 to PD3	V_{DD} = 5.5V, V_{OH} = 5.5V			10	µA
Serial interface CH2 bus switch connection impedance (in output Tr off state)	RBS	SCL0: SCL1 SDA0: SDA1	V_{DD} = 4.5V V_{SCL0} = V_{SCL1} = 2.25V V_{SDA0} = V_{SDA1} = 2.25V			120	Ω

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Supply current*1	I_{DD1}	V_{DD}	High-speed mode (1/2 frequency dividing clock) operation V_{DD} = 5V ± 0.5V		31	50	mA
	I_{DDS1}		Sleep mode V_{DD} = 5V ± 0.5V		2.3	8	mA
	I_{DD2}		32kHz crystal oscillation (C_1 = C_2 = 47pF) V_{DD} = 3V ± 0.3V		44	110	µA
	I_{DDS2}		Sleep mode V_{DD} = 3V ± 0.3V		9	35	µA
	I_{DDS3}		Stop mode (EXTAL and TEX pins oscillation stop) V_{DD} = 5V ± 0.5V			30	µA
Input capacity	C_{IN}	PC, PD, PE0, PE1, PF, PG, PI1 to PI7 PJ, $\overline{CS0}$, SI0, $\overline{SCK0}$, AN0 to AN3, EXTAL, XTAL, TEX, $\overline{TX}$, MP, $\overline{RST}$	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 When all output pins are open.

AC Characteristics

(1) Clock timing

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)	28			ns
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 (External clock drive)			200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	4tsys*1			ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ns
System clock frequency	f_C	TEX TX	Fig. 2 V_{DD} = 2.7 to 5.5V (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1 tsys indicates three values according to the contents of the clock control register (CLC; 00FE$_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Fig. 1. Clock timing

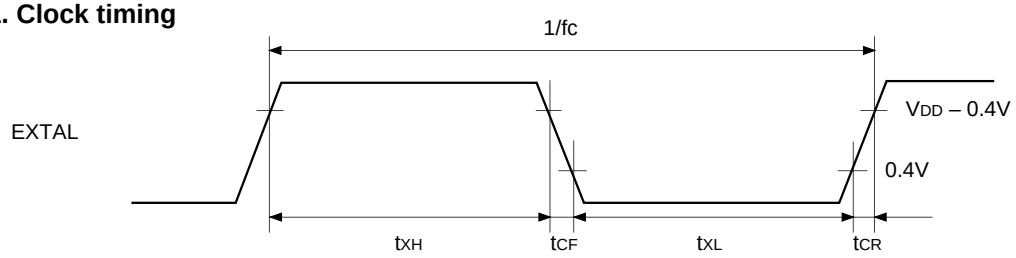


Fig. 2. Clock applied condition

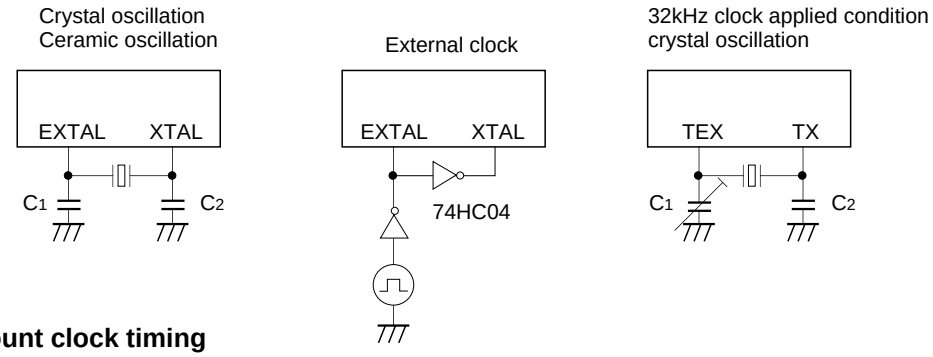
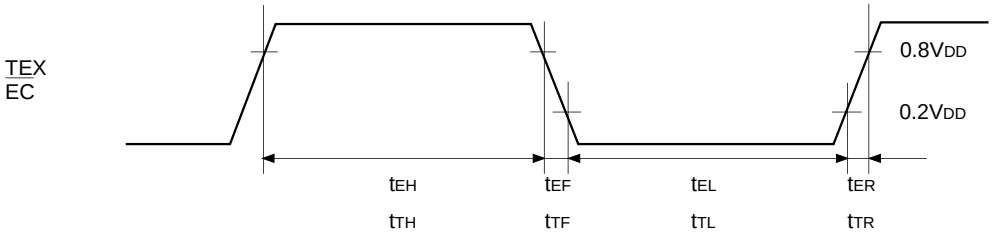


Fig. 3. Event count clock timing



(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

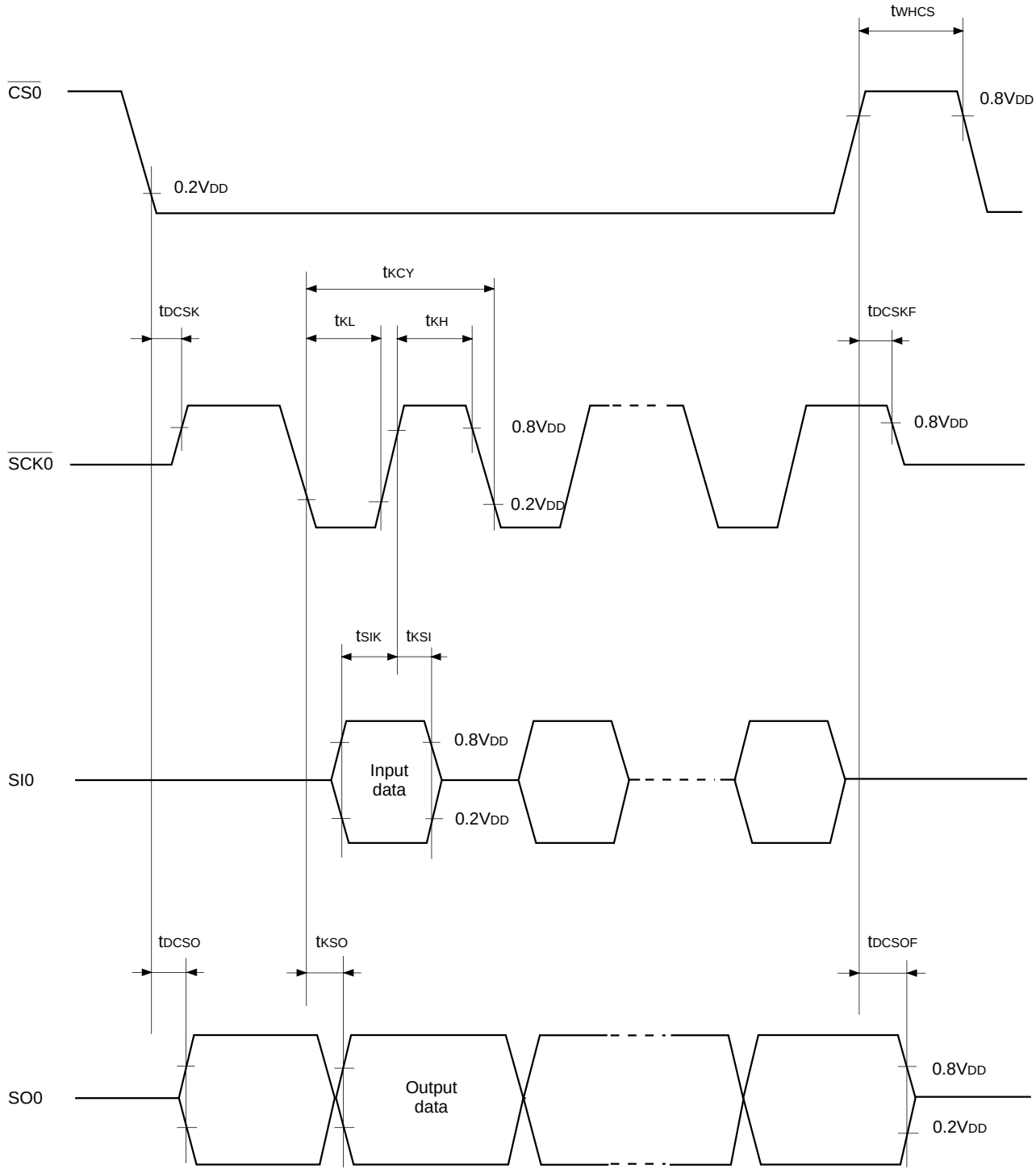
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS} \downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS} \downarrow \rightarrow$ SO floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: $00FE_H$) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Note 2) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing (CH0)



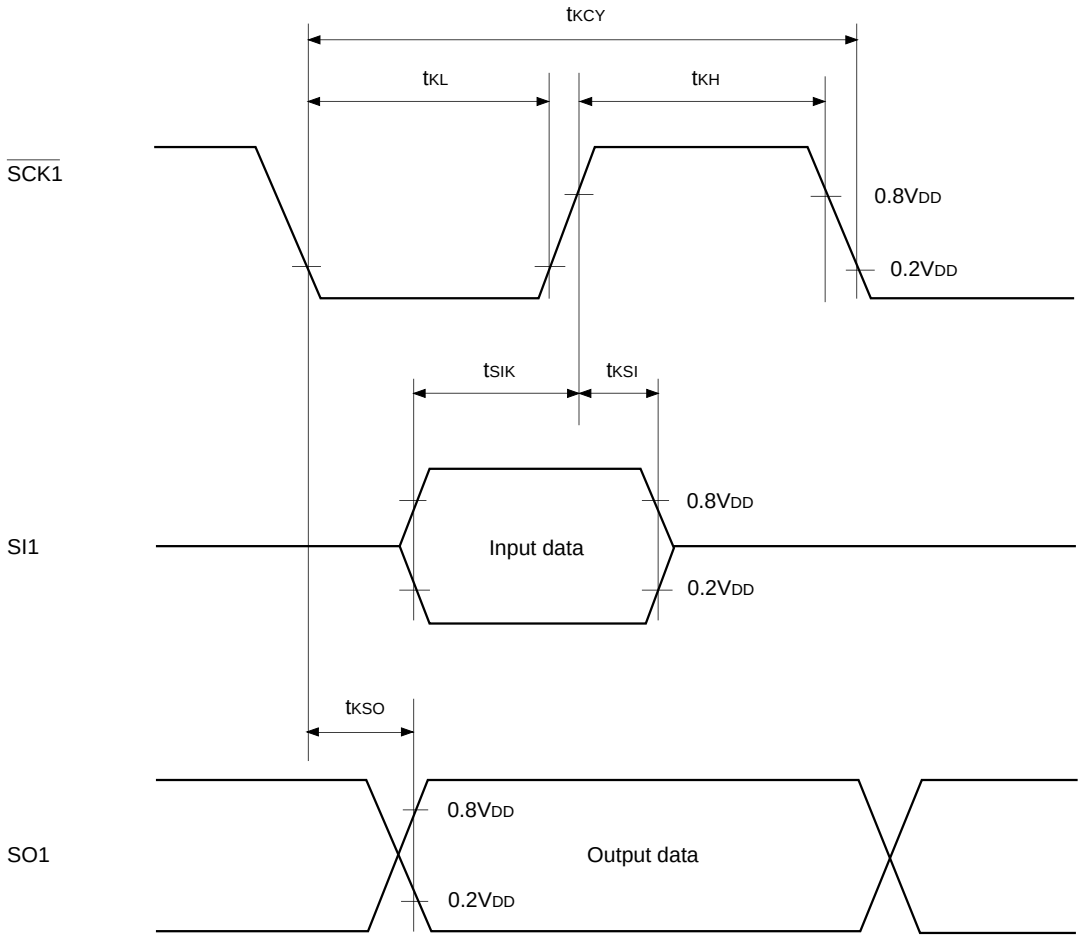
Serial transfer (CH1) (SIO mode) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK1}$ High and Low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI1 input setup time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ output mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	tsys + 200		ns
			$\overline{SCK1}$ output mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		tsys + 200	ns
			$\overline{SCK1}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (CLC: $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.

Fig. 5. Serial transfer CH1 timing (SIO mode)



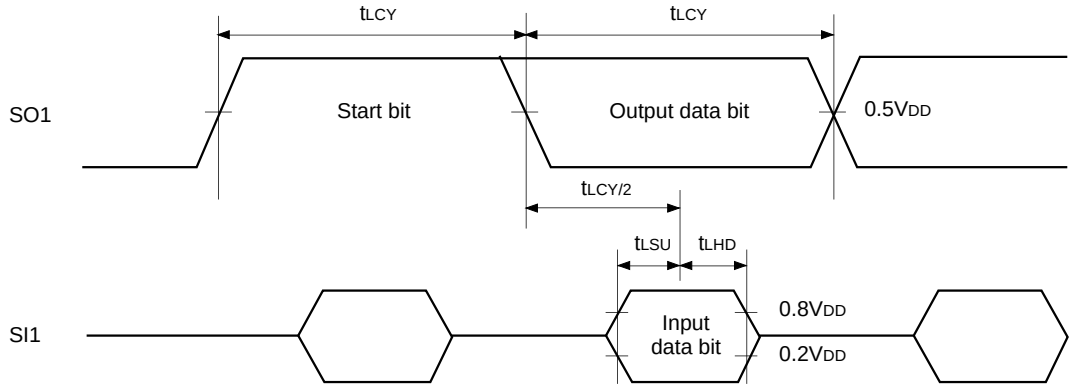
Serial transfer (CH1) (Special mode) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
SO1 cycle time	t_{LCY}	SO1 SI1	*1		104		µs
SI1 data setup time	t_{LSU}	SI1		2			µs
SI1 data hold time	t_{LHD}	SI1		2			µs

*1 t_{LCY} is specified only when serial mode register (CH1) (SIOM1: 05FZH) lower 2 bits (SO1 clock selection) has been set at 104µs.

Note) The load of SO1 pin is 50pF + 1TTL.

Fig. 6. Serial transfer CH1 timing (Special mode)



Serial transfer (CH2) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCL clock frequency	f_{SLC}	SCL			400	kHz
Bus-free time before starting transfer	t_{BUF}	SDA, SCL		2.6		µs
Hold time for starting transfer	$t_{HD;\,STA}$	SDA, SCL		1.0		µs
Clock Low level width	t_{LOW}	SCL		1.0		µs
Clock High level width	t_{HIGH}	SCL		1.0		µs
Setup time for repeated transfers	$t_{SU;\,STA}$	SDA, SCL		1.0		µs
Data hold time	$t_{HD;\,DAT}$	SDA, SCL		0*1		µs
Data setup time	$t_{SU;\,DAT}$	SDA, SCL		100		ns
SDA, SCL rise time	t_R	SDA, SCL			300	ns
SDA, SCL fall time	t_F	SDA, SCL			300	ns
Setup time for transfer completion	$t_{SU;\,STO}$	SDA, SCL		1.6		µs

*1 The SCL fall time (300ns Max.) is not included in the data hold time.

Fig. 7. Serial transfer timing (CH2)

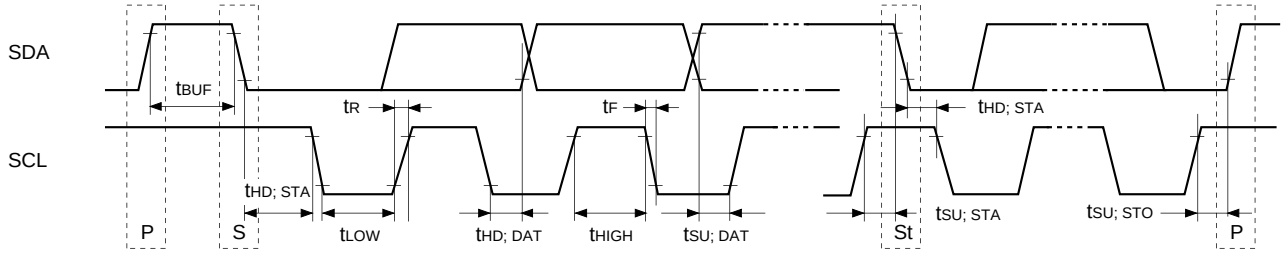
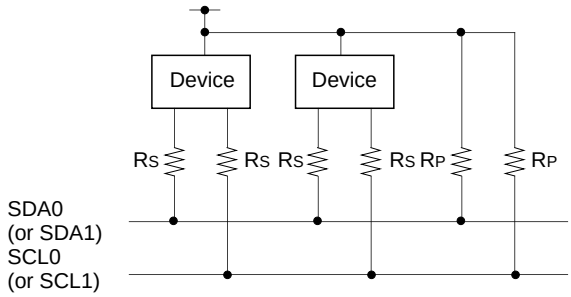


Fig. 8. Device recommended circuit



- A pull-up resistor (R_P) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be used to reduce the spike noise caused by CRT flashover.

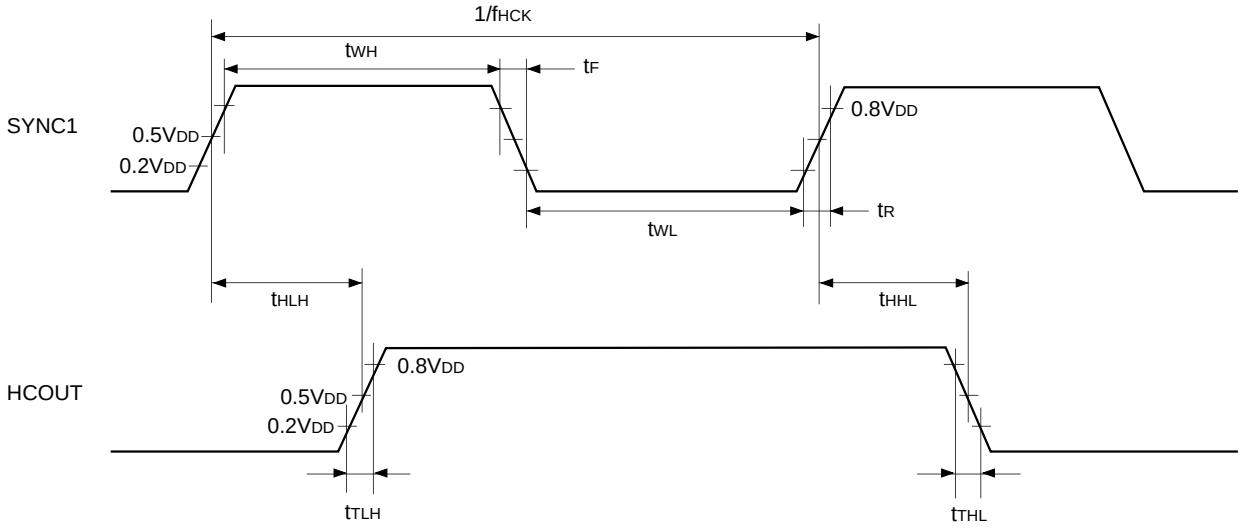
(3) HSYNC counter (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
External clock input frequency	f_{HCK}	SYNC1				12	MHz
External clock input pulse width	t_{WH}, t_{WL}	SYNC1		33			ns
External clock input rise and fall times	t_R, t_F	SYNC1				200	ns
HCOUT output delay time (for SYNC1 ↑)	t_{HLH}, t_{HHL}	HCOUT	External clock input SYNC1 $t_R = t_F$ = 6ns			tsys + 220	ns
HCOUT output rise and fall times	t_{TLH}	HCOUT	External clock input SYNC1 $t_R = t_F$ = 6ns			50	ns
	t_{THL}					25	ns

Note1) tsys indicates three values according to the contents of the clock control register (CLC: $00FE_H$) upper 2 bits (CPU clock selection).
tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11").

Note2) The load of HCOUT pin is 50pF.

Fig. 9. HSYNC counter timing

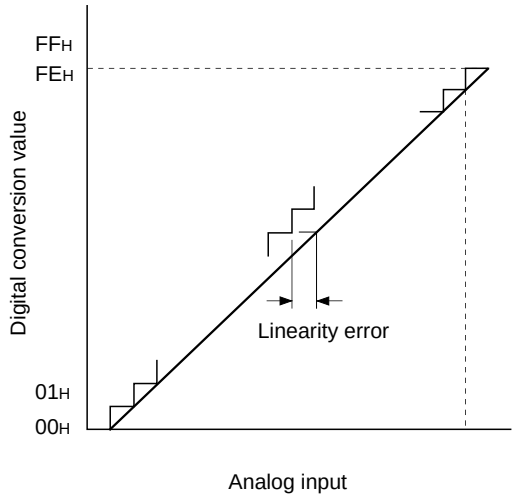


(4) A/D converter characteristics

(Ta = –10 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC}*1			µs
Sampling time	t_{SAMP}			12/f_{ADC}*1			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD} – 0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN11		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode 32kHz operating mode			10	µA

Fig. 10. Definitions of A/D converter terms



*1 f_{ADC} indicates the below values due to the ADC operation clock selection (PCC: 05F8H) bit 3 and clock control register (CLC: 00FEH) upper 2 bits.

PCC bit 3 / CLC upper 2 bits	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(5) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High and Low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$ PJ0 to PJ7		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 11. Interruption input timing

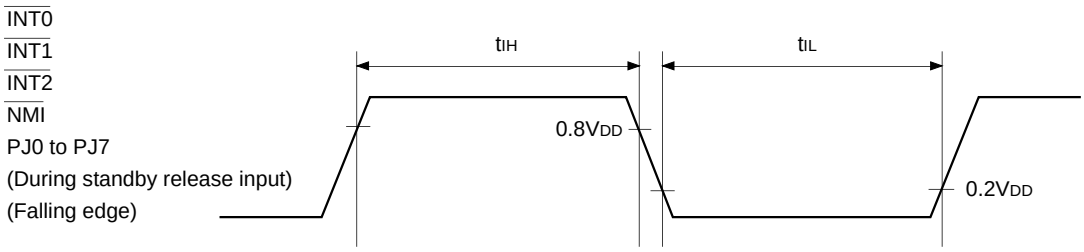
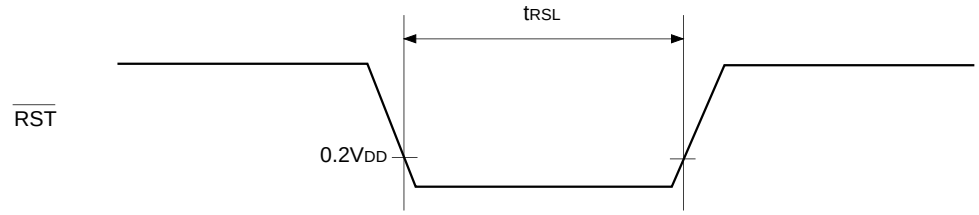


Fig. 12. Reset input timing



(6) Others (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

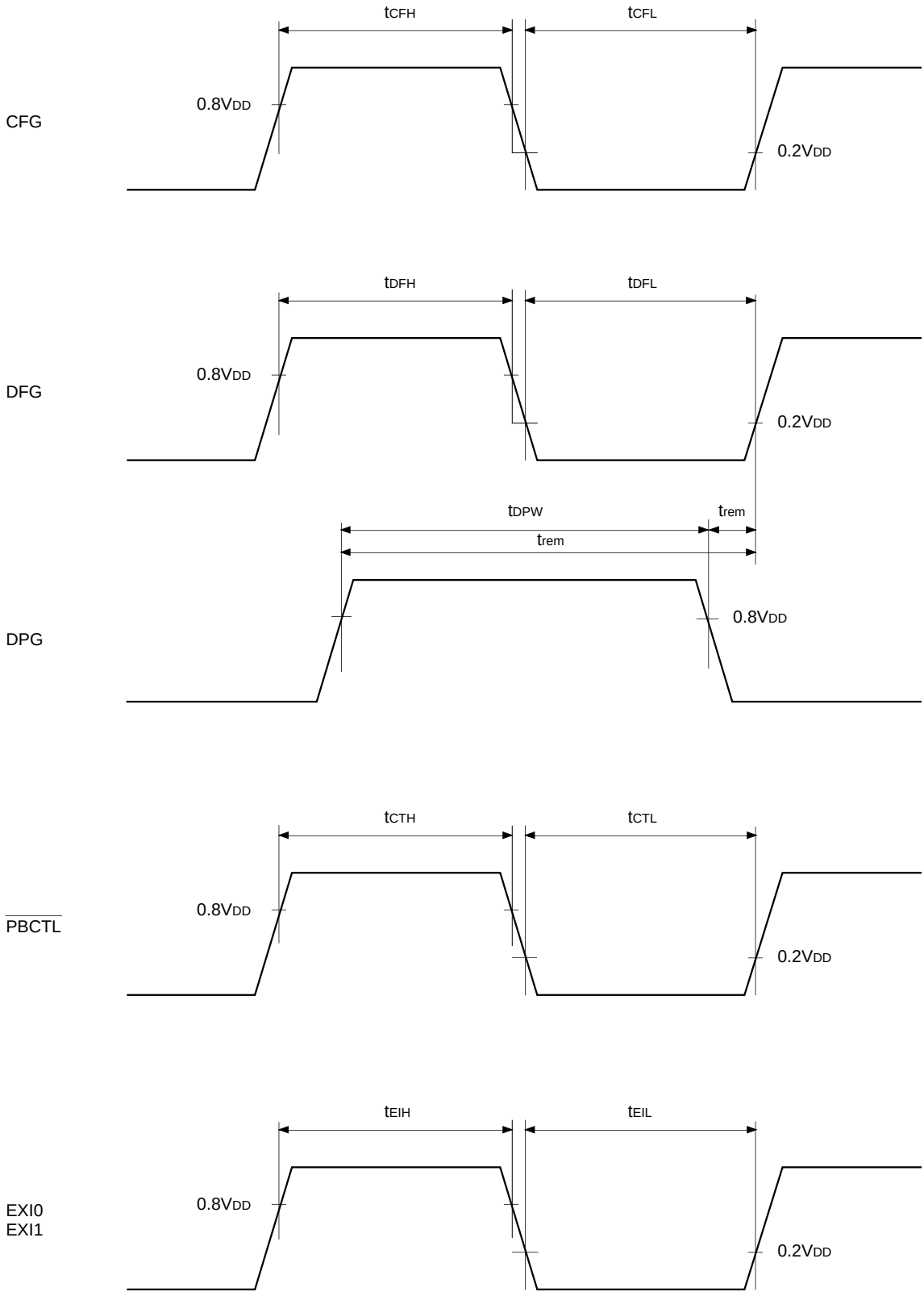
Item	Symbol	Pins	Conditions	Min.	Max.	Unit
CFG input High and Low level widths	t_{CFH} t_{CFL}	CFG		$24t_{FRC}$ + 200		ns
DFG input High and Low level widths	t_{DFH} t_{DFL}	DFG		$16t_{FRC}$ + 200		ns
DPG minimum pulse width	t_{DPW}	DPG		$8t_{FRC}$ + 200		ns
DPG minimum removal time	t_{rem}	DPG		$16t_{FRC}$ + 200		ns
$\overline{PBCTL}$ input High and Low level widths	t_{CTH} t_{CTL}	$\overline{PBCTL}$	tsys = 2000/fc	$8t_{FRC}$ + 200 + tsys		ns
EXI input High and Low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	tsys = 2000/fc	$8t_{FRC}$ + 200 + tsys		ns

Note 1) t_{FRC} = 1000/fc [ns]

Note 2) tsys indicates three values according to the contents of the clock control register (CLC: $00FE_H$) upper 2 bits (CPU clock selection).

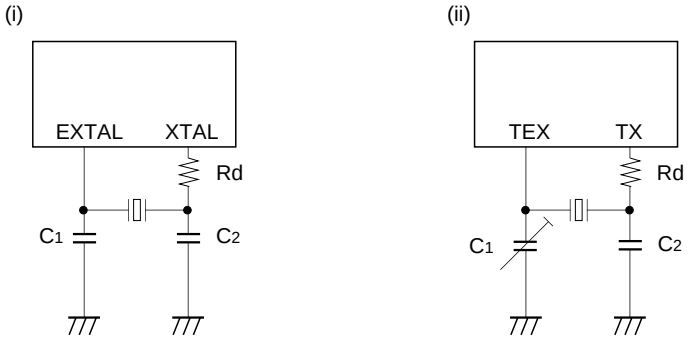
tsys [ns] = 2000/fc (Upper 2 bits = “00”), 4000/fc (Upper 2 bits = “01”), 16000/fc (Upper 2 bits = “11”)

Fig. 13. Other timings



Supplement

Fig. 14. Recommended oscillation circuit



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00	5	5		
		12.00				
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12	0	
	P3	32.768kHz	30	18	470k	(ii)

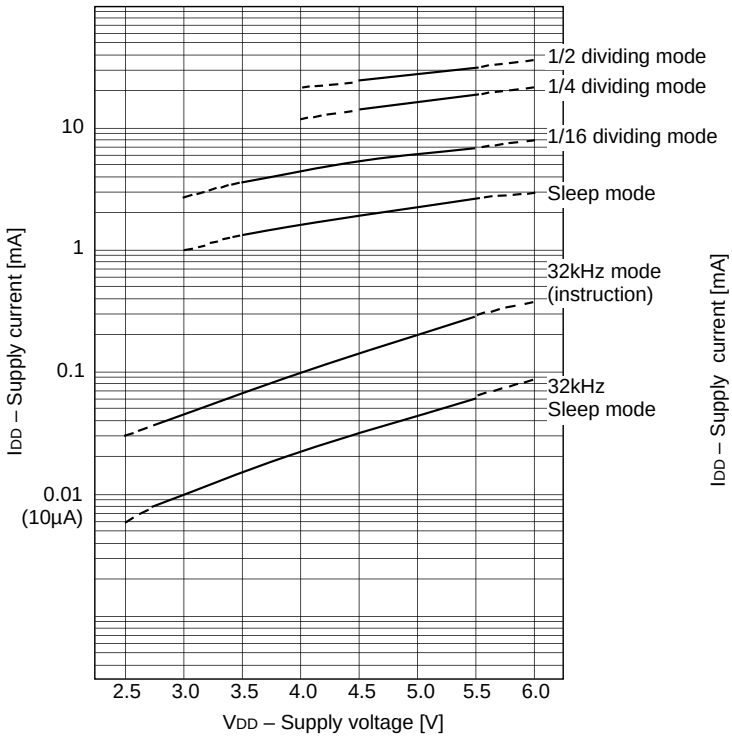
Selection Guide

Option item	Mask product	CXP878P60Q-1-□□□
Package	100-pin plastic QFP	100-pin plastic QFP
ROM capacitance	52K bytes /60K bytes	PROM 60K bytes
Reset pin pull-up resistor	Existent /Non-existent	Existent
Input circuit format*1	CMOS Schmitt /TTL Schmitt	TTL Schmitt

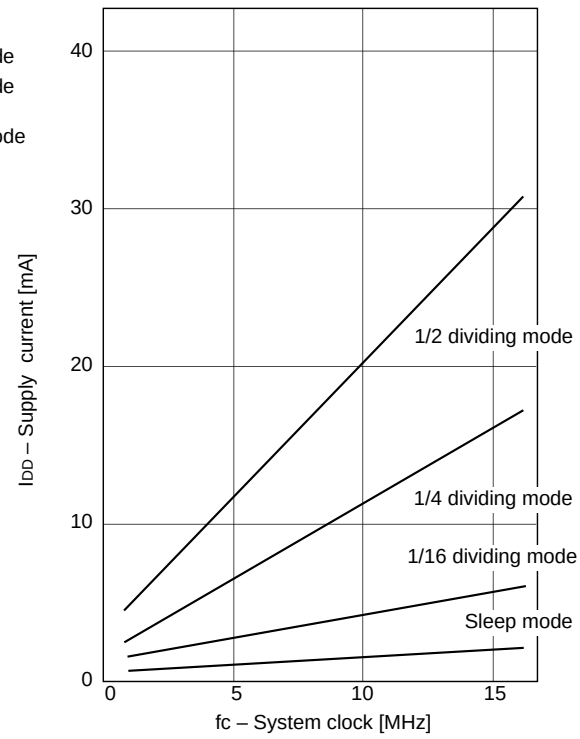
*1 Pins PG4/SYNC0, PG5/SYNC1 only.

Characteristics Curve

IDD vs. VDD
(fc = 16MHz, Ta = 25°C, Typical)

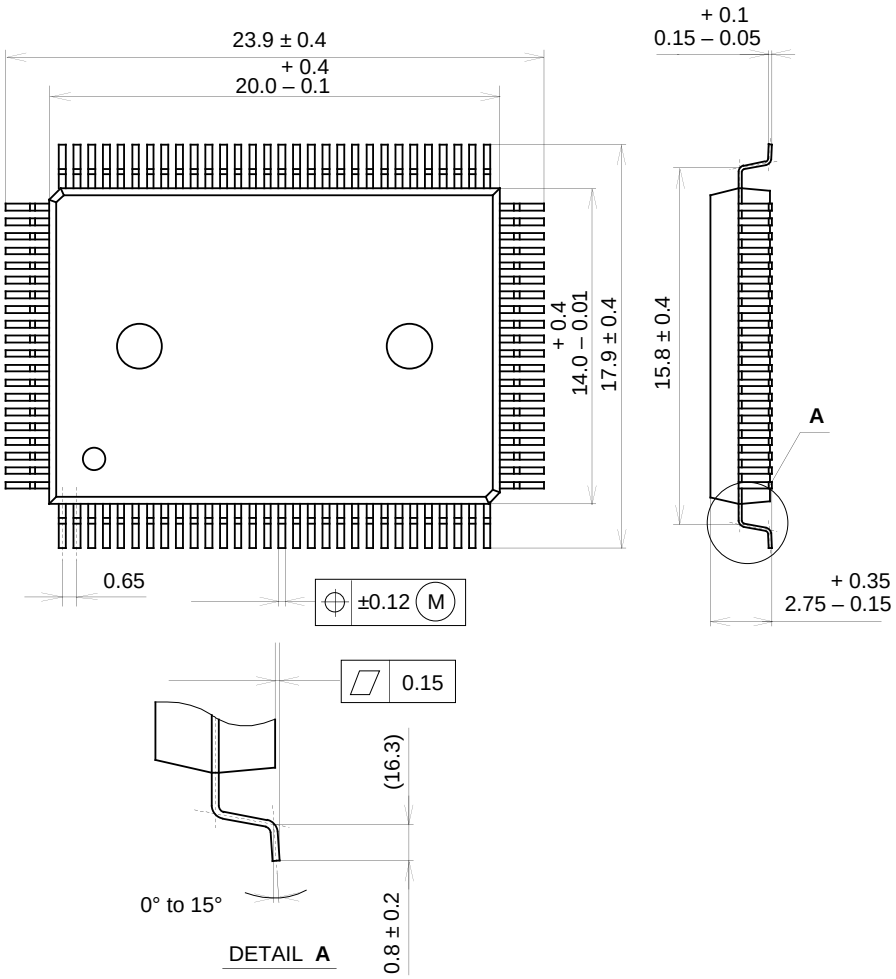


IDD vs. fc
(VDD = 5.0V, Ta = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	∗QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g