DUAL 2-INPUT NAND BUFFER/DRIVER

GENERAL DESCRIPTION

The MMC 40107 is a monolithic IC available in 14-lead dual in-line ceramic package and plastic package.
The MMC 40107 is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs.
This device features a wired-OR capability and high output sink current capability (136 mA typ at V_{DD} = 10 V, V_{DS} = 1 V).

FEATURES

- quiescent current specified to 20 V
- maximum input leakage of 1 μA at 18 V (full package temperature range)
- standardized symmetrical output characteristics
- 5 V, 10 V, and 15 V parametric ratings

APPLICATIONS

Driver circuits

ABSOLUTE MAXIMUM RATINGS

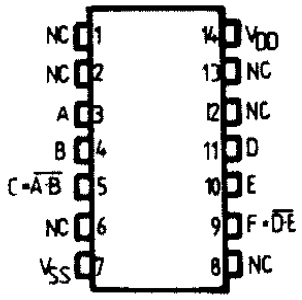
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_I	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_I	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature: G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

CONNECTION DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS

(over recommended* operating conditions)

PARAMETER		TEST CONDITIONS				VALUES							UNIT
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T^*_{LOW} min.	T^*_{LOW} max.	25°C min.	25°C typ	25°C max.	T^*_{HIGH} min.	T^*_{HIGH} max.	
I_L Quiescent current	G, H types	0/ 5			5		1		0.02	1		30	μA
		0/10			10		2		0.02	2		60	
		0/15			15		4		0.02	4		120	
		0/20			20		20		0.04	20		600	
	E, F types	0/ 5			5		4		0.02	4		30	
		0/10			10		8		0.02	8		60	
		0/15			15		16		0.02	16		120	
V_{IH}** Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/12.5	< 1	15	11		11			11		
V_{IL}** Input low voltage			4.5	< 1	5		1.5			1.5		1.5	V
			9	< 1	10		3			3		3	
			13.5	< 1	15		4			4		4	
I_{OL} Output sink current	G, H types	5	0.4		5	21		16	32		12		
		5	1		5	44		30	68		25		
		10	0.5		10	49		37	74		28		
		10	1		10	89		68	136		51		
		15	0.5		15	66		50	100		38		
	E, F types	5	0.4		5	17		13.6	32		12		
		5	1		5	35.7		25.5	68		22		
		10	0.5		10	39.1		31.4	74		27		
		10	1		10	72.2		57.8	136		51		
		15	0.5		15	53.5		42.5	100		37		
I_{OH} Output drive current		No internal pull-up device											mA
I_{IH}, I_{IL} Input leakage current	G, H types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		±1	μA
	E, F types	0/15			15		±0.3		$±10^{-5}$	±0.3		±1	
I_{OH}, I_{OL}*** 3-state output leakage current	G, H types	0/18	18		18		2		10^{-4}	2		20	μA
	E, F types	0/15	15		15		2		10^{-4}	2		20	
C_I Input capacitance		Any input							5	7.5			pF
C_O Output capacitance		Any output							30				

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.

* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V_{DD} = 5 V

2 V min. with V_{DD} = 10 V

2.5 V min. with V_{DD} = 15 V

** Measured with external pull-up resistor, R_L = 10 KΩ to V_{DD}

*** Forced output disabled

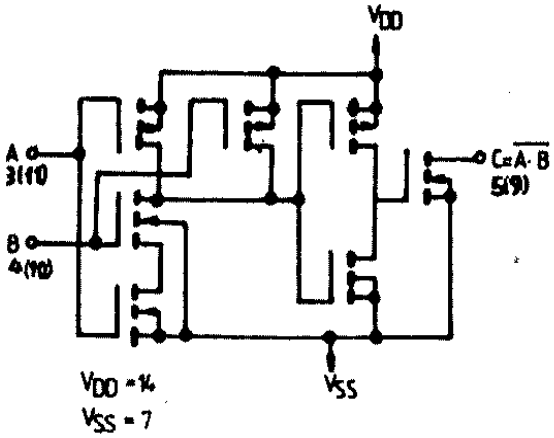
DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, C_L = 50 pF, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time 20 ns)

PARAMETER		TEST CONDITIONS		VALUES			UNIT
			V_{DD}(V)	min.	typ.	max.	
t_{PHL}, t_{PLH}	Propagation delay time High-to-Low	R_L*=120 Ω	5		100	200	ns
			10		45	90	
			15		30	60	
	Low-to-High	R_L*=120 Ω	5		100	200	ns
			10		60	120	
			15		50	100	
t_{THL}, t_{TLH}	Transition time High-to-Low	R_L*=120 Ω	5		50	100	ns
			10		20	40	
			15		10	20	
	Low-to-High	R_L*=120 Ω	5		50	100	ns
			10		35	70	
			15		25	50	

*R_L is external pull-up resistor to V_{DD}

SCHEMATIC DIAGRAM AND TRUTH TABLE



TRUTH TABLE

A	B	C	
0	0	1*	Z**
1	0	1*	Z**
0	1	1*	Z**
1	1	0	

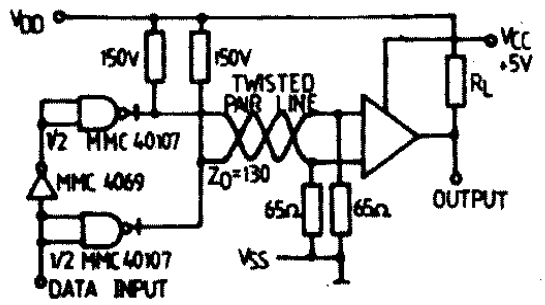
* Requires external pull-up resistor (R_L) to V_{DD}

** Without pull-up resistor (3-state)

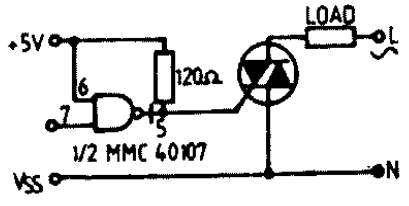
TYPICAL APPLICATIONS

The bar on the output line of this logic diagram indicates that the output is open drain as is shown in the previons schematic diagram and truth table.

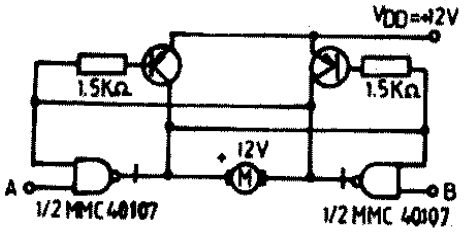
Line-driver circuit



Direct dc drive interface of 40107 with a triac

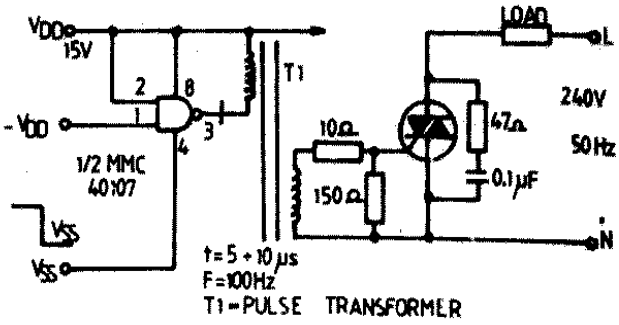


Motor-controller circuit

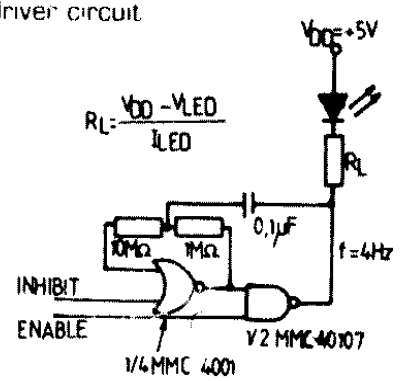


A	B	MOTOR FUNCTION
0	0	OFF
1	0	COUNTER CLOCKWISE
1	1	AS PREVIOUS STATE
0	1	CLOCKWISE
1	1	AS PREVIOUS STATE

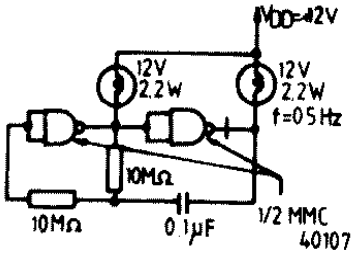
Interface of 40107 with triac whit COS/MOS component and triac isolated



LED driver circuit



A 22 watt incandescent lamp-driver circuit



INHIBIT	ENABLE	OUTPUT
0	0	OFF
1	0	OFF
0	1	OFF
1	1	ON

Multiplexed LED circuit