RF2456

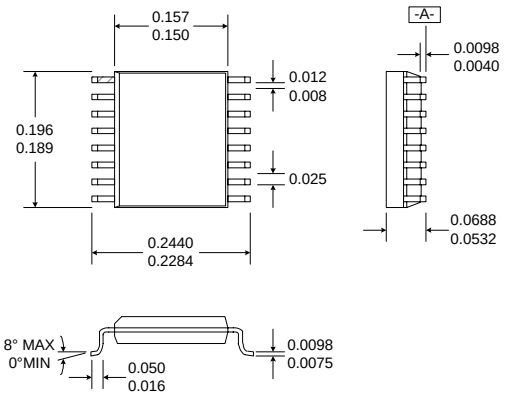
CDMA/FM DOWNCONVERTER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

Product Description

The RF2456 is a receiver dual downconverter designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to downconvert RF signals while providing 13dB gain in CDMA mode, and 7dB gain in FM mode. It also features digital control of IF output selection and power down mode. Noise Figure, IP3, and other specs are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. The IC is manufactured on an advanced Silicon Bipolar process and packaged in an SSOP-16.

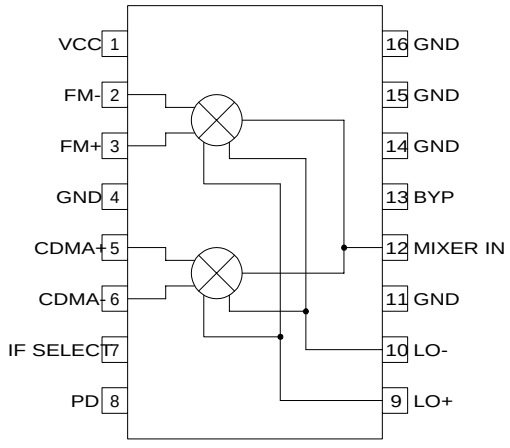


NOTES:
1. Shaded lead is Pin 1.
2. All dimensions are excluding mold flash.
3. Lead coplanarity - 0.005 with respect to datum "A".

Package Style: SSOP-16

Optimum Technology Matching® Applied

- ☑ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Dual Mode CDMA/AMPS
- Dual Mode JCDMA/TACS
- Digitally Selectable IF Outputs
- 500MHz to 1100MHz Operation
- Power Down Mode

Ordering Information

RF2456	CDMA/FM Downconverter
RF2456 PCBA	Fully Assembled Evaluation Board

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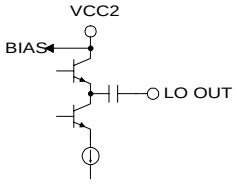
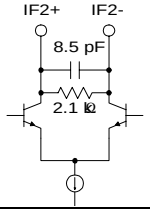
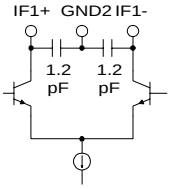
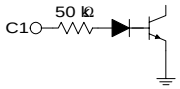
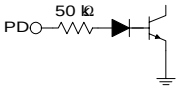
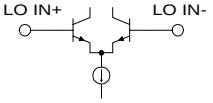
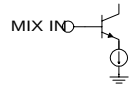
http://www.rfmd.com

Absolute Maximum Ratings

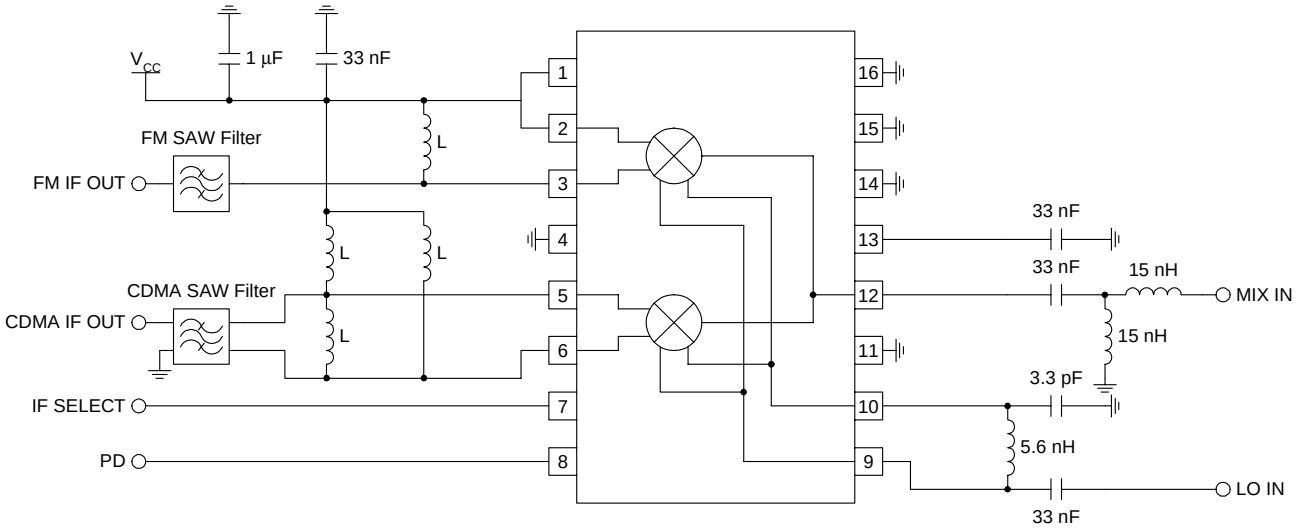
Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, RF=881MHz, LO=966MHz @ 0dBm, IF1= CDMA, IF2=FM
RF Frequency Range		200 to 1000		MHz	
LO Frequency Range		500 to 1100		MHz	
IF Frequency Range		0.1 to 250		MHz	
Conversion Gain	12.5	13.0		dB	IF1, 1kΩ balanced load.
	5	7		dB	IF2, 870Ω load.
Noise Figure		12		dB	IF1 single sideband.
		13		dB	IF2 single sideband
Input VSWR		<1.5:1			IF1 with external matching
		<2:1			IF2 with external matching
Input IP3	+3.0	+3.5		dBm	IF1
	+3.0	+10.0		dBm	IF2
Input P1dB		-7		dBm	IF1
		-4		dBm	IF2
MIX IN to IF1, IF2 Rejection		35		dB	
IF1, IF2 Output Freq. Range		70 to 100		MHz	With external IF interface network
Output Impedance		>1		kΩ	IF1, balanced, open collector
		870		Ω	IF2, single ended, with external inductor.
LO Input					
LO Input Range	-10	-3	0	dBm	
LO IN to RF Input Rejection		20		dB	
LO IN to IF1, IF2 Rejection		15		dB	
LO Input VSWR		<2:1			IF1 with external matching network
		2.5			IF2 with external matching network
Power Supply					
Voltage	2.7	3.0	4.0	V	
Current Consumption		18	21	mA	IF1 selected
		15	16	mA	IF2 selected
			5	µA	Power down (PD=0)

Pin	Function	Description	Interface Schematic
1	VCC	Supply Voltage for the mixers, bias circuits, and control logic. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
2	IF2-	Same as pin 3, except complimentary output. For typical single ended operation, this pin is connected directly to V_{CC}.	See pin 3.
3	IF2+	FM IF Output pin. This is a balanced output, but is typically used as a single-ended output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, is about 870Ω at 85MHz. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
4	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
5	IF 1+	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to V_{CC}, sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 85MHz is higher than 1kΩ, even though the part is designed to drive a 1kΩ load. Because this pin is biased to V_{CC}, a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	
6	IF 1-	Same as pin 5, except complementary output.	See pin 5.
7	IF SELECT	Control line for IF out select. A logic “low” enables the FM output. A logic “high” enables the CDMA output. The threshold voltage is 1.6V, and the pin draws less than 50μA when selected.	
8	PD	Power down pin. A logic “low” turns the part off. A logic “high” (>1.6V) turns the part on. In addition, pin 7 (IF SELECT) should also be taken low during power down.	
9	LO IN+	Mixer LO Balanced Input Pin. For single-ended input operation, this pin is used as an input and pin 10 is bypassed to ground.	
10	LO IN-	Same as pin 9 except complementary input.	See pin 9.
11	GND	Ground connection for the mixer. For best performance, keep traces physically short and connect immediately to ground plane.	
12	MIX IN	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	
13	BYP	Internal voltage reference. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
14	GND	Same as pin 4.	
15	GND	Same as pin 4.	
16	GND	Same as pin 4.	

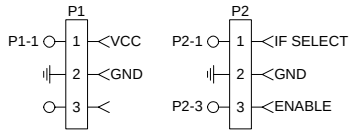
Application Schematic

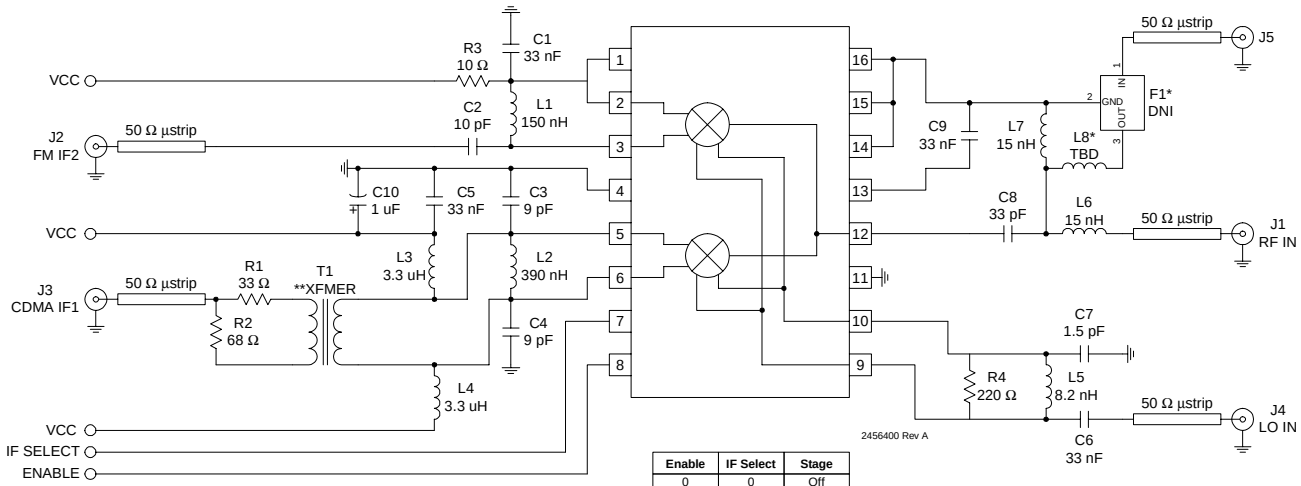


Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)

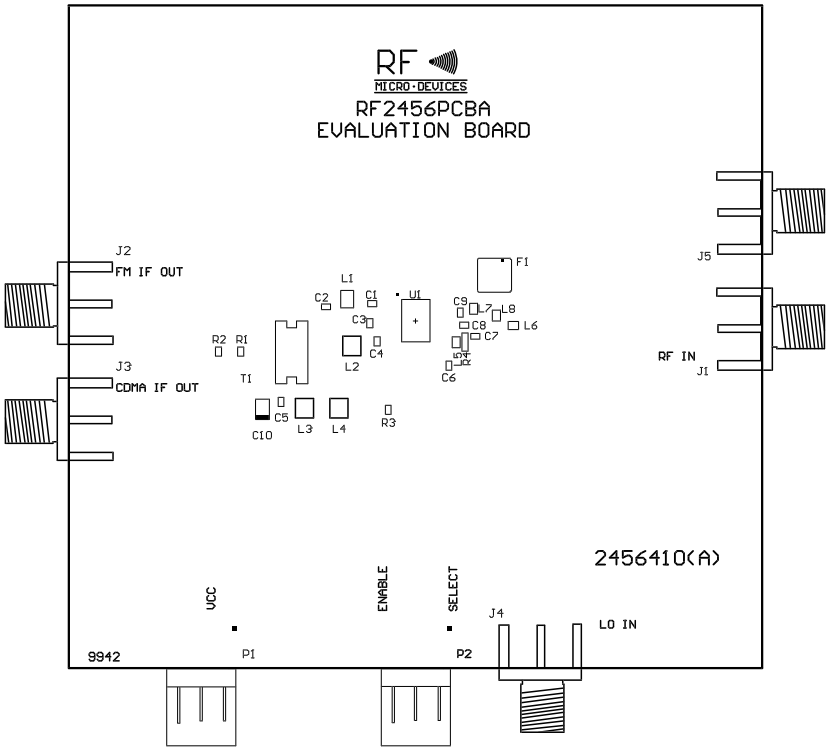
NOTE:
**Core: Fair-Rite Balun #2865002402
L12: 3 turns #30 AWG (Green)
L34: 12 turns #32 AWG (Red)
One turn = One pass through BOTH holes winding starts and finishes on same end of core.
L12 and L34 exit opposite ends of core.

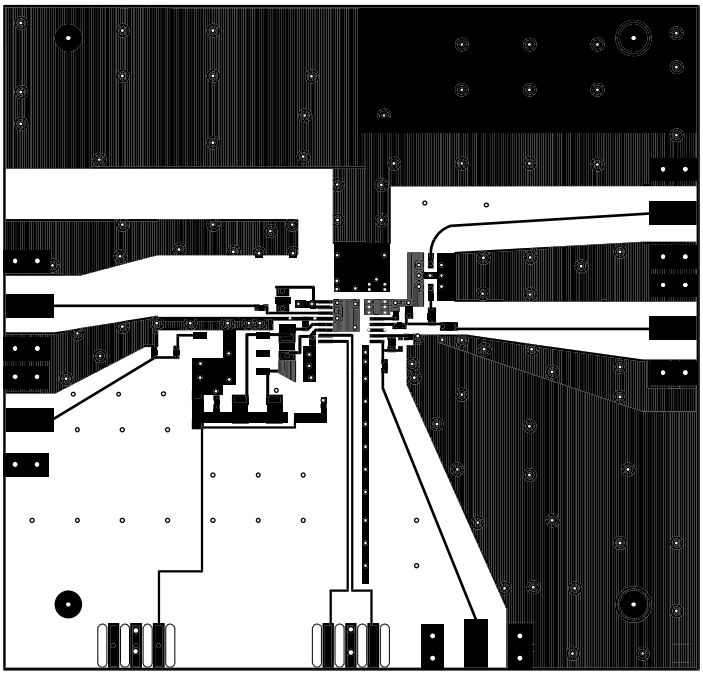


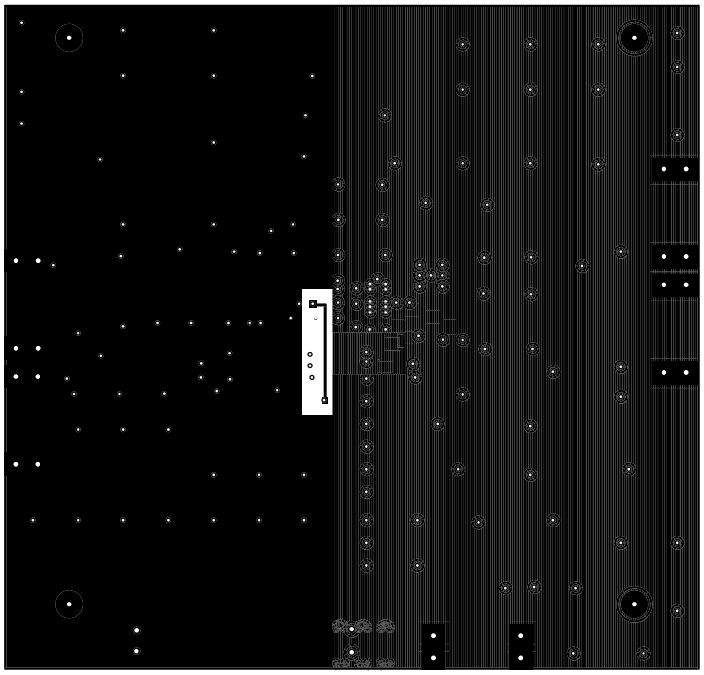


Enable	IF Select	Stage
0	0	Off
0	1	Off
1	0	FM
1	1	CDMA

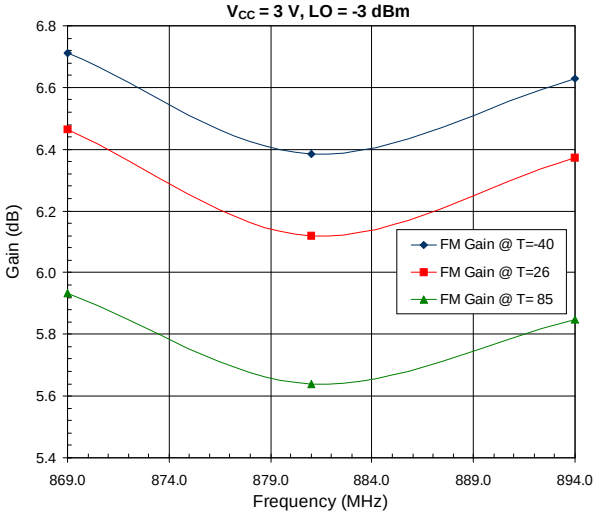
Evaluation Board Layout
Board Size 3.070" X 2.928"
Board Thickness 0.056", Board Material FR-4







FM Gain versus Temperature over Frequency,
V_{CC} = 3 V, LO = -3 dBm



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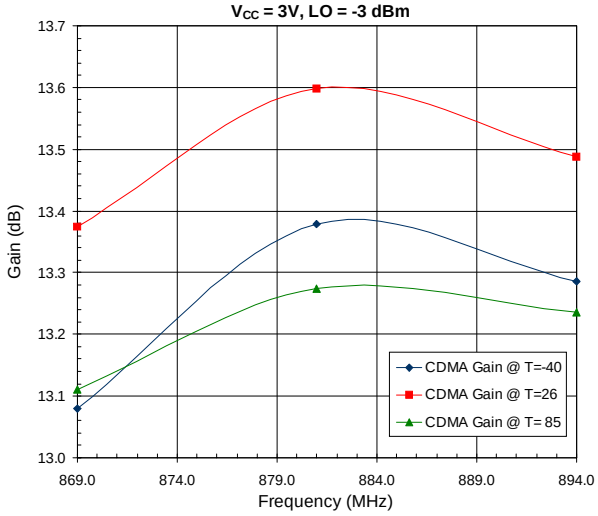
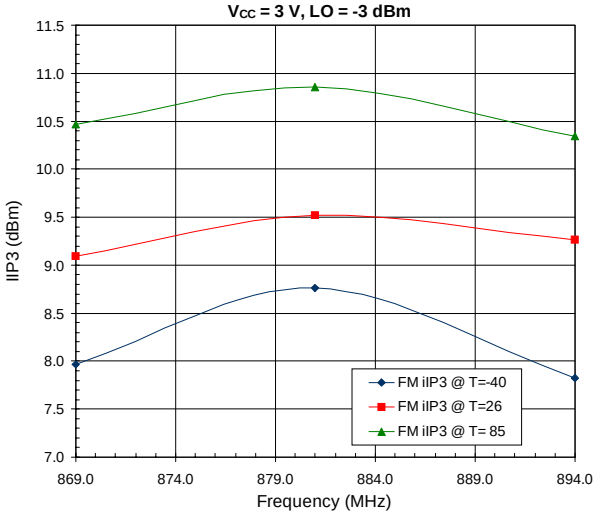
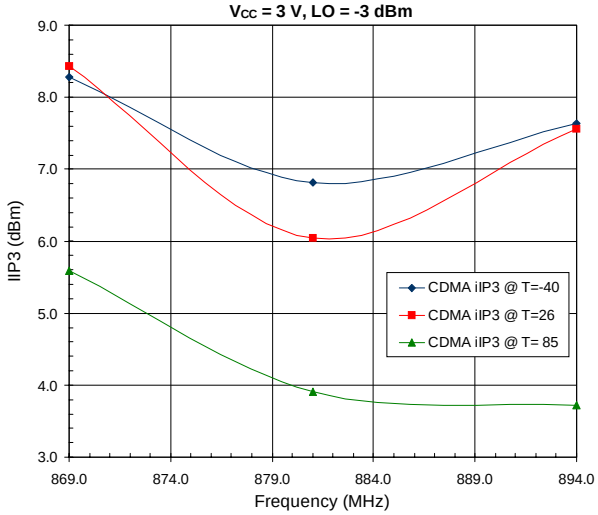


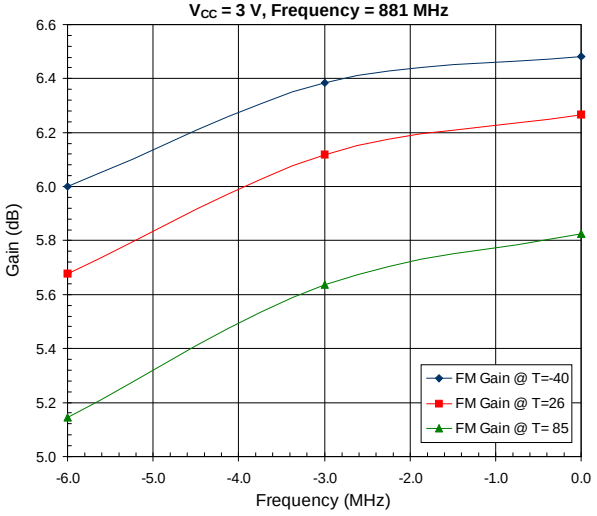
FM IIP3 versus Temperature over Frequency,
V_{CC} = 3 V, LO = -3 dBm



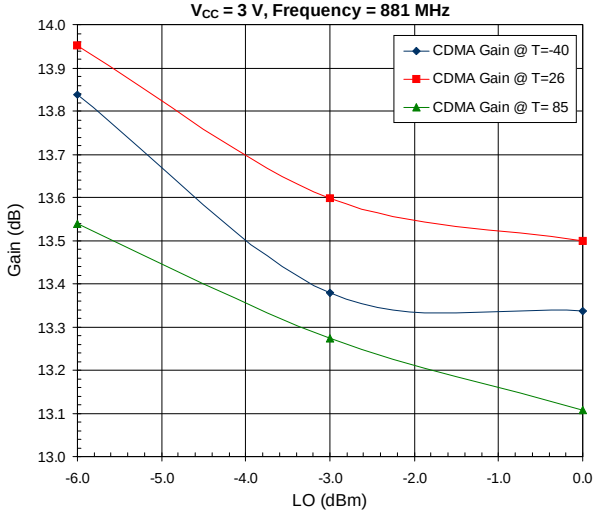
CDMA IIP3 versus Temperature over Frequency,
V_{CC} = 3 V, LO = -3 dBm



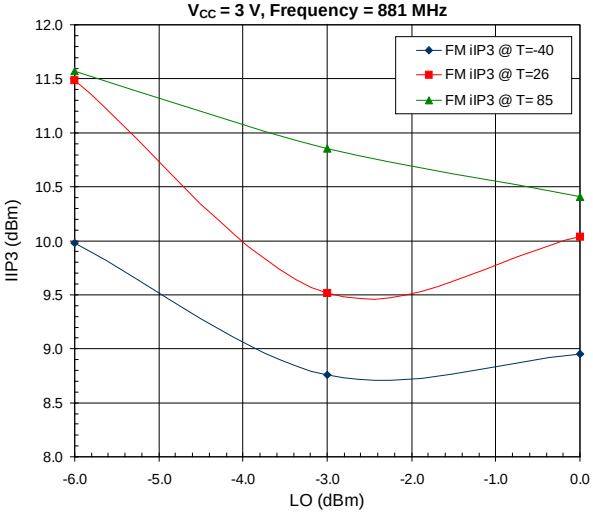
FM Gain versus Temperature over LO,
V_{CC} = 3 V, Frequency = 881 MHz



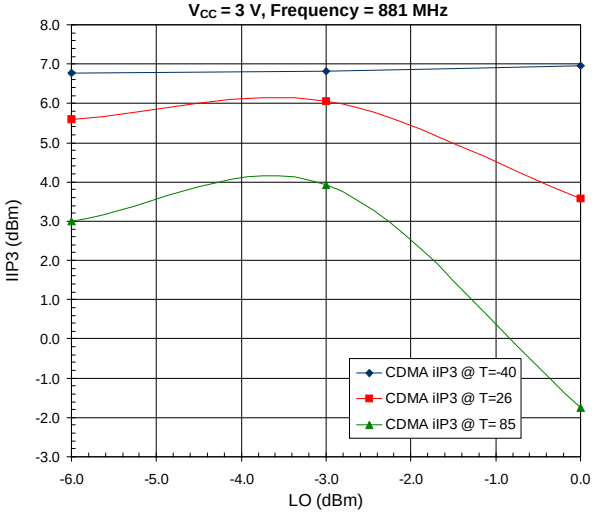
CDMA Gain versus Temperature over LO,
V_{CC} = 3 V, Frequency = 881 MHz



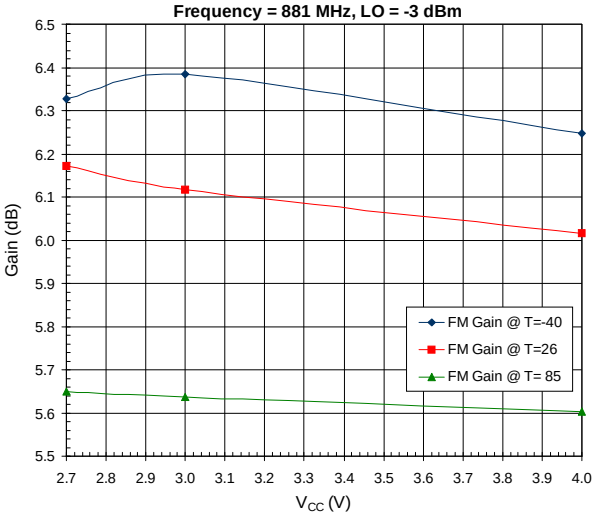
FM IIP3 versus Temperature over LO,
V_{CC} = 3 V, Frequency = 881 MHz



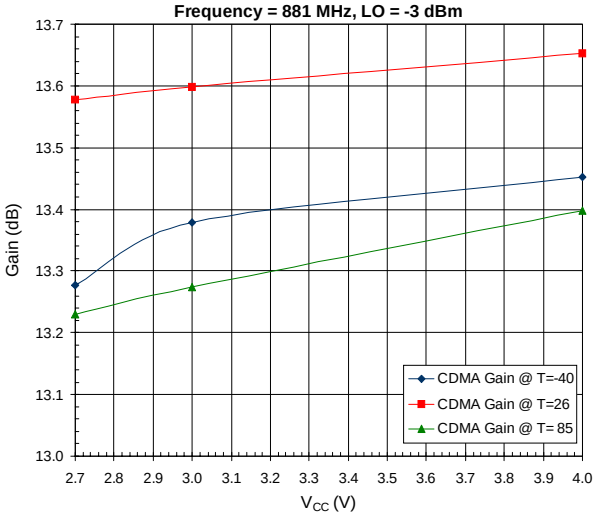
CDMA IIP3 versus Temperature over LO,
V_{CC} = 3 V, Frequency = 881 MHz



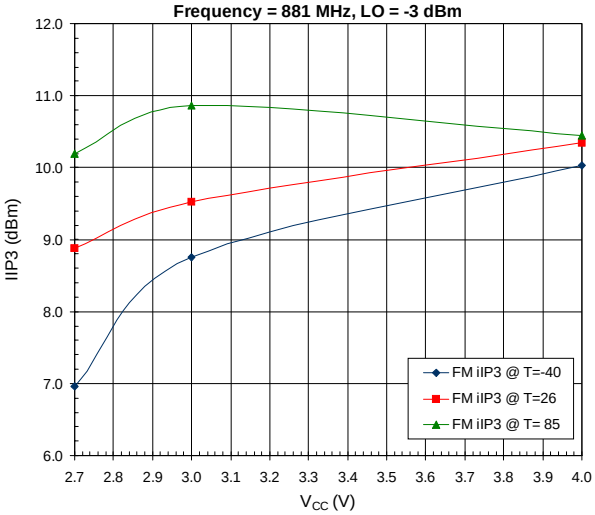
FM Gain versus Temperature over V_{CC},
Frequency = 881 MHz, LO = -3 dBm



CDMA Gain versus Temperature over V_{CC},
Frequency = 881 MHz, LO = -3 dBm



FM IIP3 versus Temperature over V_{CC},
Frequency = 881 MHz, LO = -3 dBm



CDMA IIP3 versus Temperature over V_{CC},
Frequency = 881 MHz, LO = -3 dBm