TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T C 7 M E T 5 7 4 A F K

Octal D-Type Flip-Flop with 3-State Output

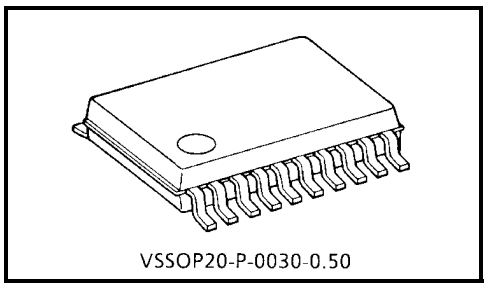
The TC7MET574AFK is an advanced high speed CMOS octal flip-flop with 3-state output fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent bipolar schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The input voltage are compatible with TTL output voltage.



Weight: 0.016 g (typ.)

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

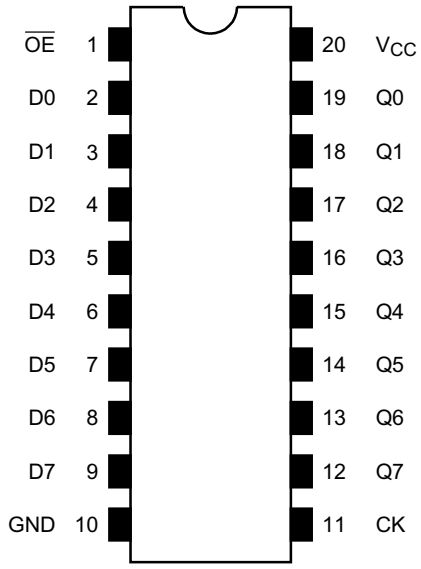
Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (*) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

*: output in off state

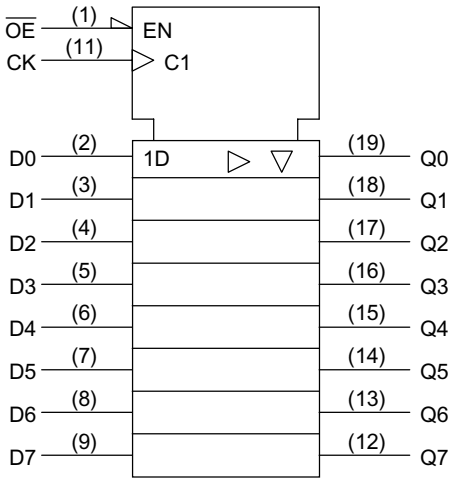
Features

- High speed: f_{max} = 140 MHz (typ.) (V_{CC} = 5 V)
- Low power dissipation: I_{CC} = 4 μA (max) (Ta = 25°C)
- Compatible with TTL outputs: V_{IL} = 0.8 V (max)
  V_{IH} = 2.0 V (min)
- Power down protection is provided on all inputs and outputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Low noise: V_{OLP} = 1.5 V (max)
- Pin and function compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 574 type.

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

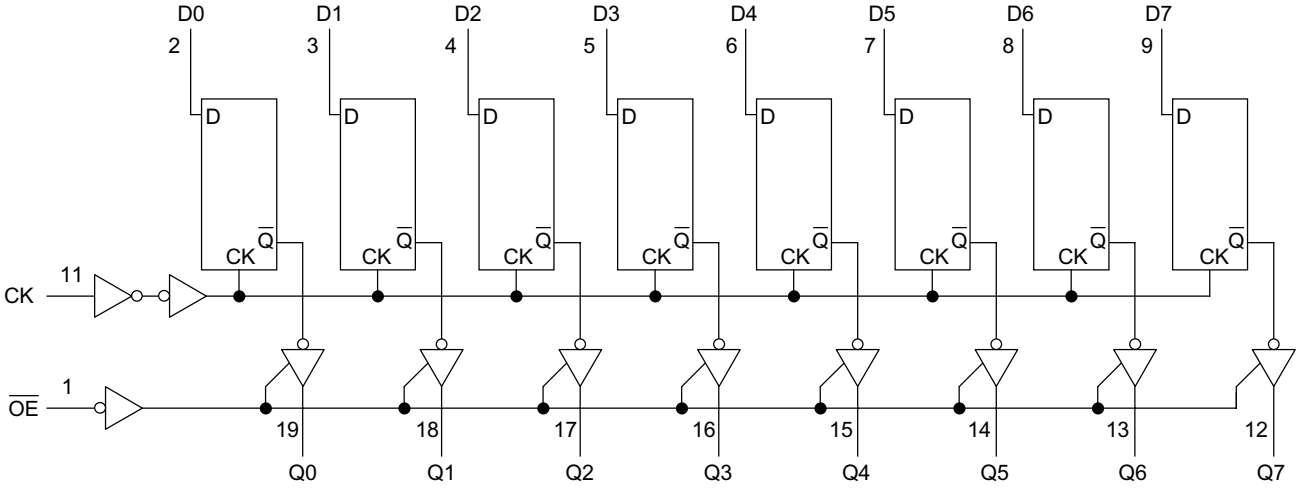
Inputs			Outputs
$\overline{OE}$	CK	D	
H	X	X	Z
L	↓	X	Q_n
L	↑	L	L
L	↑	H	H

X: Don't care

Z: High impedance

Q_n: No change

System Diagram



Maximum Ratings

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5~7.0	V
DC input voltage	V_{IN}	−0.5~7.0	V
DC output voltage	V_{OUT}	−0.5~7.0 (Note1)	V
		−0.5~V_{CC} + 0.5 (Note2)	
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20 (Note3)	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65~150	°C

Note1: Output is off-state

Note2: High or low state. I_{OUT} absolute maximum rating must be observed.

Note3: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5~5.5	V
Input voltage	V_{IN}	0~5.5	V
Output voltage	V_{OUT}	0~5.5 (Note4)	V
		0~V_{CC} (Note5)	
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~20	ns/V

Note4: Output in off state

Note5: High or low state

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40~85°C Min	Ta = −40~85°C Max	Unit
Input voltage	High level	V_{IH}	—		4.5~5.5	2.0	—	—	2.0	—	V
	Low level	V_{IL}	—		4.5~5.5	—	—	0.8	—	0.8	
Output voltage	High level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	4.5	4.4	4.5	—	4.4	—	V
				I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
	Low level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	—	0	0.1	—	0.1	
				I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.25	−	±2.50	μA
Input leakage current		I_{IN}	V_{IN} = 5.5 V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA
		I_{CCT}	Per input: V_{IN} = 3.4 V Other input: V_{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output leakage current		I_{OPD}	V_{OUT} = 5.5 V		0	—	—	0.5	—	5.0	μA

Timing Requirements (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = −40~85°C Limit	Unit
Minimum pulse width (CK)	$t_{w(H)}$ $t_{w(L)}$	—	5.0 ± 0.5	—	6.5	8.5	ns
Minimum set-up time	t_s	—	5.0 ± 0.5	—	2.5	2.5	ns
Minimum hold time	t_h	—	5.0 ± 0.5	—	2.5	2.5	ns

AC Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	—	5.0 ± 0.5	15	—	4.1	9.4	1.0	10.5	ns
				50	—	5.6	10.4	1.0	11.5	
3-state output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	5.0 ± 0.5	15	—	6.5	10.2	1.0	11.5	ns
				50	—	7.3	11.2	1.0	12.5	
3-state output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	5.0 ± 0.5	50	—	7.0	11.2	1.0	12.0	ns
Maximum clock frequency	f_{max}	—	5.0 ± 0.5	15	90	140	—	80	—	MHz
				50	85	130	—	75	—	
Output to output skew	t_{osLH} t_{osHL}	(Note6)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Output capacitance	C_{OUT}	—			—	9	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note7)			—	25	—	—	—	pF

Note6: Parameter guaranteed by design.
$t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

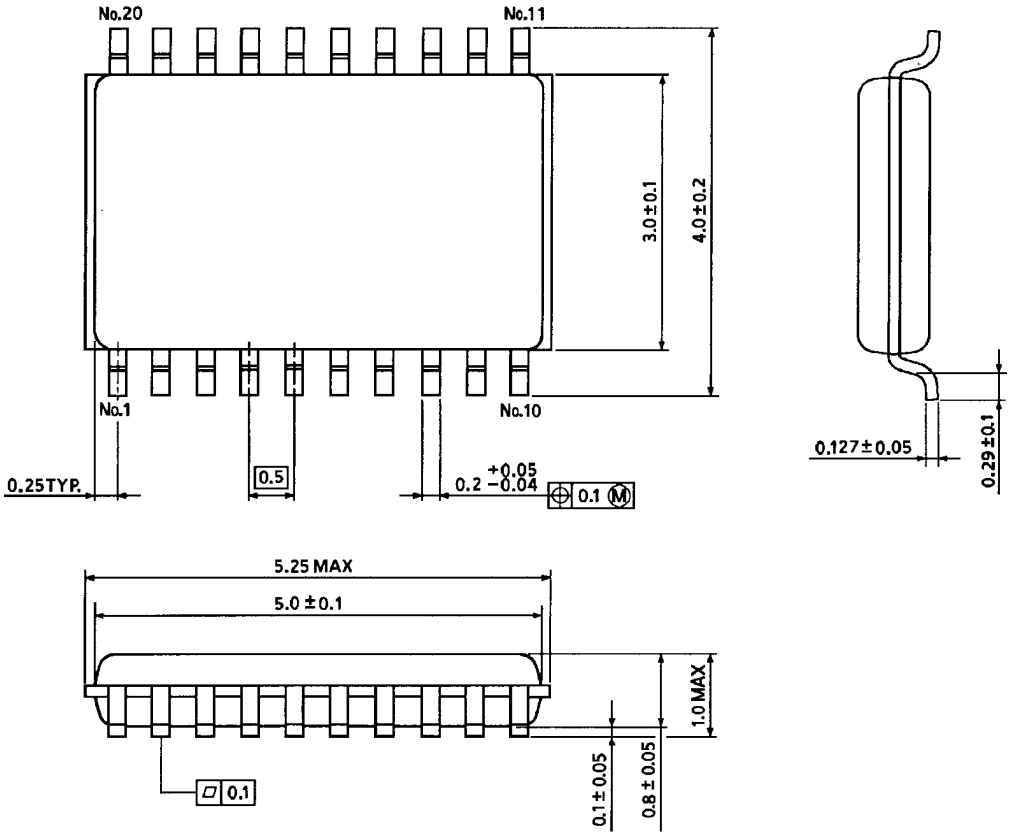
Note7: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F)
And the total C_{PD} when n pcs. of latch operate can be gained by the following equation:
C_{PD} (total) = 14 + 11·n

Noise Characteristics (Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	1.1	1.5	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	−1.1	−1.5	V
Minimum high level dynamic input voltage V_{IH}	V_{IHD}	C_L = 50 pF	5.0	—	2.0	V
Maximum low level dynamic input voltage V_{IL}	V_{ILD}	C_L = 50 pF	5.0	—	0.8	V

Package Dimensions

VSSOP20-P-0030-0.50 Unit : mm



Weight: 0.03 g (typ.)