1.3 GHz PLL for TV- and VCR- Tuner

Description

The U6209B is a single chip PLL frequency synthesizer with unidirectional I²C-bus control. This IC contains a high frequency prescaler which can be switched off. Five open collector switching outputs are available. The U6209B has a programmable 512/1024 reference divider.

Features

- 1.3 GHz divide-by-8 prescaler integrated (can be bypassed)
- 15 bit counter accepts input frequencies up to 170 MHz
- Programmable reference divider: divider by 512 or 1024
- µP-controlled by I²C-Bus (MC44818 data format compatible)
- Five port outputs (open collector)
- Four addresses selectable at Pin 10 for multi-tuner application
- 31.25 kHz (–1.3 GHz) / 3.90625 kHz (–170 MHz) tuning steps with 4MHz Xtal
- Electrostatic protection according to MILSTD 883
- SO16 small package

Block Diagram

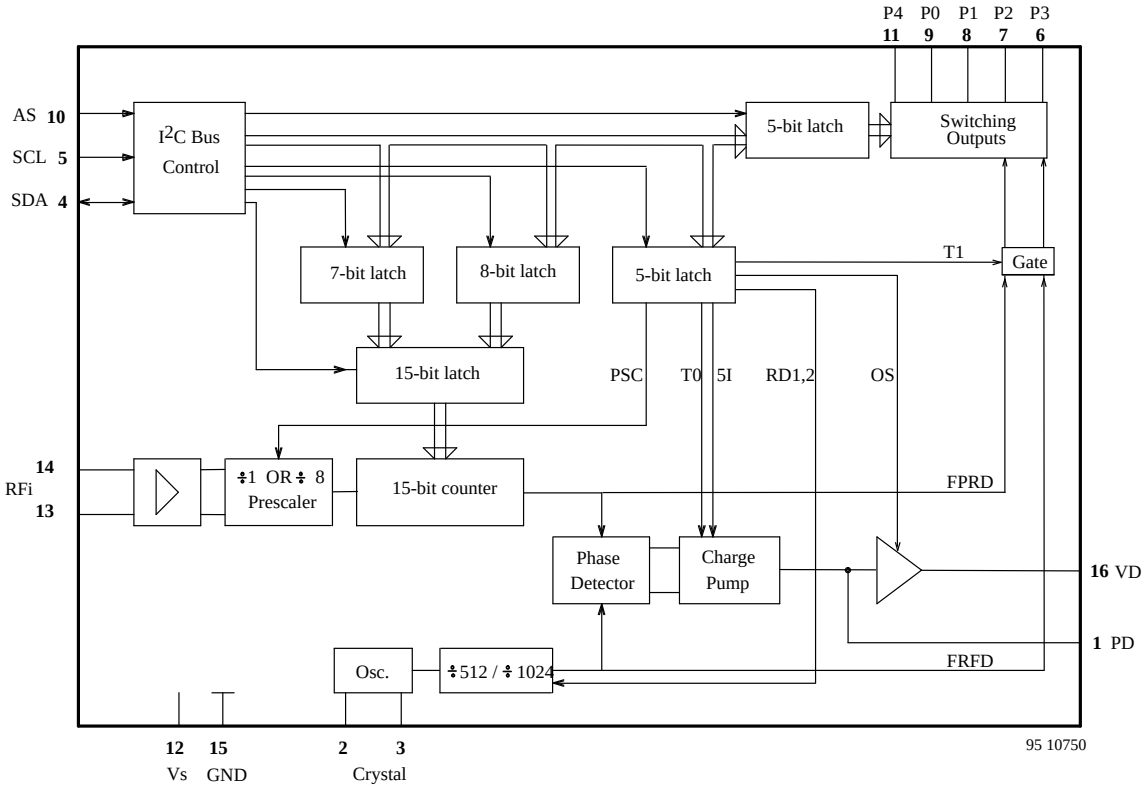


Figure 1.

Ordering Information

Extended Type Number	Package	Remarks
U6209B-GFPG3	SO16 plastic package	Taped and reeled

Pin Configuration

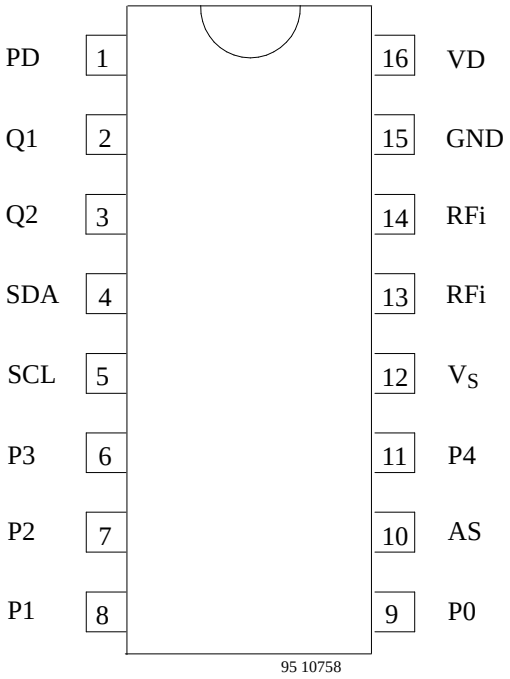


Figure 2.

Pin	Symbol	Function
1	PD	Charge pump output
2	Q1	Crystal
3	Q2	Crystal
4	SDA	Data in/output
5	SCL	Clock
6	P3	Port output (open collector)
7	P2	Port output (open collector)
8	P1	Port output (open collector)
9	P0	Port output (open collector)
10	AS	Address select input
11	P4	Port output (open collector)
12	Vs	Supply voltage
13	RFi	RF input
14	RFi	RF input
15	GND	Ground
16	VD	Active filter output

Circuit Description

The U6209B is a single-chip PLL designed for TV and VCR receiver systems. It consists of a bridgeable divide-by-8 prescaler with an integrated preamplifier, a 15-bit programmable divider, a crystal oscillator and a reference divider with two selectable divider ratios (512 / 1024), and a phase/frequency detector together with a charge pump which drives the tuning amplifier. Only one external transistor is required for varactor-line driving. The device can be controlled via I^2C bus format. There are four programmable addresses selectable, programmed by applying a specific input voltage to the address-select input, enabling the use of up to four synthesizers in a system. Five open collector output port functions are included which are capable of sinking at least 10 mA.

Oscillator frequency calculation:

fvco = PSF x SF x frefosc / 1024

fvco: Locked frequency of voltage controlled oscillator

PSF : Scaling factor of prescaler (1 or 8)
SF : Scaling factor of programmable 15-bit divider
frefosc :Reference oscillator frequency:
3.2/4 MHz crystal or external reference frequency

In addition, there are port outputs available for band-switching and other purposes.

Application

A typical application is shown on page 10. All input / output interface circuits are shown on page 9.

Some special features which are related to test- and alignment procedures for tuner production are explained together within the following I^2C bus mode description.

Absolute Maximum Ratings

All voltages are referred to GND (Pin 15).

Parameters		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 12	V_S	–0.3		6	V
RF input voltage	Pins 13,14	RFi	–0.3		V_S + 0.3	V
Crystal input voltage	Pin 2	Q1	–0.3		V_S + 0.3	V
Charge pump output voltage	Pin 1	PD	–0.3		V_S + 0.3	V
Active filter output voltage	Pin 16	VD	–0.3		V_S + 0.3	V
Bus input/ output voltage	Pin 4	VSDA	–0.3		6	V
	Pin 5	VSCL	–0.3		6	V
SDA output current	open collector Pin 4	ISDA	–1		5	mA
Address select voltage	Pin 10	VAS	–0.3		V_S + 0.3	V
Port output current open collector	Pins 6–9,11	P0–4	–1		15	mA
Total port output current open collector	Pins 6–9,11	P0–4	–1		50	mA
Port output voltage in off state		P0–4	–0.3		15	V
In ON state	Pins 6–9,11		–0.3		6	V
Junction temperature		Tj	–40		125	°C
Storage temperature		Tstg	–40		125	°C

Operating Range

All voltages are referred to GND (Pin 15).

Parameters	Test Conditions / Pins		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Pin 12	Vs	4.5		5.5	V
Ambient temperature			T_{amb}	0		70	°C
Input frequency	PSC = 1	Pins 13,14	RFi	64		1300	MHz
Input frequency	PSC = 0	Pins 13,14	RFi	1		170	MHz
Programmable divider			SF	256		32767	
Crystal oscillator		Pin 2	fXTAL	3	4	4.48	MHz

Thermal Resistance

Parameters	Symbol	Value	Unit
SO16 small package	R_{thJA}	110	K/W

Electrical Characteristics

Test Conditions (unless otherwise specified) : V_S = 5V, T_{amb} = 25°C.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current (prescaler ON)	SW 0–4 = 0; PSC =1 Pin 12	Is	32	42	52	mA
(prescaler OFF)	SW 0–4 = 0; PSC =0 Pin 12	Is	22	28	35	mA
Input sensitivity						
fi = 80 - 1000 MHz	PSC = 1 Pin 13	Vi 1)	10		315	mVrms
fi = 1300 MHz	PSC = 1 Pin 13	Vi 1)	40		315	mVrms
fi = 10 - 170 MHz	PSC = 0 Pin 13	Vi 1)	10		315	mVrms
Port outputs (open collector)	P0–4 Pins 6–9, 11					
Leakage current	VH = 13.5 V	IL			10	uA
Saturation voltage	IL = 10 mA	VSL 2)			0.5	V
Charge pump output (PD)						
Charge pump current ‘H’	5I = 1, VPD = 2 V Pin 1	IPDH		180		uA
Charge pump current ‘L’	5I = 0, VPD = 2 V Pin 1	IPDL		50		uA
Charge pump leakage current	T0 = 0, VPD = 2 V Pin 1	IPDTRI		5		nA
Charge pump amplifier gain	Pins 1, 16			6400		
Bus inputs (SDA,SCL)						
Input voltage high	Pins 4, 5	Vi ‘H’	3		5.5	V
Input voltage low	Pins 4, 5	Vi ‘L’			1.5	V
Input current high	Vi ‘H’ = V_S Pins 4, 5	Ii ‘H’			10	uA
Input current low	Vi ‘L’ = 0 V Pins 4, 5	Ii ‘L’	– 20			uA
Output voltage SDA (open collector)	ISDA ‘L’ = 2 mA Pin 4	VSDA ‘L’			0.4	V
Address selection input (AS)						
Input current high Input current low	VAS “H” = V_S Pin 8 VAS “L” = 0 V Pin 8	IiAS “H” IiAS “L”	 – 100		10	uA

Notes:
1) RMS-voltage calculated from the measured available power on 50 Ω
2) Tested with one switch active

Functional Description

The U6209B is programmed via a 2–wire I^2C bus data format. The three bus input Pins 4, 5, 10 are used as SDA, SCL and address select inputs. The data includes the scaling factor SF (15 bit) and port output information. There are some additional functions included for testing of the device.

I^2C - Bus Description

The U6209B is controlled via a 2-wire I^2C bus format by feeding data and clock signals into the SDA and SCL lines respectively. The table 'I^2C–BUS DATA FORMAT' describes the format of the data and shows how to select the device address by applying a voltage at pin 10. When the correct address byte has been received, the SDA line is pulled low by the device during the acknowledge period, and then also during the acknowledge periods, when additional data bytes are programmed. After the address transmission (first byte), data bytes can be sent to the device. There are four data bytes requested to fully program the device. The programmable divider latch is loaded after the 8th clock pulse of the second divider byte PDB2, the control and the port register latches are loaded after the 8th clock pulse of the control byte CB1 respectively post byte CB2. The table 'I^2C-BUS PULSE DIAGRAM' shows some possible data transfer examples.

The programmable divider bytes PDB1 and PDB2 are stored in a 15-bit latch and control the division ratio of the 15-bit programmable divider. The control Byte CB1 enables the control of the the following special functions:

- 5I-bit switches between low and high charge pump current
- T1-bit enables divider test mode when it is set to logic 1
- T0-bit enables the charge pump to be disabled when it is set to logic 1
- RD1 and RD2-bit allow selection of the reference divider ratio
- PSC–bit switches prescaler off when it is set to logic 0
- OS-bit disables the charge pump drive amplifier output when it is set to logic 1.

When T1 is set to logic 1, the programmable divider output signal is switched to pin 7 and the reference divider output signal is switched to pin 6. The OS-bit function disables the complete PLL function. This enables tuner alignment by supplying the tuning voltage directly via the 30-V supply voltage of the tuner. The control byte CB2 programs the port outputs P0-4; a logic 0 for high impedance output (off) and a logic 1 for low impedance output (on).

I²C - Bus Description (continued)

Data Formats

Description	Data Format								
	MSP							LSB	
Address byte	1	1	0	0	0	AS1	AS2	0	A
Programmable divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Programmable divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control byte 1	1	5I	T1	T0	RD2	RD1	PSC	OS	A
Control byte 2	X	X	X	P4	P3	P2	P1	P0	A

A = Acknowledge; X = not used; Unused bits of control byte 2 should be 0 for lowest power consumption

n0..n14 :	Scaling factor (SF)	SF = 16384 x n14 + 8192 x n13 + ... + 2 x n1 + n0	
PSC :	Prescaler on / off	PSC = 1 : prescaler on (PSF = 8)	
		PSC = 0 : prescaler off (PSF = 1)	
T0, T1 :	Testmode selection	T1 = 1 : divider test mode on	T1 = 0 : divider test mode off
		T0 = 1 : charge pump disable	T0 = 0 : charge pump enable
P0–4:	Port outputs	P0–4 = 1: open collector active	
5I :	Charge pump current switch	5I = 1 : high current	5I = 0 : low current
OS :	Output switch	OS = 1 : varicap drive disable	OS = 0 : varicap drive enable
RD1, RD2:	Reference divider section		

RD1,RD2 : Reference divider selection

RD2	RD1	Reference Divider Ratio
0	0	512
0	1	1024
1	0	1024
1	1	512

AS1	AS2	Address	Hex. Value	Dec. Value	Voltage at Pin 10
0	1	1	C2	194	open
0	0	2	C0	192	0 to 10% V_S
1	0	3	C4	196	40 to 60% V_S
1	1	4	C6	198	90 to 100% V_S

Pulse Diagram

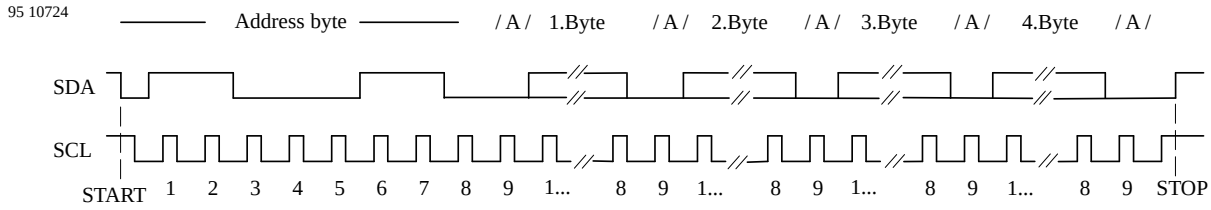


Figure 3.

Data transfer examples	Description
	START = Start condition
START – ADR – PDB1 – PDB2 – CB1 – CB2 – STOP	ADR = Address byte
START – ADR – CB1 – CB2 – –PDB1 – PDB2 – STOP	PDB1 = Programmable divider byte 1
START – ADR – PDB1 – PDB2 – CB1 – STOP	PDB2 = Programmable divider byte 2
START – ADR – PDB1 – PDB2 – STOP	CB1 = Control byte 1
START – ADR – CB1 – CB2 – STOP	CB2 = Control byte 2
START – ADR – CB1 – STOP	STOP = Stop condition

Bus Timing

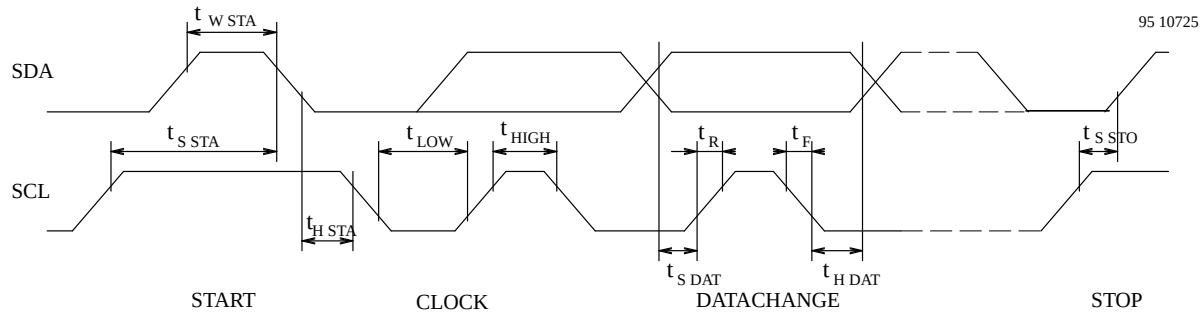


Figure 4.

tS STT	– Set-up time start	tS DAT	– Set-up time data
tW STT	– Waiting-time start	tH DAT	– Hold-time data
tH STT	– Hold-time start	tS STO	– Set-up time stop
tLOW	– “L”-Pulse width clock	tR	– Rise time
tHIGH	– “H”-Pulse width clock	tF	– Fall time

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Bus timing						
Rise time SDA, SCL		tR			15	µs
Fall time SDA, SCL		tF			15	µs
Clock frequency SCL		fSCL	0		100	kHz
Clock “H” Pulse		tHIGH	4			µs
Clock “L” Pulse		tLOW	4			µs
Hold time start		tHSTA	4			µs
Waiting time start		tWStt	4			µs
Set up time start		tSSTT	4			µs
Set-up time stop		tSSTO	4			µs
Set-up time data		tSDAT	0.3			µs
Hold time data		tHDAT	0			µs

Typical Prescaler Input Sensitivity (Prescaler on: PSC = 1) :

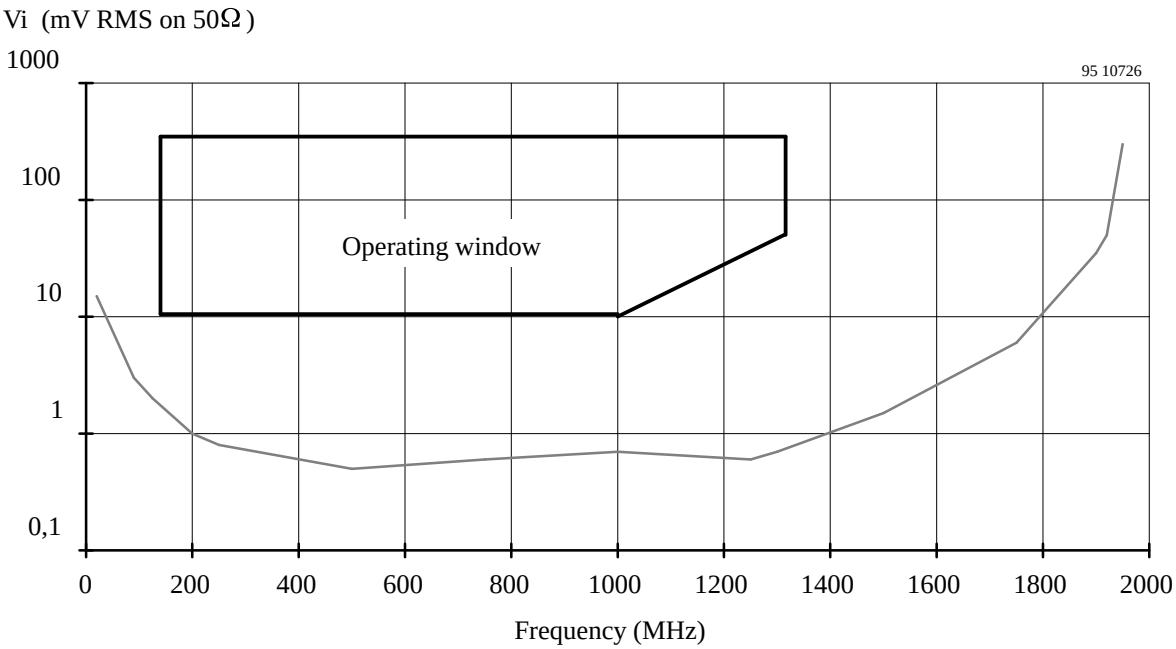


Figure 5.

Typical Prescaler Input Sensitivity (Prescaler off: PSC = 0) :

ω

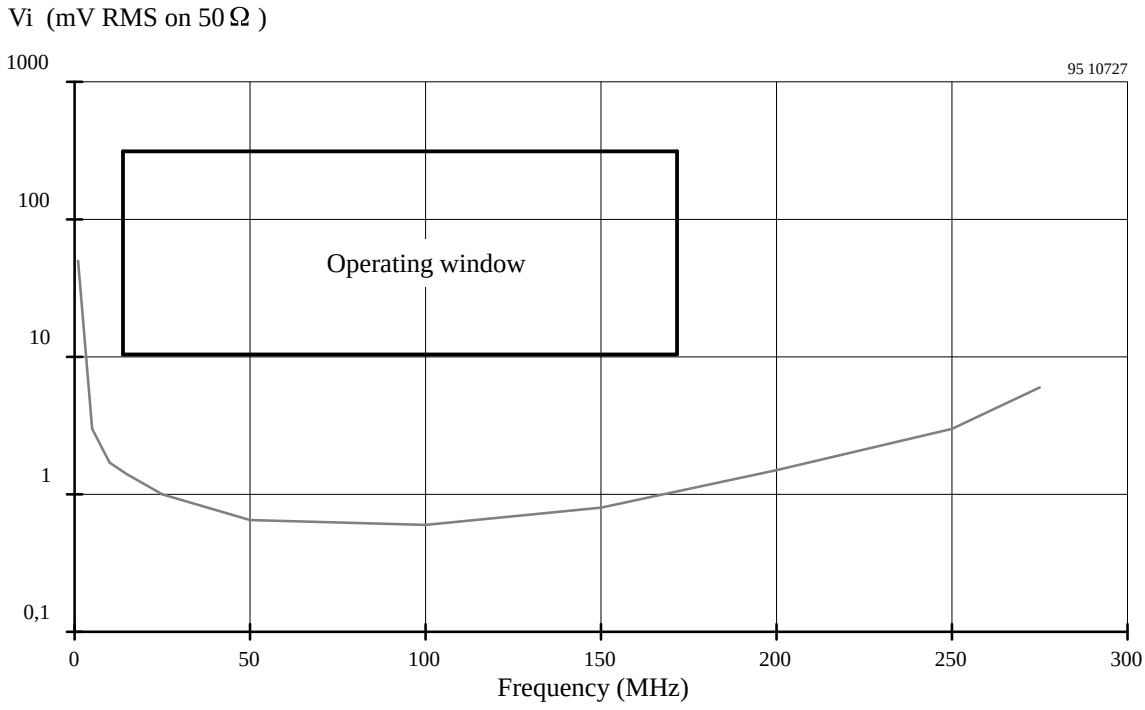


Figure 6.

Input/Output Interface Circuits

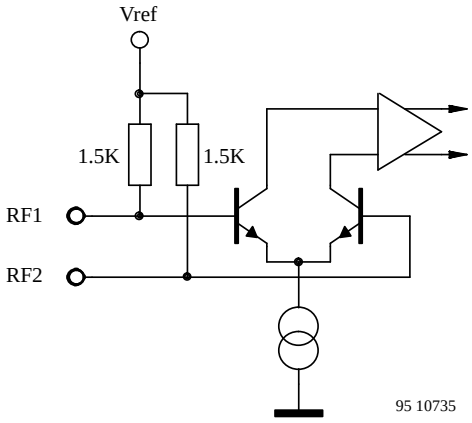


Figure 7. RF input

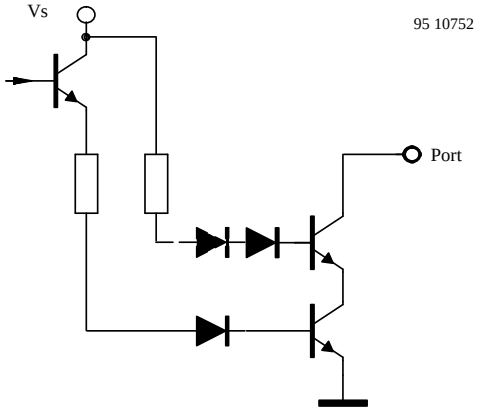


Figure 10. Ports

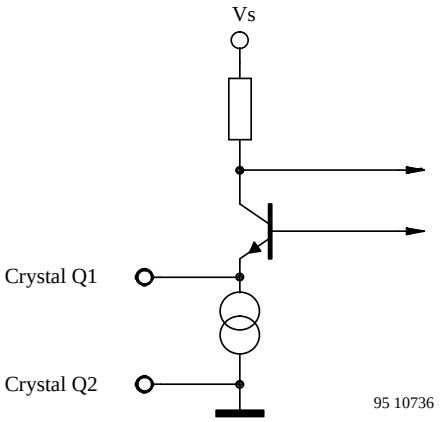


Figure 8. Reference oscillator

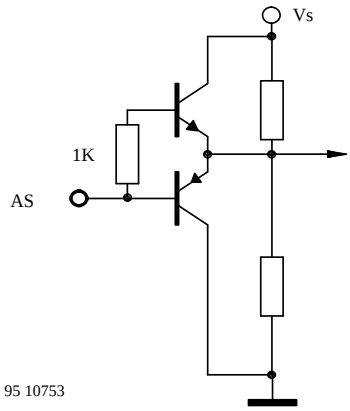


Figure 11. Address select input

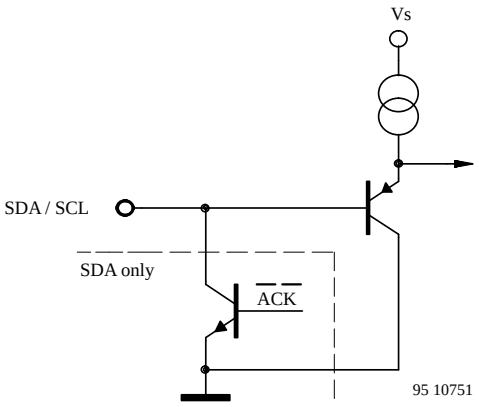


Figure 9. SCL and SDA input

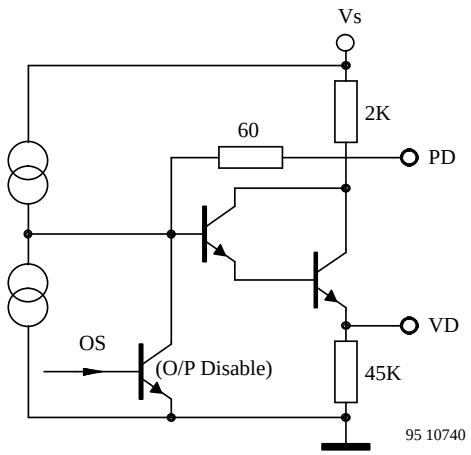


Figure 12. Loop amplifier

Application Circuit

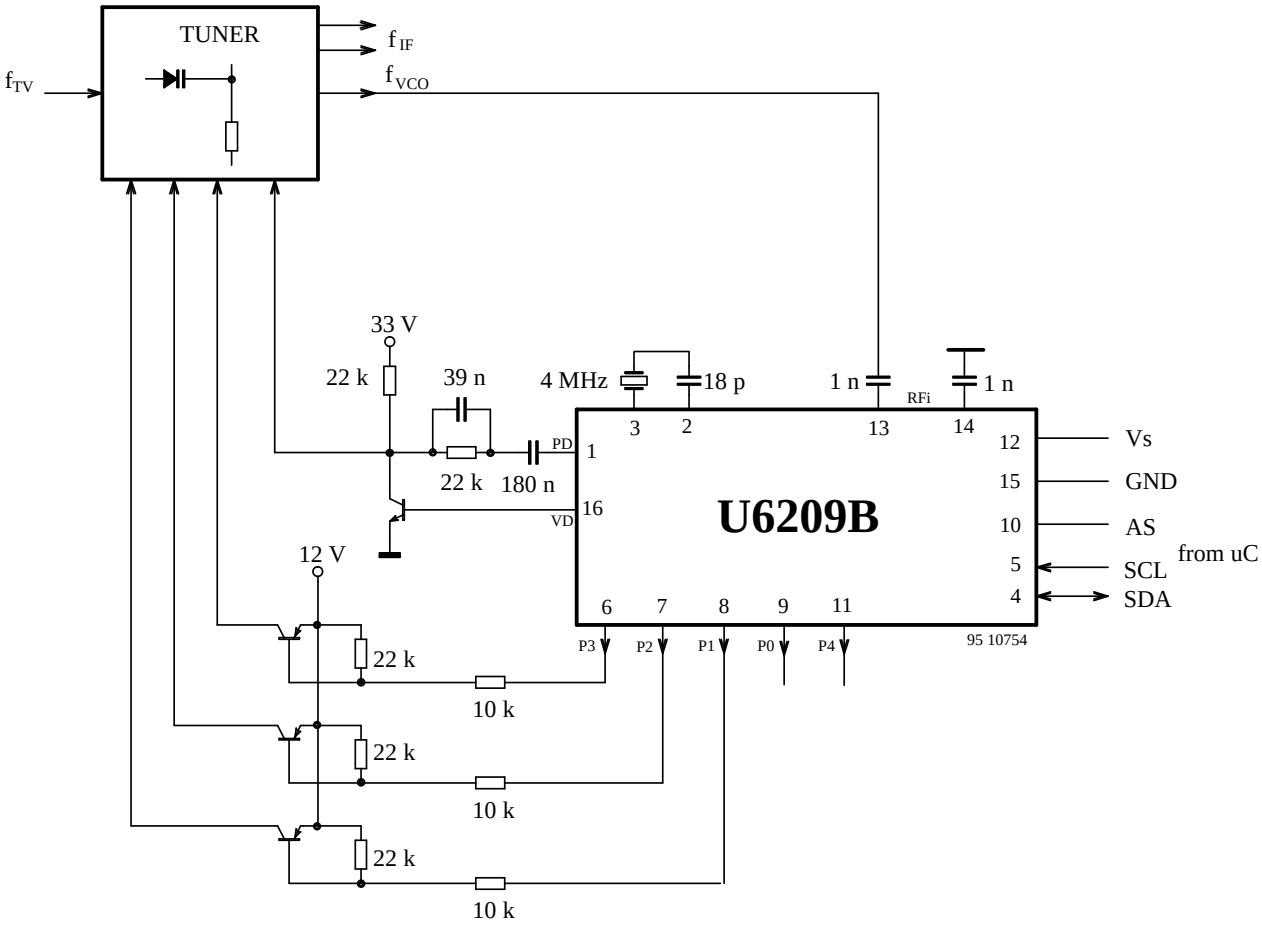
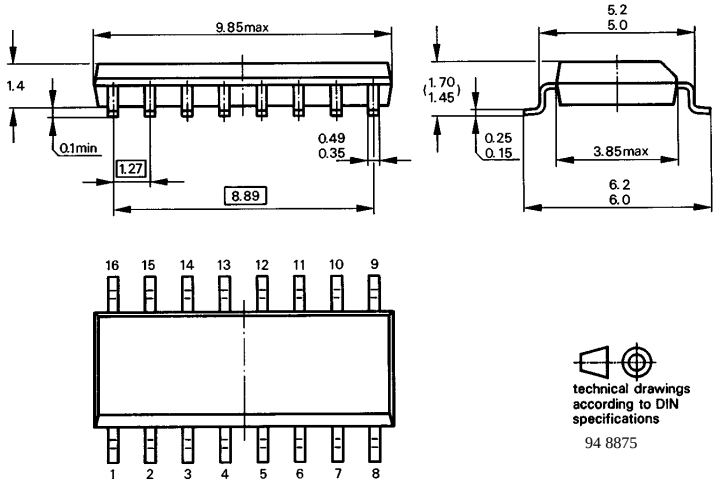


Figure 13.

Package Dimensions

Small outline plastic package, 16-pin SO16
Dimensions in mm



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1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423