XILINX®

XCR3320: 320 Macrocell SRAM CPLD

DS033 (v1.3) October 9, 2000 **Product Specification**

Features

- 320 macrocell SRAM based CPLD
- Configuration times of under 1.0 second
- IEEE 1149.1 compliant JTAG testing capability
  - Five pin JTAG interface
  - IEEE 1149.1 TAP controller
- In system configurable
- 3.3V device with 5V tolerant I/O
- Innovative XPLA2 Architecture combines extreme flexibility and high speeds
- Eight synchronous clock networks with programmable polarity at every macrocell
- Up to 32 asynchronous clocks support complex clocking needs
- Innovative XOR structure at every macrocell provides excellent logic reduction capability
- Logic expandable to 36 product terms on a single macrocell
- Advanced 0.35µ SRAM process
- Design entry and verification using industry standard and Xilinx CAE tools
- Control Term structure provides either sum terms or product terms in each logic block for:
  - 3-state buffer control
  - Asynchronous macrocell register reset/preset
- Global 3-state pin facilitates "bed of nails" testing without sacrificing logic resources
- Programmable slew rate control
- Small form factor packages with high I/O counts
- Available in commercial and industrial temperature ranges

Description

The XCR3320 device is a member of the CoolRunner® family of high-density SRAM-based CPLDs (Complex Programmable Logic Device) from Xilinx. This device combines high speed and deterministic pin-to-pin timing with high density. The XCR3320 uses the patented Fast Zero Power (FZP™) design technique that combines high speed and low power for the first time ever in a CPLD. FZP allows the XCR3320 to have true pin-to-pin timing delays of 7.5 ns, and standby currents of 100 µA without the need for `turbo bits' or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used since the bipolar era) with a cascaded chain of pure CMOS gates, both standby and dynamic power are dramatically reduced when compared to other CPLDs. The FZP design technique is also what allows Xilinx to offer a true CPLD architecture in a high density device.

The Xilinx XCR3320 devices use the patented XPLA2 (eXtended Programmable Logic Array) architecture. This architecture combines the best features of both PAL- and PLA-type logic structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA2 architecture is constructed from 80 macrocell Fast Modules that are connected together by an interconnect array. Within each Fast Module are four Logic Blocks of 20 macrocells each. Each Logic Block contains a PAL structure with four dedicated product terms for each macrocell. In addition, each Logic Block has 32 additional product terms in a PLA structure that can be shared through a fully programmable OR array to any of the 20 macrocells. This combination efficiently allocates logic throughout the Logic Block, which increases device density and allows for design changes without re-defining the pinout or changing the system timing. The XCR3320 offers pin-to-pin propagation delays of 7.5 ns through the PAL array of a Fast Module; and if the PLA array is used, an additional 1.5 ns is added to the delay, no matter how many PLA product terms are used. If the interconnect array between Fast Modules is used, there is a second fixed delay of 2.0 ns. This means that the worst case pin-to-pin propagation delay within a fast module is 7.5 + 1.5 = 9.0 ns, and the delay from any pin to any other pin across the entire chip is 7.5 + 2.0 = 9.5 ns if only the PAL array is used, and 7.5 + 1.5 + 2.0 = 11.0 ns if the PLA array is used.

Each macrocell also has a two input XOR gate with the dedicated PAL product terms on one input and the PLA product terms on the other input. This patent-pending Versatile XOR structure allows for very efficient logic optimization compared to competing XOR structures that have only one product term as the second input to the XOR gate. The Versatile XOR allows an 8-bit XOR function to be implemented in only 20 product terms, compared to 65 product terms for the traditional XOR approach.

The XCR3320 is SRAM-based, which means that it is configured from an external source at power up. See the configuration section of this data sheet for more information. The device supports the full JTAG specification (IEEE 1149.1) through an industry standard JTAG interface. It can also be configured through the JTAG port, which is very useful for prototyping. See section titled "Device Configuration Through JTAG" on page 29 for more information.

The XCR3320 CPLDs are supported by industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, Synario, Viewlogic, and Synplicity), using text (ABEL, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses a Xilinx developed tool including WebFITTER.

XPLA2 Architecture

Figure 1 shows a high level block diagram of the XCR3320 implementing the XPLA2 architecture. The XPLA2 architecture is a multi-level, modular hierarchy that consists of Fast Modules interconnected by a virtual crosspoint switch called the Global Zero Power Interconnect Array (GZIA). Each Fast Module accepts 64 bits from the GZIA and outputs 64 bits to the GZIA. Each Fast Module is essentially an 80 macrocell CPLD with four logic blocks of 20 macrocells each inside. There are eight dedicated, low-skew, global clocks for the device; and each Fast Module has access to any two of these clocks (there are additional asynchronous clocks available in the Fast Modules, see Figure 3. There are also Global 3-state (gts) and Global Reset (rstn) pins that are common to all Fast Modules. When gts is pulled high, all output buffers in the device will be disabled, causing all I/O pins to be tri-stated. When rstn is pulled low, all flip-flops of the device will be reset.

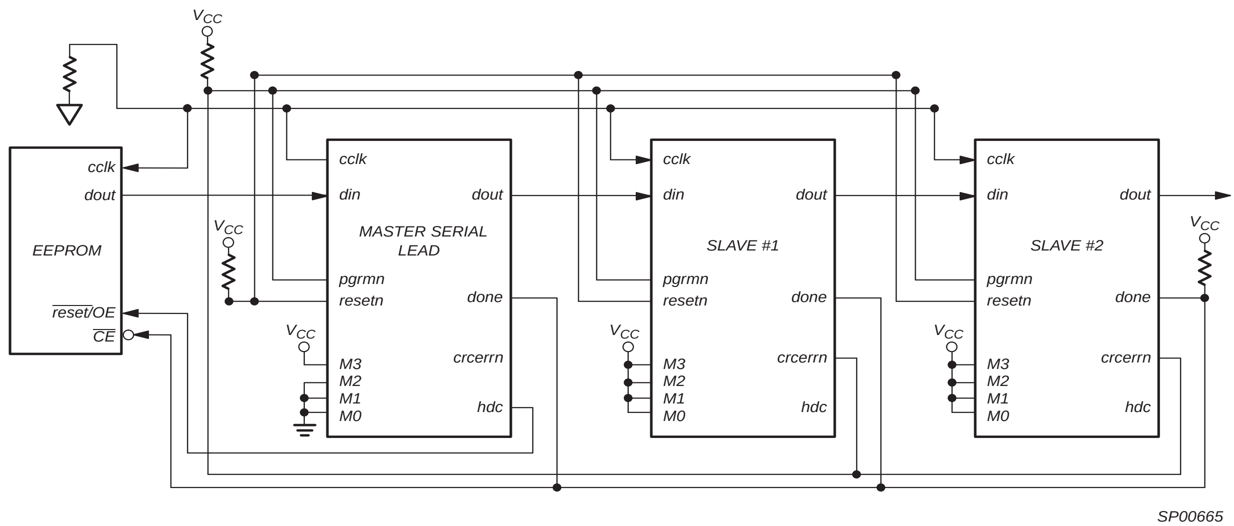


Figure 1: Xilinx XPLA2 CPLD Architecture

XPLA2 Fast Module

Each Fast Module consists of four Logic Blocks of 20 macrocells each. Depending on the package, either seven or 12 of the 20 macrocells in each Logic Block are connected to I/O pins, and the remaining macrocells are used as buried nodes. These four Logic Blocks are connected together by the Local Zero Power Interconnect Array (LZIA). The LZIA is a virtual crosspoint switch that connects the Logic Blocks to each other and to the GZIA. The feedback from all 80 macrocells, input from the I/O pins, and the 64 bit input bus from the GZIA are input into the LZIA. The LZIA outputs 36 signals into each Logic Block and 64 signals into the GZIA (Figure 2).

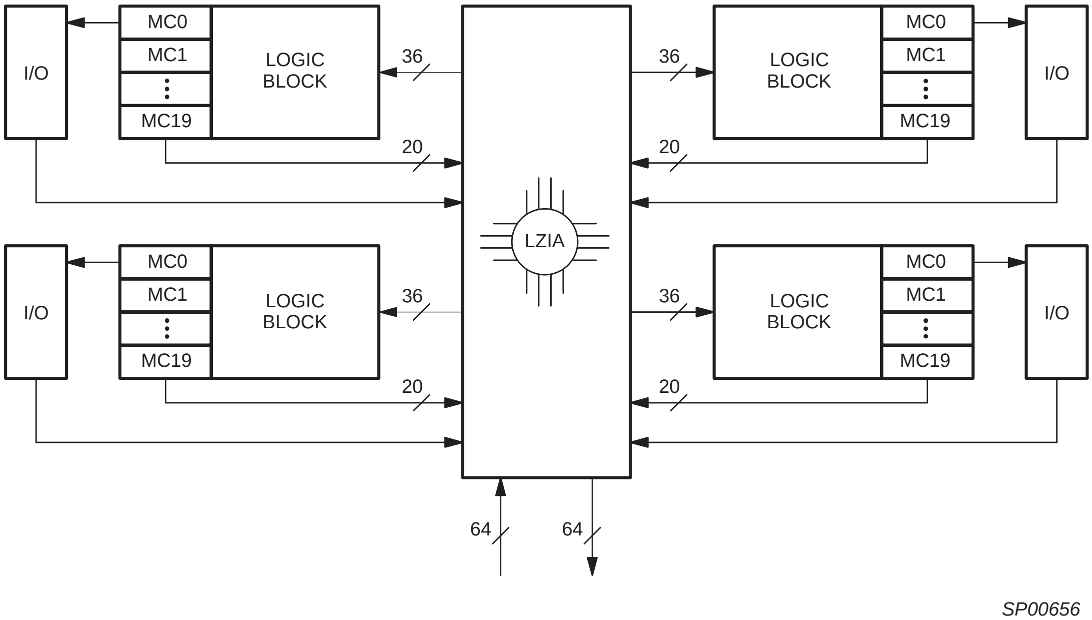


Figure 2: Xilinx XPLA2 Fast Module

XPLA2 Logic Block Architecture

Figure 3 illustrates the XPLA2 Logic Block architecture. Each Logic Block contains eight control terms, a PAL array, a PLA array, and 20 macrocells. The 36 inputs from the LZIA are available to all control terms and to each product term in both the PAL and the PLA array. The eight control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the asynchronous preset and reset functions of the macrocell registers, the output enables of the 20 macrocells, and for asynchronous clocking. The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array.

Each macrocell has four dedicated product terms from the PAL array. When additional logic is required, each macrocell takes the extra product terms from the PLA array. The PLA array consists of 32 extra product terms that are shared between the 20 macrocells of the Logic Block. The PAL product terms can be connected to the PLA product terms through either an OR gate or an XOR gate. One input to the XOR gate can be connected to all the PLA terms, which provides for extremely efficient logic synthesis. An eight bit XOR function can be implemented in only 20 product terms. Each macrocell can use the output from the OR gate or the XOR gate in either normal or inverted state.

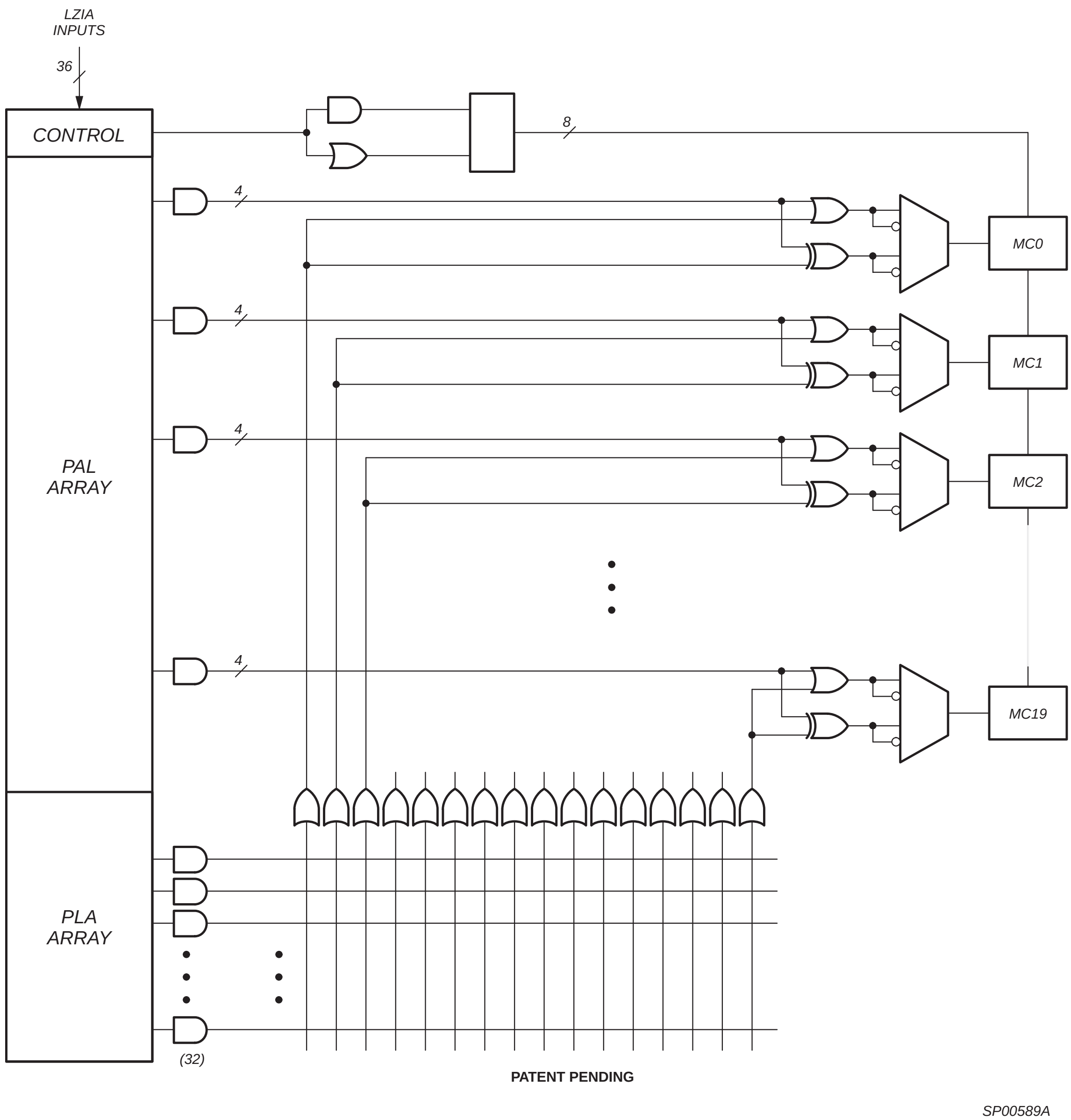


Figure 3: Xilinx XPLA2 Logic Block Architecture

XPLA2 Macrocell Architecture

Figure 4 shows the XPLA2 macrocell architecture used in the XCR3320. The macrocell can be configured as either a D- or T-type flip-flop or a combinatorial logic function. A D-type flip-flop is generally more useful for implementing state machines and data buffering while a T-type flip-flop is generally more useful in implementing counters. Each of these flip-flops can be clocked from any one of four sources. Two of the clock sources (CLK0 and CLK1) are from the eight dedicated, low-skew, global clock networks designed to preserve the integrity of the clock signal by reducing skew between rising and falling edges. These clocks are designated as "synchronous" clocks and must be driven by an external source. Both CLK0 and CLK1 can clock the macrocell flip-flops on either the rising edge or the falling edge of the clock signal. The other clock sources are designated as "asynchronous" and are connected to two of the eight control terms (CT6 and CT7) provided in each logic block. These clocks can be individually configured as any PRODUCT term or SUM term equation created from the 36 signals available inside the logic block. Thus, in each Logic Block, there are up to four possible clocks; and in each Fast Module, there are up to ten possible clocks. Throughout the entire device, there are up to 40 possible clocks–eight from the dedicated, low-skew, global clocks, and two for each of the 16 logic blocks.

The remaining six control terms of each logic block (CT0-CT5) are used to control the asynchronous preset/reset of the flip-flops and the enable/disable of the output buffers in each macrocell. Control terms CT0 and CT1 are used to control the asynchronous preset/reset of the macrocell's flip-flop. Note that the power-on reset leaves all macrocells in the "zero" state when power is properly applied, and that the preset/reset feature for each macrocell can also be disabled. Each macrocell can choose between an asynchronous reset or an asynchronous preset function, but both cannot be simultaneously used on the same register. The global rstn function can always be used, regardless of whether or not asynchronous reset or preset control terms are enabled. Control terms CT2, CT3, CT4 and CT5 are used to enable or disable the macrocell's output buffer. The output buffers can also be always enabled or always disabled. All CoolRunner devices also provide a Global 3-state (GTS) pin, which, when pulled high, will 3-state all the outputs of the device. This pin is provided to support "In-Circuit Testin" or "Bed-of-Nails" testing used during manufacturing.

For the macrocells in the Logic Block that are associated with I/O pins, there are two feedback paths to the LZIA: one from the macrocell, and one from the I/O pin. The LZIA feedback path before the output buffer is the macrocell feedback path, while the LZIA feedback path after the output buffer is the I/O pin feedback path. When these macrocells are used as outputs, the output buffer is enabled, and either feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pins are used as inputs, the output buffer of these macrocells will be 3-stated and the input signal will be fed into the LZIA via the I/O feedback path. In this case the logic functions implemented in the buried macrocell can be fed back into the LZIA via the macrocell feedback path. For macrocells that are not associated with I/O pins, there is one feedback path to the LZIA. Logic functions implemented in these buried macrocells are fed back into the LZIA via this path. All unused inputs and I/O pins should be properly terminated. Please refer to "Terminations" on page 8.

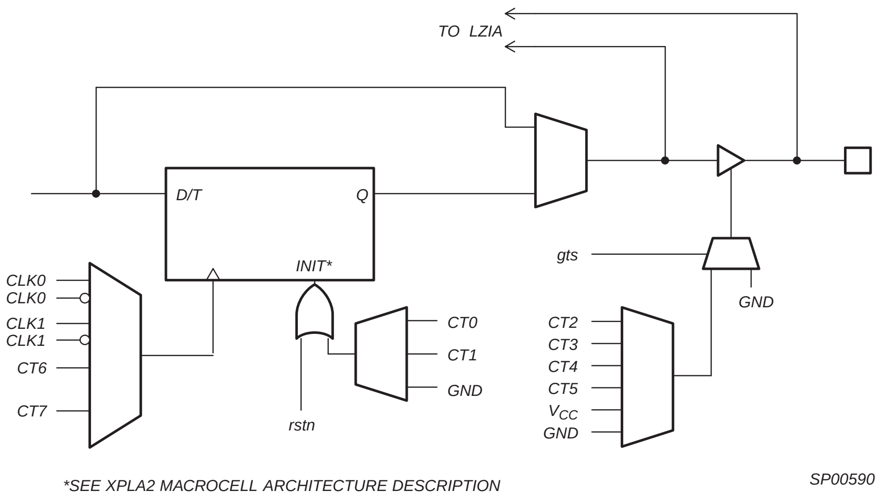


Figure 4: XCR3320 Macrocell Architecture

Simple Timing Model

Figure 5 shows the XCR3320 timing model. The XCR3320 timing model is very simple compared to the models of competing architectures. There are three main timing parameters: the pin-to-pin delay for combinatorial logic functions (t_{PD}), the input pin to register set up time (t_{SU}), and the register clock to valid output time (t_{CO}). As the model shows, timing is only dependent on whether or not the PLA array is used, and whether or not the logic function is created within a single Fast Module or uses the GZIA. The timing starts with a set time for t_{PD} and t_{SU} through the PAL array in a Fast Module, and there are fixed delays added for use of the PLA array or the GZIA. The t_{CO} (pin-to-pin) timing specification never changes. For example, a combinatorial logic function of four or fewer product terms constructed from inputs within the same logic block would have a t_{PD} delay of 7.5 ns. If the logic function were more than four product terms wide, the delay would be t_{PD} plus the fixed PLA delay, or 7.5 +1.5 = 9.0 ns. A function that used the PAL array and inputs from a different Fast Module would have a propagation delay of t_{PD} plus the fixed GZIA delay, or 7.5 + 2.0 = 9.5 ns.

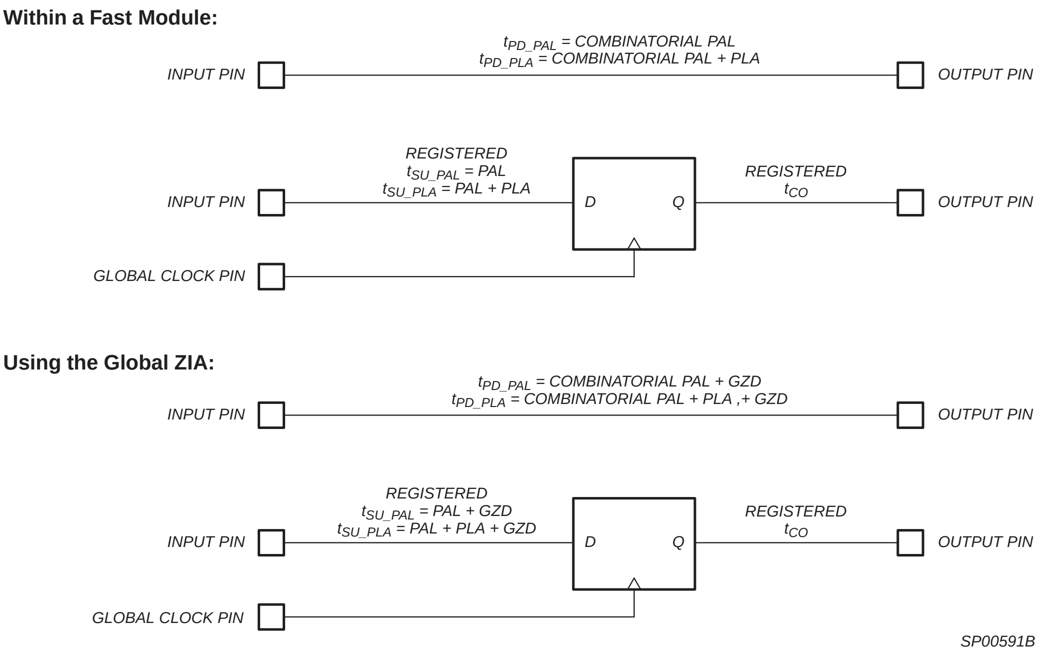


Figure 5: XCR3320 Timing Module

TotalCMOS Design Technique for Fast Zero Power

Xilinx is the first to offer a TotalCMOS CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its product terms instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. This also makes it possible to manufacture high density CPLDs like the XCR3320 that consume a fraction of the power of competing devices. Refer to Figure 6 and Table 1 showing the I_{CC} vs. Frequency of the XCR3320 TotalCMOS CPLD (data taken with 20 16-bit counters at 3.3V, 25°C, output buffers disabled).

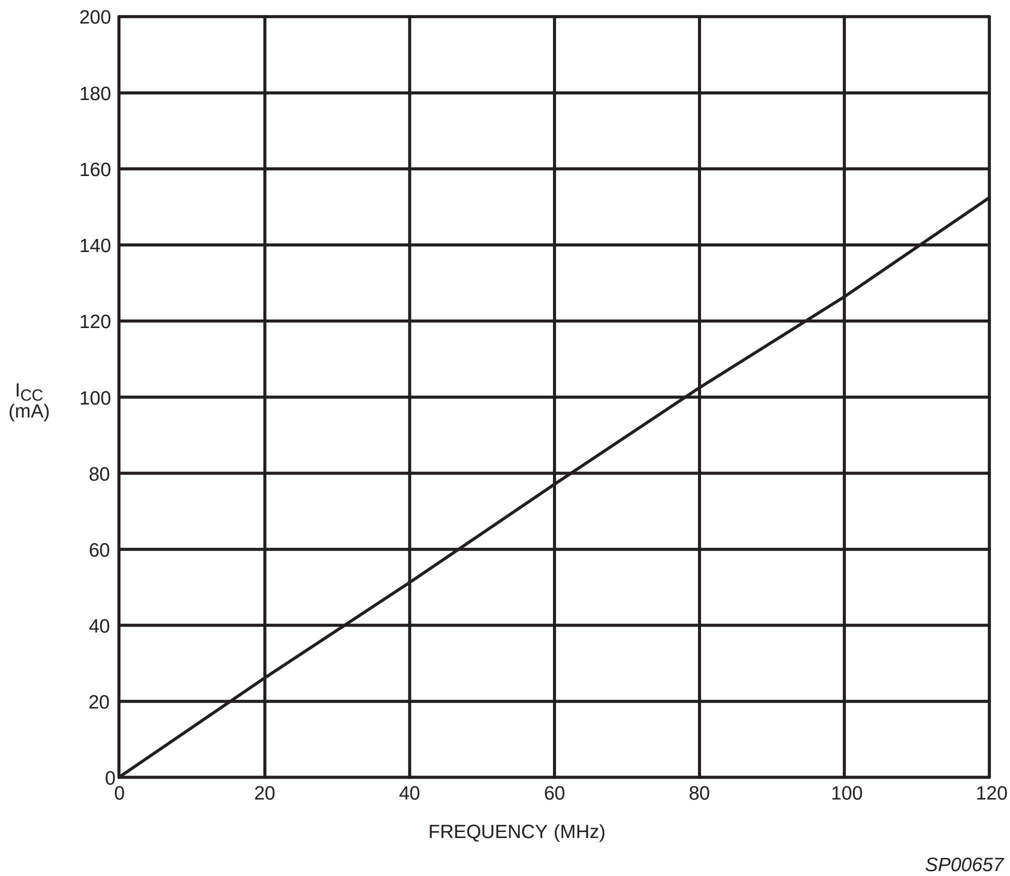


Figure 6: I_{CC} vs. Frequency at V_{CC} = 3.3V, 25°C

Table 1: I_{CC} vs. Frequency (V_{CC} = 3.3V, 25°C)

Frequency (MHz)	0	1	20	40	60	80	100	120
Typical I_{CC} (mA)	0.01	1.3	26	51	77	102	126	152

Terminations

The CoolRunner XCR3320 CPLDs are TotalCMOS™ devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. It can also cause the voltage on a configuration pin to float to an unwanted voltage level, interrupting device operation.

The XCR3320 CPLDs have programmable on-chip pull-down resistors on each I/O pin. These pull-downs are automatically activated by the fitter software for all unused I/O pins. Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the pull-down resistors will be turned on. We recommend that any unused I/O pins on the XCR3320 device be left unconnected.

There are no on-chip pull-down structures associated with dedicated pins used for device configuration or special device functions like global reset and global 3-state. Xilinx recommends that these pins be terminated consistent with pin functionality. Xilinx recommends the use of weak pull-up and pull-down resistors for terminating these pins. See the appropriate configuration section for more information on terminating dedicated pins.

When using the JTAG Boundary Scan functions, it is recommended that 10kΩ pull-up resistors be used on the tdi, tms, tck, and trstn pins. The tdo signal pin can be left floating unless it is connected to the tdi of another device. Letting these signals float can cause the voltage on tms to come close to ground, which could cause the device to enter JTAG/ISP mode at unspecified times.

Configuration Introduction

The Xilinx CoolRunner series are available in technologies which use non-volatile (EEPROM-based) and volatile (SRAM based) configuration memory. The functionality of the XPLA2 family of the CoolRunner series is defined by on-chip SRAM. The devices are configured in a manner similar to that of most FPGAs. This section describes the configuration of the XCR3320, and applies to all similarly configured devices to be produced by Xilinx.

Either Xilinx or third party software is used to generate a JEDEC file. The JEDEC file contains the configuration data, which is loaded into the XCR3320 configuration memory to control the XCR3320 functionality. This is done at power-up and/or with configure command. This section provides some of the trade-offs in selecting a configuration mode, and provides debug hints for configuration problems.

There are several different methods of configuring the XCR3320. The mode used is selected using the mode select pins. There are three basic configuration methods: master, slave, and peripheral. The configuration data can be transmitted to the XCR3320 serially or in parallel bytes. As a master, the XCR3320 generates the clock and control signals to strobe configuration data into the XCR3320. As a slave device, a clock is generated externally, and provided into the XCR3320s cclk pin. In the peripheral mode, the XCR3320 interfaces as a microprocessor peripheral. Please note that M3 should always be High. Table 2 lists the states for the other mode pins by configuration mode.

Table 2: Configuration Modes

M2	M1	M0	Cclk	Configuration Mode	Data Format
0	0	0	Output	Master serial	Serial
0	0	1	Input	Slave parallel	Parallel
0	1	0	Reserved		
0	1	1	Input	Synchronous peripheral	Parallel
1	0	0	Output	Master parallel - up	Parallel
1	0	1	Reserved		
1	1	0	Reserved		
1	1	1	Input	Slave serial	Serial

Design Flow Overview

Figure 7 is a diagram of the steps used in configuring the XCR3320. The development system is used to generate configuration data in the JEDEC file. Using the `<design>.jed` file, there are two general methods of configuring the XCR3320. The utility **download** can load the configuration data from a PC or workstation hard disk into the XCR3320. Alternately, the XCR3320 can be loaded from non-volatile ICs such as serial or parallel EEPROMs, after converting the JEDEC file to an MCS file using the `jed2mcs` utility.

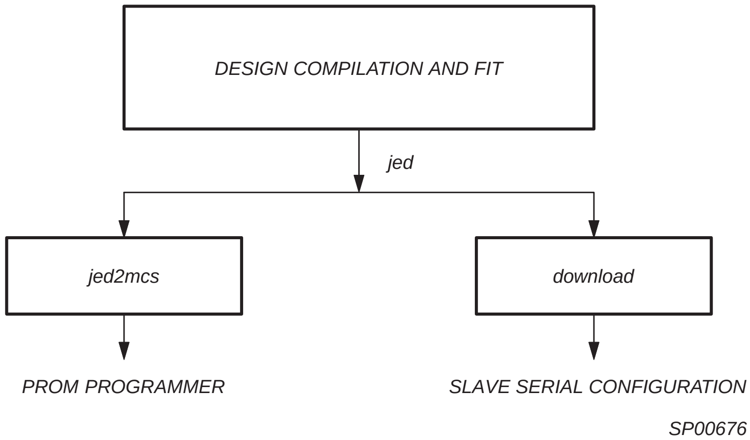


Figure 7: Design Flow

XCR3320 States Of Operation

Prior to becoming operational, the XCR3320 goes through a sequence of states, including initialization, configuration, and start-up. This section discusses these three states. In the master configuration modes, the XCR3320 is the source of configuration clock (cclk).

When configuration is initiated, a counter in the XCR3320 is set to zero and begins to count configuration clock cycles applied to the XCR3320. As each configuration data frame is supplied to the XCR3320, it is internally assembled into data words. Each data word is loaded into the internal configuration memory. The configuration loading process is complete when the internal length count equals the loaded length count in the length count field, and the required end of configuration frame is written.

All configuration I/Os used as inputs operate with TTL-level input thresholds during configuration. All I/Os that are not used during the configuration process are 3-stated with internal pull-downs. During configuration, registers are reset. The combinatorial logic begins to function as the XCR3320 is configured. Figure 6 shows the flow between the initialization, configuration, and start-up states. Figure 9 gives the general timing information for configuring the device.

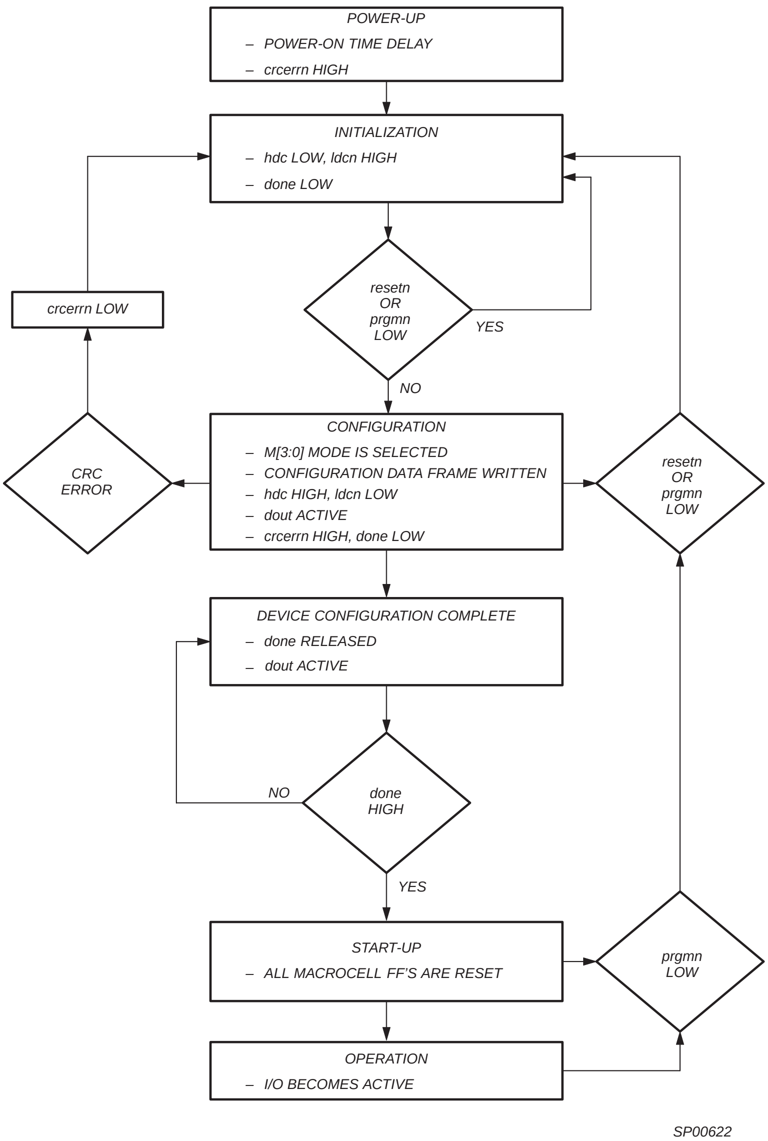


Figure 8: Chart Of Initialization, Configuration, and Operating States

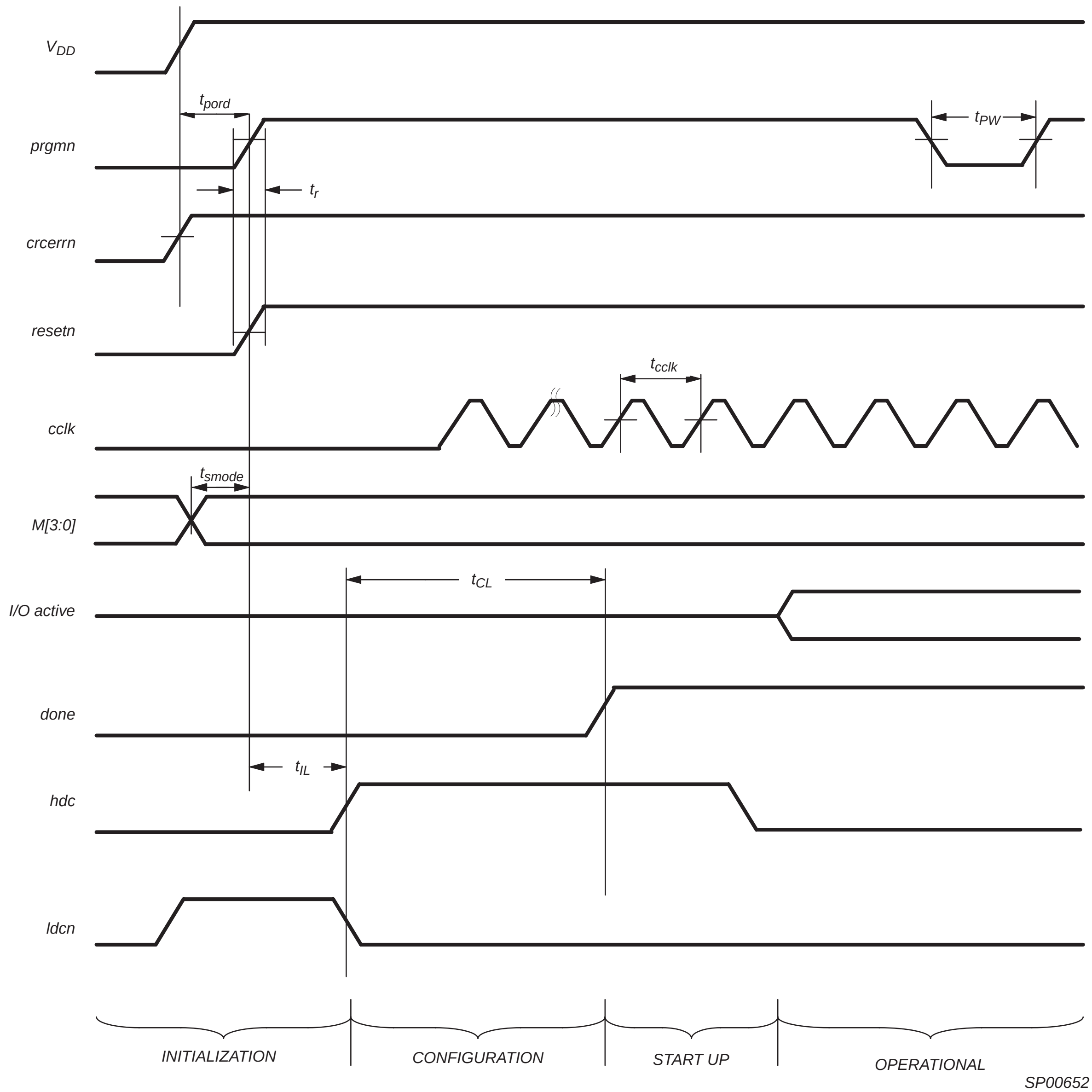


Figure 9: General Configuration Mode Timing Diagram

Table 3: General Configuration Mode Timing Characteristics

Symbol	Parameter		Min.	Max.	Unit
All Configuration Modes					
t_{SMODE}	M[3:0] setup time to prgmn high		0	-	ns
t_{HMODE}	M[3:0] hold time from done high		10	-	ms
t_{PW}	prgmn pulse width low		50	-	ns
t_{gtsr}	Global 3-state disable			40	ns
t_{IL}	Initialization latency (prgmn high to hdc high) XCR3320	M3 = 1	250	700	ns
t_{PORD}	Power-on reset delay		1		ms
t_r	Configuration signal rise time		-	1.0	ms
Master Modes					
t_{CCLK}	cclk period	M3 = 1	714	1667	ns
t_{CL}	Configuration latency (non-compressed) XCR3320	M3 = 1	135	316	ms
Slave Serial, Slave Parallel, And Synchronous Peripheral Modes					
t_{CCLK}	cclk period	Single device	100	-	ns
		Daisy-chain	1000	-	ns
t_{CL}	Configuration latency (non-compressed) XCR3320	Single device	19	-	ms
		Daisy-chain	189	-	ms

Initialization

Upon power-up, the device goes through an initialization process. First, an internal power-on-reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the XCR3320 begin to operate (1.5V), the configuration pins are set to be inputs or outputs based on the configuration mode, as determined by the mode select inputs M[2:0]. The mode pins must be stable t_{SMODE} nanoseconds before the rising edge of prgmn or resetn. A time-out delay is initiated when V_{CC} reaches between 1.0V and 2.0V to allow the power supply voltage to stabilize. The done output is low. At power-up, if the power supply does not rise from 1.0V to V_{CC} in less than 25 ms, the user should delay configuration by inputting a low into prgmn or resetn until V_{CC} is greater than the recommended minimum operating voltage (3.0V for commercial devices). If prgmn has a rise time of greater than one microsecond, resetn must be held low until after prgmn goes high. If the rise time for prgmn is 1 ms or less, the order in which these pins go high is arbitrary.

The High During Configuration (hdc), Low During Configuration (ldcn), and done signals are active outputs in the XCR3320's initialization and configuration states. hdc, ldcn, and done can be used to provide control of external logic signals such as reset, bus enable, or EEPROM enable during configuration. For master parallel configuration mode, these signals provide EEPROM enable control and allow the data pins to be shared with user logic signals.

If configuration has begun, an assertion of resetn or prgmn initiates an abort, returning the XCR3320 to the initialization state. The resetn and prgmn pins must be high before the XCR3320 will enter the configuration state, and the mode pins must be stable t_{SMODE} nanoseconds before they rise. During the start-up and operating states, only the assertion of prgmn causes a reconfiguration.

During initialization and configuration, all I/O's are 3-stated and the internal weak pull-downs are active. See "Terminations" on page 8 for more information.

Start-up

After configuration, the XCR3320 enters the start-up phase. This phase is the transition between the configuration and operational states. This transition occurs within three cclk cycles of the done pin going high (it is acceptable to have additional cclk cycles beyond the three required). The system design task in the start-up phase is to ensure that multi-function pins (See "230-pin Function Table" on page 36.) transition from configuration signals to user definable I/Os without inadvertently activating devices in the system or causing bus contention. The done signal goes High at the beginning of the start up phase, which allows configuration sources to be disconnected so that there is no bus contention when the I/Os become active. In addition to controlling the XCR3320 during start-up, additional start-up techniques to avoid contention include using isolation devices between the XCR3320 and other circuits in the system, re-assigning I/O locations, and keeping I/Os 3-stated until contentions are resolved. For example, Figure 10 shows how to use the Global 3-state (GTS) signal to avoid signal contention when any multi-function pins

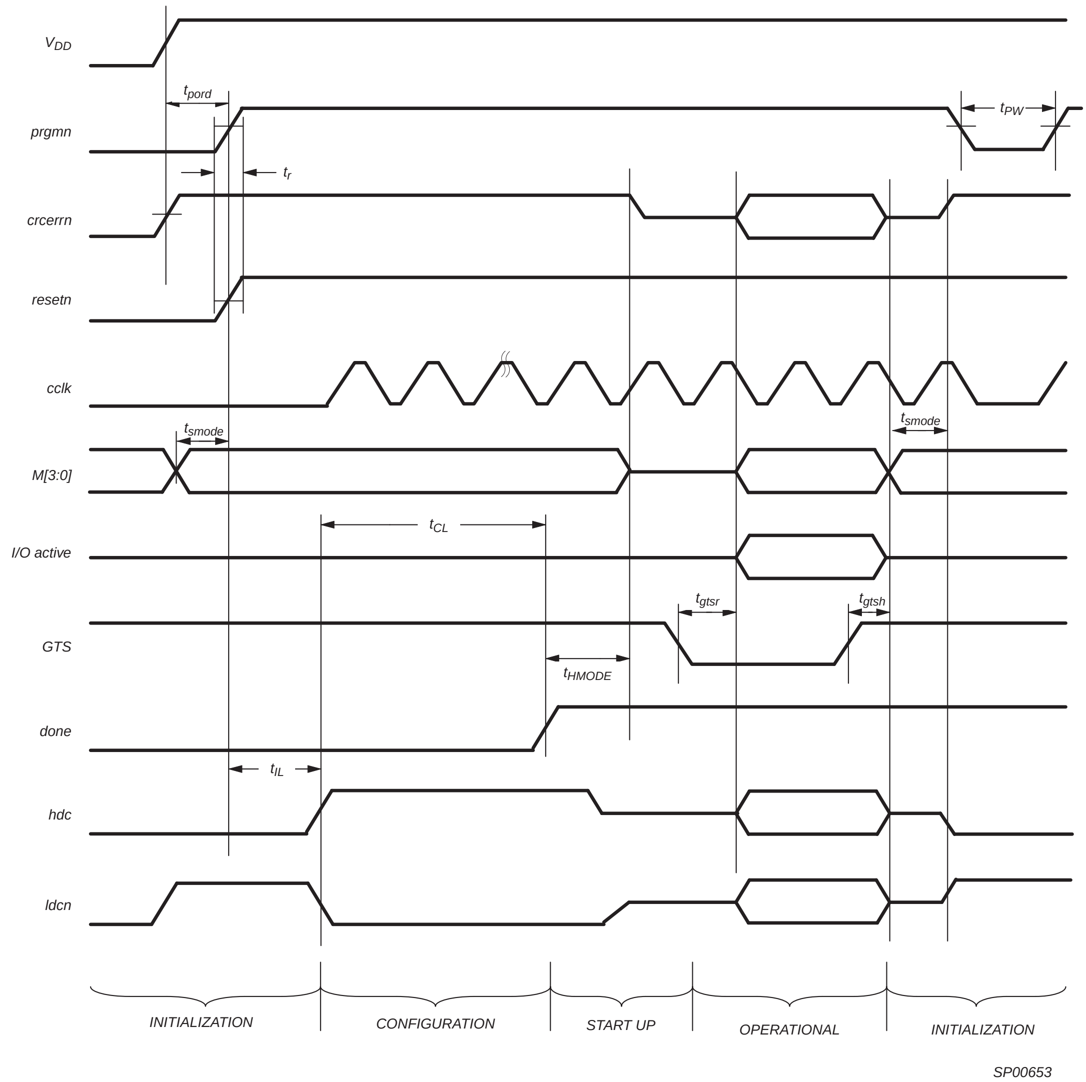


Figure 10: Using GTS Signal with Power Up to Avoid Signal Contention with Multi-function Pins Used as I/O

are used as I/O after configuration is finished. Holding gts high until after the multi-function pins are disconnected from the driving source allows these pins to transition from configuration pins to user definable I/O without signal contention. In this case, the I/O become active a t_{GTSR} delay after the gts pin is pulled low.

The flip-flops are reset one cycle after done goes high so that operation begins in a known state. The done outputs from multiple XCR3320s can be wire ANDed and used as an active-high ready signal, to disable PROMs with active-low enable(s), or to reset to other parts of the system (see Figure 27).

Configuration Data Format Overview

The XCR3320 functionality is determined by the state of internal configuration RAM. This section discusses the configuration data format, and the function of each field in configuration data packets.

Configuration Data Packets

Configuration of the XCR3320 is done using configuration packets. The configuration packet is shown in Figure 11. The data packet consists of a header and a data frame. There are four types of data frames. The header is shifted into the device first, followed by one data frame. Configuration of a single XCR3320 requires 338 data packets, one for each address. All preceding data must contain only 1's. Once a device is configured, it retransmits data of any polarity. Before and during configuration, all data retransmitted out the daisy-chain port (dout) are 1's.

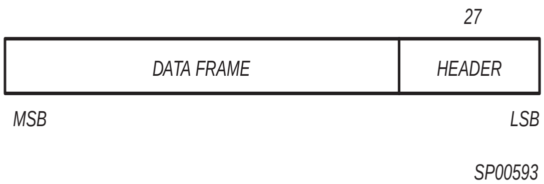


Figure 11: Data Packet

The ordering of the data packets may be random, but they cannot be mixed with other devices' data packets. Alignment bits are not required between data packets. If used, alignment bits must be included in the length count, and they must be at least 2-bits long.

Table 4: Configuration Frame Size

Device	XCR3320
Number of frames	338
Data bits/standard frame	560
Data bits/compressed frame	14
Data bits/user_code frame	560
Data bits/isc_code frame	560
Maximum configuration data – # bits/frame x # frames	189280

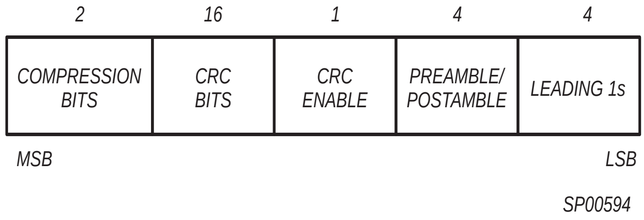


Figure 12: 27-bit Header

The header is fixed and consists of five fields:

- Leading 1s,
- Preamble,
- CRC Enable,
- CRC Bits,
- Compression Bits.

The leading 1s enter the device first. The following is a description of each field in the header.

Leading 1s:
This is a four or greater bit field consisting of 1s.

Preamble/Postamble:
This is a four bit field which indicates the start of a frame or the end of configuration:
Preamble: -0010 - signals the beginning of a configuration data packet.
Postamble: 0100 -signals the end of configuration.
All other values of the preamble field force configuration of the entire system to restart.

The segments CRC Enable, CRC Bits, and Compression Bits are valid only if the Preamble field is 0010.

Cyclic Redundancy Check (CRC) Enable:
In this single bit field, a 0 disables CRC checking of the data stream. If the CRC is disabled the 16 bit CRC field must be the default described below. A1 enables CRC error checking of the data stream.

CRC Error Checking:
The CRC field is a 16 bit field. The default value is 1010_1010_1010_1010. The calculated value is from data, address, stop bit, and first alignment bit (starting with crc_reg[15:0] = [0]). Using verilog operators, the crc is calculated as:

```
crc_reg[14:2] <= cr_reg[14:2] << 1;
cr_reg[2] <= cr_reg[15]^din^cr_reg[1];
cr_reg[1] <= cr_reg[0];
cr_reg[0] < cr_reg[15]^din;
cr_reg[15] <= cr_reg[15]^din^cr_reg[14];
```

If a CRC error is detected, configuration is halted and must be restarted.

Compression Bits:

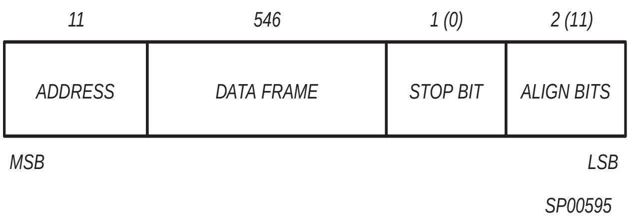
This 2-bit field defines the use of compression of the data packets.

00 - Standard mode:
The data packet contains both address and data
01 - Reset mode:
The data packet contains only the address field. This pattern causes the configuration register to be reset.
10 - Hold mode:
The data packet contains only the address field. This pattern causes the configuration register to hold its value.
11 - Set mode:
The data packet contains only the address field. This pattern causes the configuration register to be set.

Data Frames

The four types of data frames are standard, compressed, user_code, and isc_code. All fields must be completely filled, with 1s used to fill unused bits. The definition of each frame is described below:

Standard Frame



igure 13: Standard Frame

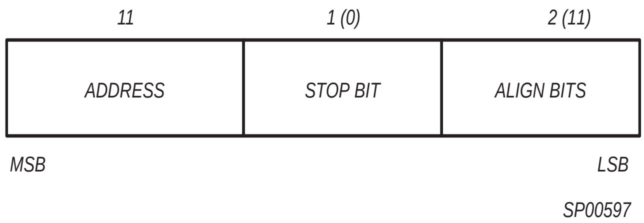
Address:
This is an 11 bit field for providing 338 (336 SRAM plus 2user) addresses.

Data:
546 bit field.

Stop bit:
This is a one bit field which must be 0.

Align bit:
This is a two bit field which must be 11.

Compressed Frame



igure 14: Compressed Frame

The compressed frame contains no data.

User Code Frame

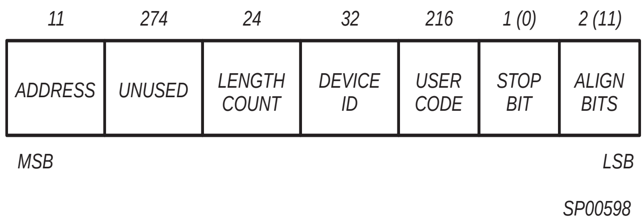


Figure 15: User Code Frame

The user code is located at address 336.

Length Count:
This is a 24 bit field containing the length of the data stream transmitted to configure all of the devices in the daisy chain. This field is only used by a XCR3320 if it is in the master mode.

Device ID:
This is a 32-bit field containing XCR3320 device ID: 0000_001_001_010000_1_000_00000010101_1

User Code:
This is a 216 bit field reserved for user information.

ISC Code Frame

The isc_code address is 337.

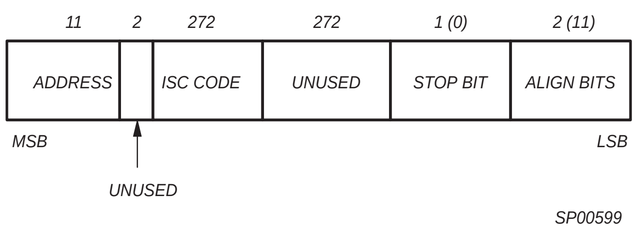


Figure 16: ISC Frame

The ISC frame allows the user to write an ISC code to the device.

Reconfiguration

To reconfigure the XCR3320 when the device is operating in the system, a low pulse is input into prgmn. The I/Os not used for configuration are 3-stated. The XCR3320 then samples the mode select inputs and begins re-configuration. The mode pins are continuously sampled, so the signals must be stable while prgmn is low. When configuration is compete, done is released, allowing it to be pulled high.

CRC Error Checking

CRC checking is done on each frame if enabled by setting the CRCen bit in the header. If there is an error, a CRC error is flagged by pulling crcerrn low. The XCR3320 is forced into the initialization state, and then moves into the configuration state after prgmn and resetn go high. The XCR3320 will also pull crcerrn low if an invalid preamble is detected within a configuration data packet.

XCR3320 Configuration Modes

The method for configuring the XCR3320 is selected by the m0, m1, and m2 inputs. The m3 input should be high for all modes. In master modes, cclk is an output with a nominal frequency of 1 MHz. In slave modes, cclk is an input with a maximum frequency of 10 MHz if configuring only a single device, and 1 MHz if devices are daisy chained.

Master Serial Mode

In the master serial mode, the XCR3320 loads the configuration data from an external serial ROM. The configuration data is either loaded automatically at start-up or on a command to reconfigure. Serial EEPROMs from Altera, Atmel, Lucent, Microchip, and Xilinx can be used to configure the XCR3320 in the master serial mode. This provides a simple four-pin interface in an eight-pin package. Serial EEPROMs are available in 32K, 64K, 128K, 256K, and 1M bit densities.

Configuration in the master serial mode can be done at power-up and/or upon a configure command. The system or the XCR3320 must activate the serial EEPROM's $\overline{\text{RESET}}$/OE and $\overline{\text{CE}}$ inputs. At power-up, the XCR3320 and serial EEPROM each contain internal power-on reset circuitry which allows the XCR3320 to be configured without the system providing an external signal. The power-on reset circuitry causes the serial EEPROMs' internal address pointer to be reset. After power-up, the XCR3320 automatically enters its initialization phase.

The serial EEPROM/XCR3320 interface used depends on such factors as the availability of a system reset pulse, availability of an intelligent host to generate a configure command, whether a single serial EEPROM is used or multiple serial ROMs are cascaded, whether the serial EEPROM contains a single or multiple configuration programs, etc.

Data is read into the XCR3320 sequentially from the serial ROM. The DATA output from the serial EEPROM is connected directly into the din input of the XCR3320. The cclk output from the XCR3320 is connected to the CLOCK input of the serial EEPROM. During the configuration process, cclk clocks one data bit into the XCR3320 on each rising edge.

Since the data and clock are direct connects, the XCR3320/serial EEPROM interface task is to use the system or XCR3320 to enable the $\overline{\text{RESET}}$/OE and $\overline{\text{CE}}$ of the serial EEPROM(s). The serial EEPROM's $\overline{\text{RESET}}$/OE is programmable to function with $\overline{\text{RESET}}$ active-low and OE active-high, which allows hdc from the XCR3320 to control this function.

Likewise, the serial EEPROM could be programmed to function with RESET active high and $\overline{\text{OE}}$ active low, allowing the ldcn pin from the XCR3320 to control this function. The XCR3320 done pin is connected to the serial EEPROM $\overline{\text{CE}}$ to enable the EEPROMs during configuration and disable them when configuration is complete.

In Figure 17, the serial EEPROMs $\overline{\text{RESET}}$/OE pin has been programmed to function with $\overline{\text{RESET}}$ active low and OE active high, and it is controlled by the XCR3320's hdc pin. This resets the serial EEPROMs during the initialization state and enables their output during the configuration state. If a bit error is found during configuration, hdc will go low, signifying the XCR3320 is back in initialization state and also resetting the EEPROMs. This restarts the configuration process.

The XCR3320 done pin is routed to the $\overline{\text{CE}}$ pin of the EEPROMs. The Low signal on done during configuration enable the serial EEPROMs. At the completion of configuration, the High on done disables the EEPROMs.

In Figure 17, a serial EEPROM is programmed to configure a XCR3320. When configuration data requirements exceed the capacity of a single serial EEPROM, multiple serial EEPROMs can be cascaded to support the configuration of a single (or multiple) XCR3320(s). After the last bit from the first serial ROM is read, the serial ROM outputs $\overline{\text{CEO}}$ Low and 3-states the DATA output. The next serial ROM recognizes the Low on $\overline{\text{CE}}$ input and outputs configuration data on the DATA output. After configuration is complete, the XCR3320's done output into $\overline{\text{CE}}$ disables the serial EEPROMs.

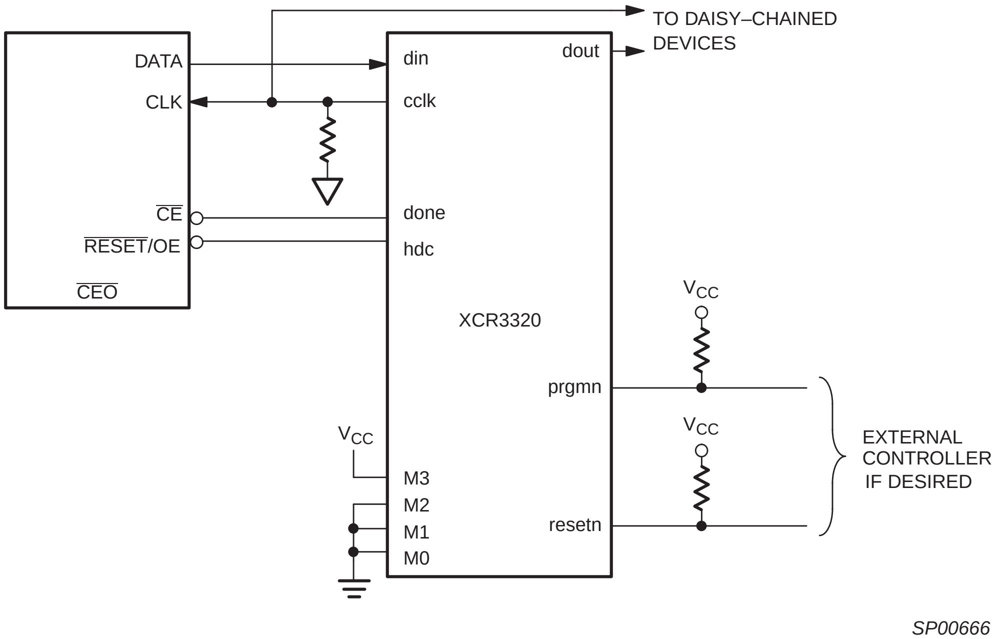


Figure 17: Master Serial Configuration

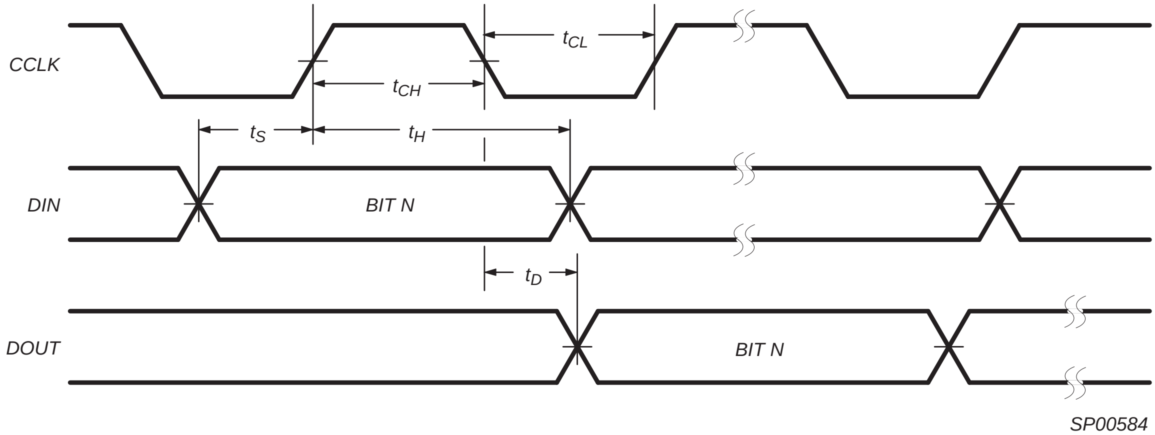


Figure 18: Master Serial Configuration Mode Timing Diagram

Table 5: Master Serial Configuration Mode Timing Characteristics

Symbol	Parameter	Min.	Nom.	Max.	Unit
t_S	din setup time	60	-	-	ns
t_H	din hold time	0	-	-	ns
t_D	cclk to dout delay	-	-	300	ns
t_{CL}	cclk low time (M3 = 1)	357	500	833	ns
t_{CH}	cclk high time (M3 = 1)	357	500	833	ns
t_C	cclk frequency (M3 = 1)	0.6	1.0	1.4	MHz

In applications in which a serial EEPROM stores multiple configuration programs, the subsequent configuration program(s) are stored in EEPROM locations that follow the last address for the previous configuration program. The user must ensure that the serial EEPROMs address pointer is not reset, causing the first device configuration to be reloaded.

Contention on the XCR3320's din pin must be avoided. During configuration, din receives configuration data. After configuration, it is a user I/O.

Master Parallel Mode

The master parallel configuration mode is generally used to interface to industry-standard byte-wide memory such as 256K and larger EEPROMs. Figure 19 provides the interface for master parallel mode. The XCR3320 outputs a 20-bit address on A[19:0] to memory and reads one byte of configuration data every eighth cclk. The parallel bytes are internally serialized starting with the least significant bit, D0. The starting memory address is 00000 Hex and the XCR3320 increments the address for each byte loaded. The starting address is output when the device enters the configuration state. The XCR3320 latches the data byte on the second rising edge of cclk. This next data byte is latched in the XCR3320 seven cclk cycles later.

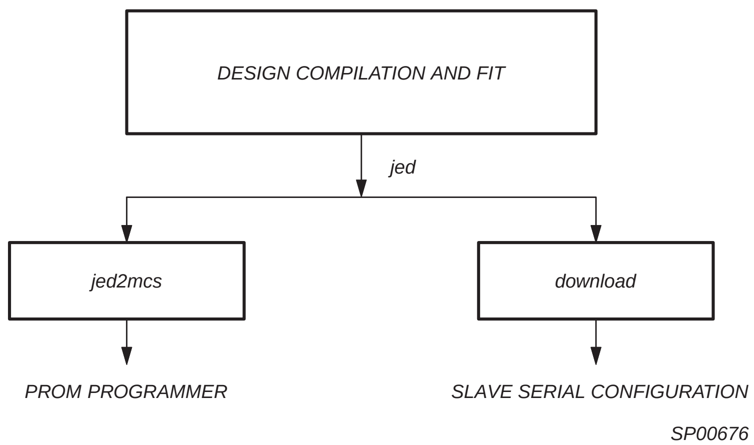


Figure 19: Master

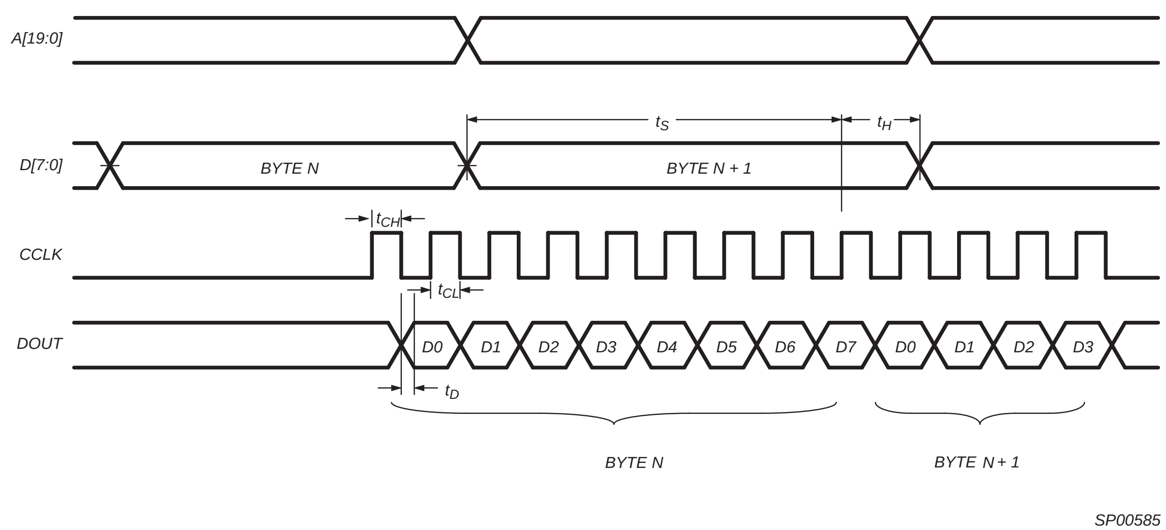


Figure 20: Master Parallel Configuration Mode Timing Diagram

.

Table 6: Master Parallel Configuration Mode Timing Characteristics

Symbol	Parameter		Min.	Nom.	Max.	Unit
t_{AV}	cclk to address valid		0	-	200	ns
t_S	D[7:0] setup time to cclk high		60		-	ns
t_H	D[7:0] hold time from cclk high		0		-	ns
t_{CL}	cclk low time	M3 = 1	357	500	833	ns
t_{CH}	cclk high time	M3 = 1	357	500	833	ns
t_D	cclk to dout delay		-		300	ns
f_C	cclk frequency	M3 = 1	0.6	1.0	1.4	MHz

Synchronous Peripheral Mode

In the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the cclk input. The first data byte is clocked in on the second cclk after hdc goes high. Subsequent data bytes are clocked in on every eighth rising edge of cclk. The process repeats until all of the data is loaded into the XCR3320. The serial data begins shifting out on dout 0.5 cycles after the parallel data was loaded. It requires additional cclks after the last byte is loaded to complete the shifting. Figure 21 shows the interface for synchronous peripheral mode. When configuring a single device, the frequency of cclk can be up to 10 MHz. As with master modes, this mode can be used for the lead XCR3320 for daisy-chained devices. Note that the cclk frequency for daisy-chained operation is limited to 1 MHz.

Also note that CS1 is a multi-function pin, which means that it is available as a user I/O during normal device operation. As with all user I/O on the XCR3320, CS1 has an internal pull-down resistor that is automatically activated if the I/O pin is not used (see "Terminations" on page 8 for more information). If CS1 is left attached to V_{CC} after configuration, and it is not used as an I/O, the internal pull-down must be disabled or a path from V_{CC} to ground is created. To disable the pull-down, use the XPLA property statement `'signal name:pin number tri-state'` to disable the resistor.

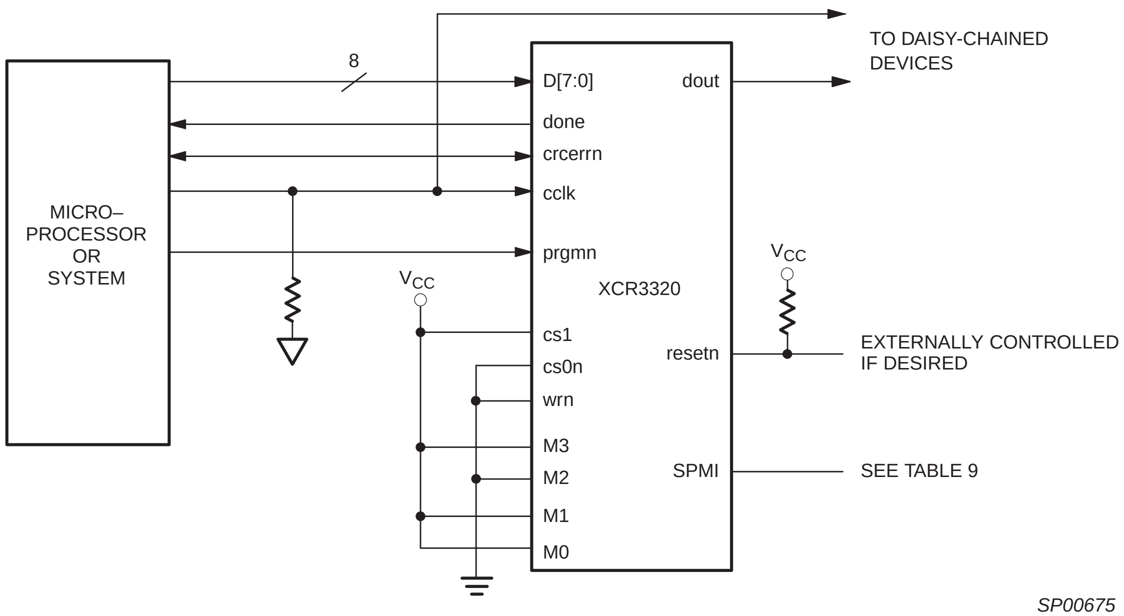


Figure 21: Synchronous Peripheral Configuration

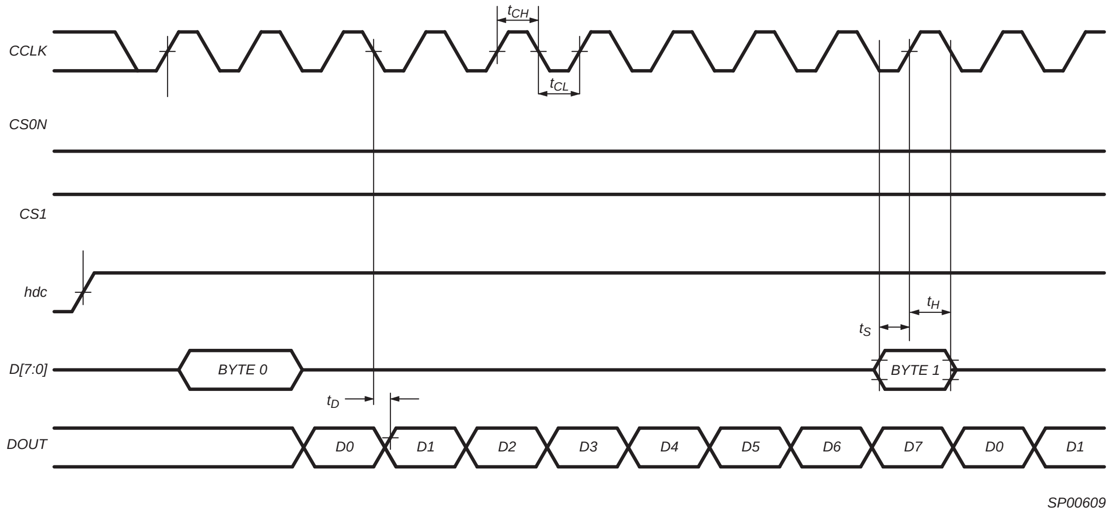


Figure 22: Synchronous Peripheral Configuration Mode Timing Diagram

Table 7: Synchronous Peripheral Configuration Mode Timing Characteristics

Symbol	Parameter		Min.	Max.	Unit
t_S	D[7:0] setup time		20	0	ns
t_H	D[7:0] hold time		0	-	ns
t_{CH}	cclk high time	Single device	50	-	ns
		Daisy-chain device	500	-	ns
t_{CL}	cclk low time	Single device	50	-	ns
		Daisy-chain device	500	-	ns
f_C	cclk frequency	Single device	-	10	MHz
		Daisy-chain device	-	1	MHz

Slave Serial Mode

Figure 23 shows the interface for the slave serial configuration mode. The configuration data is provided into the XCR3320's din input synchronous with the cclk input. After the XCR3320 has loaded its configuration data, it re-transmits incoming configuration data on dout. When configuring a single device, the frequency of cclk can be up to 10 MHz.

A device in slave serial mode can be used as the lead device in a daisy-chain. When used in daisy-chained operation, cclk is routed into all slave serial mode devices in parallel and the frequency is limited to 1 MHz. The dout pin of the lead device is connected to the din pin of the next device and so on. In daisy-chained operation, all downstream devices use slave serial mode regardless of the configuration mode of the lead device.

Multiple slave XCR3320s can be loaded with identical configurations simultaneously. This is done by loading the configuration data into the din inputs in parallel.

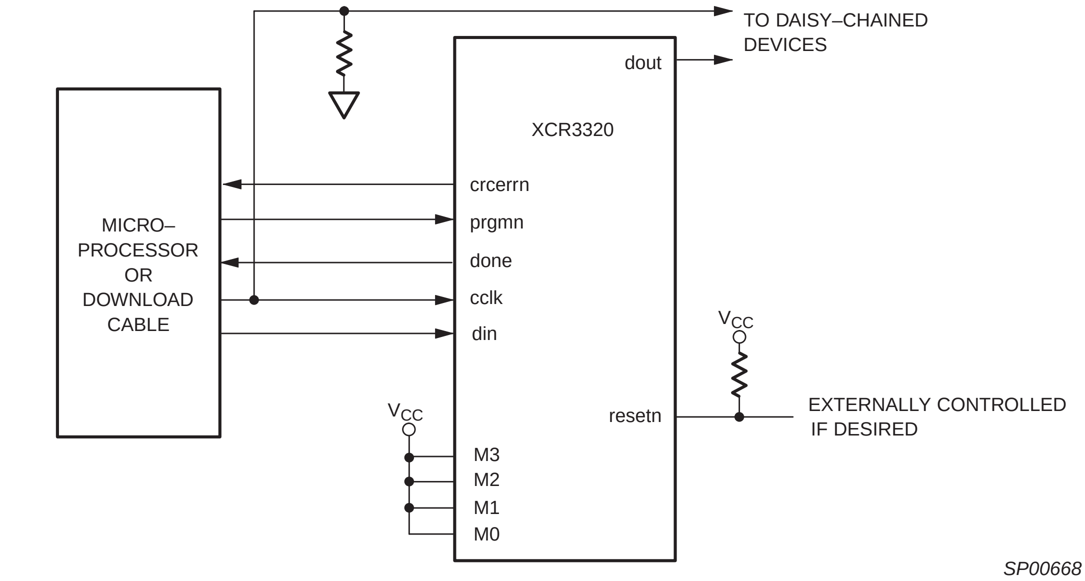


Figure 23: Slave Serial Configuration Schematic

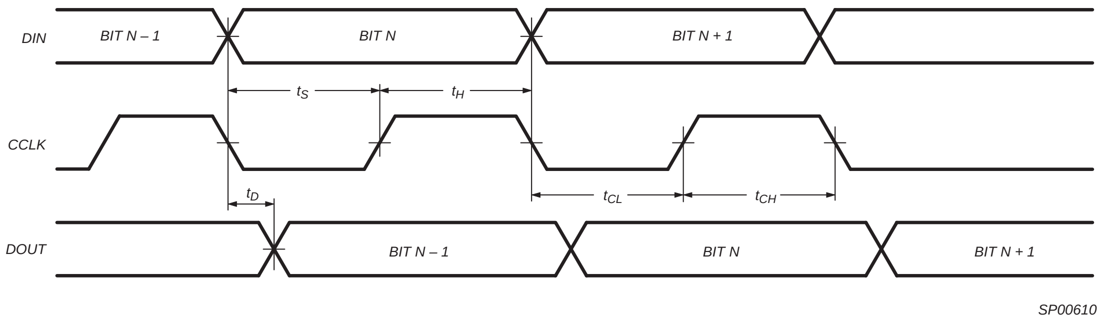


Figure 24: Slave Serial Configuration Mode Timing Diagram

Table 8: Slave Serial Configuration Mode Timing Characteristics

Symbol	Parameter		Min	Max.	Unit
t_S	din setup time		20	0	ns
t_H	din hold time		0	-	ns
t_{CH}	cclk high time	Single device	50	-	ns
		Daisy-chain device	500	-	ns
t_{CL}	cclk low time	Single device	50	-	ns
		Daisy-chain device	500	-	ns
f_C	cclk frequency	Single device	-	10	MHz
		Daisy-chain device	-	1	MHz

Slave Parallel Mode

The slave parallel mode is essentially the same as the synchronous peripheral mode, except that the chip select pins (cs1 and cs0n) are not used. As in the synchronous peripheral mode, byte-wide data is input into D[7:0] on the rising edge of the cclk input. The first data byte is clocked in on the second cclk after hdc goes High. Subsequent data bytes are clocked in on every eighth rising edge of cclk. The process repeats until all of the data is loaded into the XCR3320. The serial data begins shifting out on dout 0.5 cycles after the parallel data was loaded. It requires additional cclks after the last byte is loaded to complete the shifting. Figure 25 shows the interface for slave parallel mode. When configuring a single device, the frequency of cclk can be up to 10 MHz.

As with synchronous peripheral mode, the slave parallel mode can be used as the lead XCR3320 for daisy-chained devices. Note that the cclk frequency for daisy-chain operation is limited to 1 MHz.

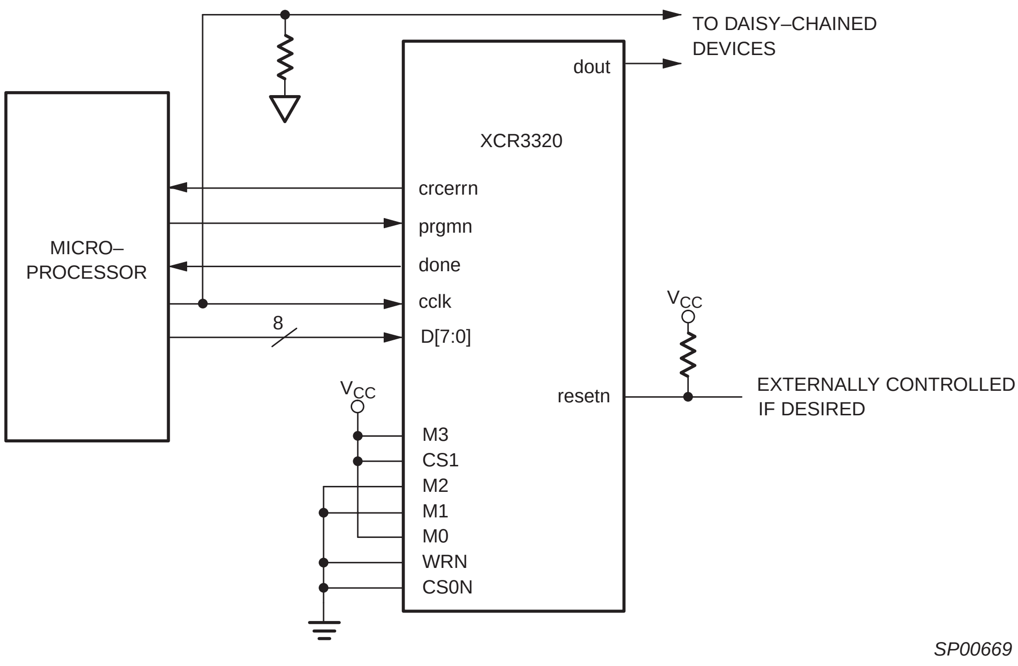


Figure 25: Slave Parallel Configuration Schematic

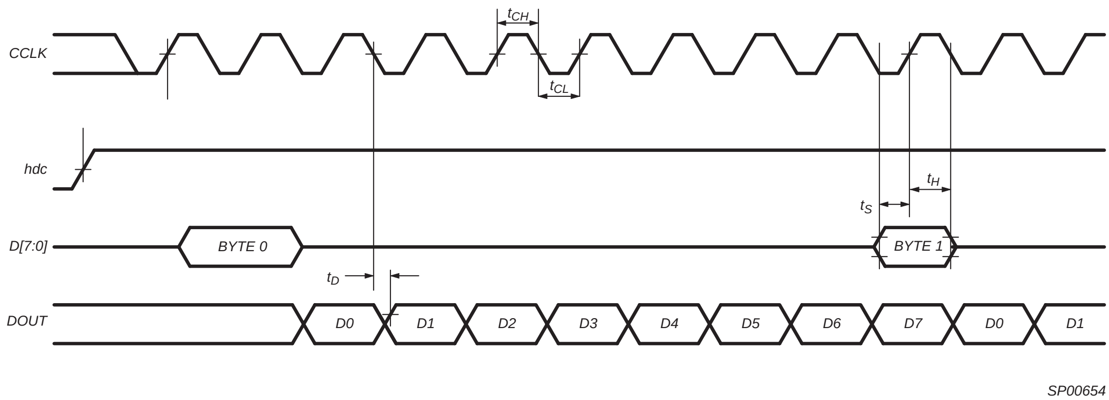


Figure 26: Slave Parallel Configuration Mode Timing Diagram

Table 9: Slave Parallel Configuration Mode Timing Characteristics

Symbol	Parameter		Min.	Max.	Unit
t_S	D[7:0] setup time		20	0	ns
t_H	D[7:0] hold time		0	-	ns
t_{CH}	cclk high time	Single device	50	-	ns
		Daisy-chain device	500	-	ns
t_{CL}	cclk low time	Single device	50	-	ns
		Daisy-chain device	500	-	ns
f_C	cclk frequency	Single device	-	10	MHz
		Daisy-chain device	-	1	MHz

Daisy Chain Operation

Multiple XCR3320s can be configured by using a daisy-chain of XCR3320s. Daisy-chaining uses a lead XCR3320 and one or more XCR3320s configured in slave serial mode. The lead XCR3320 can be configured in any mode. Figure 27 shows the connections for loading multiple XCR3320s in a daisy-chain configuration with the lead devices configured in master parallel mode. Figure 28 shows the connections for loading multiple XCR3320's with the lead device configured in master serial mode.

Daisy-chained XCR3320s are connected in series. An upstream XCR3320 which has received the preamble outputs a high on dout, ensuring that downstream XCR3320s do not receive frame start bits. When the lead device receives the postamble, its configuration is complete. At this point, the configuration RAM of the lead device is full and its done pin is released. The lead device continues to load configuration data until the internal frame bit counter reaches the length count or all the done pins of the chain have gone high. Since the configuration RAM of the lead device is full, this data is shifted out serially to the downstream devices on the dout pin. As the configuration is completed for the downstream devices, each will release its done pin. Because the done pins of each device in the chain are wire-anded together, the done pin will be pulled high when all devices in the daisy-chain have completed configuration. All devices now move to the start-up state simultaneously.

The generation of cclk for the daisy-chained devices which are in slave serial mode differs depending on the configuration mode of the lead device. A master parallel mode device uses its internal timing generator to produce an internal cclk. If the lead device is configured in either synchronous peripheral, slave serial mode, or slave parallel mode, cclk is an input and is mated to the lead device and to all of the daisy-chained devices in parallel. The configuration data is read into din of slave devices on the positive edge of cclk, and shifted out dout on the negative edge of cclk. Note that daisy-chain operation is limited to a cclk frequency of 1 MHz. If a CRC error or an invalid preamble is detected by a slave device, crcerrn will be pulled low and in turn pull prgmn low, halting configuration for all devices. If a CRC error is detected by the master device, hdc will be pulled low, resetting the EEPROM to the first address and restarting configuration.

The development software can create a composite configuration file for configuring daisy-chained XCR3320s. The configuration data consists of multiple concatenated data packets.

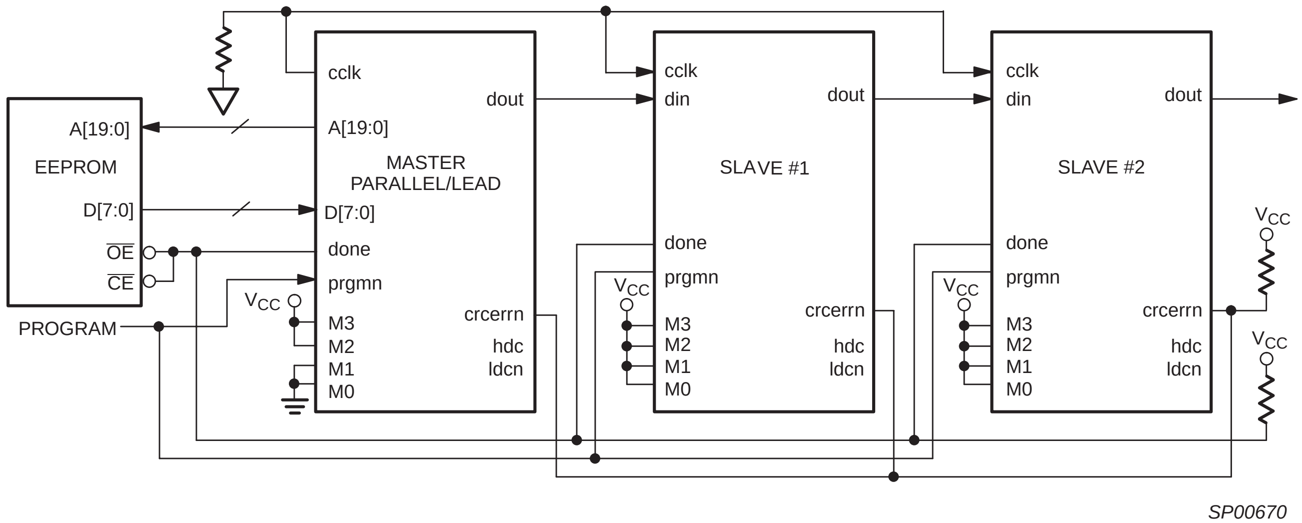


Figure 27: Daisy-Chain Schematic with Lead Device in Master Parallel

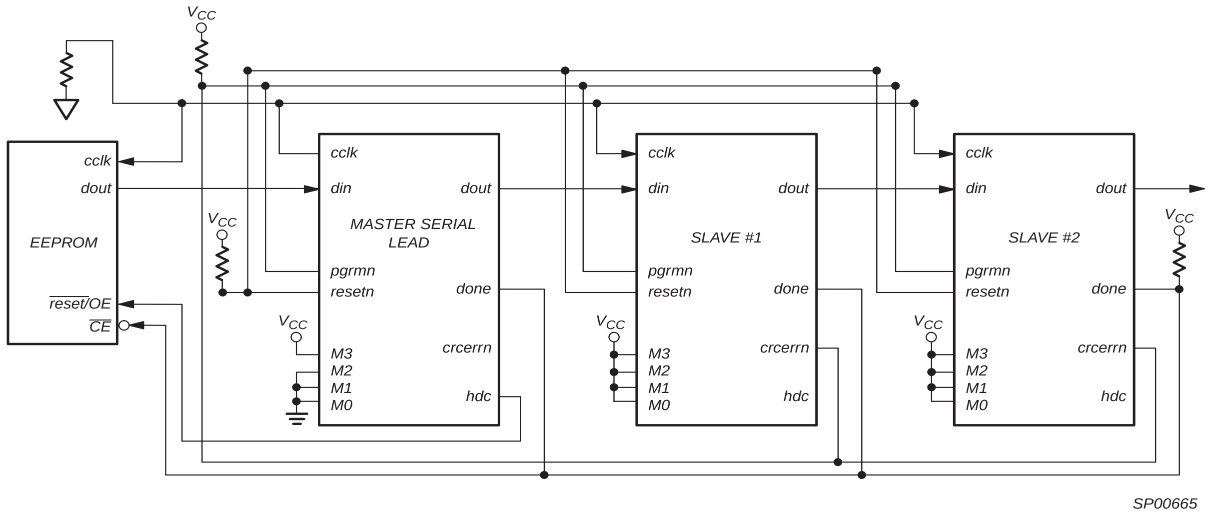


Figure 28: Daisy Chain Schematic with Master Serial Lead Device

JTAG Testing Capability

JTAG is the commonly-used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands which facilitate both board and device level testing without the use of specialized test equipment. BST provides the ability to test the external connections of a device, test the internal logic of the device, and capture data from the device during normal operation. BST provides a number of benefits in each of the following areas:

- Testability
  - Allows testing of an unlimited number of interconnects on the printed circuit board
  - Testability is designed in at the component level
  - Enables desired signal levels to be set at specific pins (Preload)
  - Data from pin or core logic signals can be examined during normal operation
- Reliability
  - Eliminates physical contacts common to existing test fixtures (e.g., “bed-of-nails”)
  - Degradation of test equipment is no longer a concern
  - Facilitates the handling of smaller, surface-mount components
  - Allows for testing when components exist on both sides of the printed circuit board
- Cost
  - Reduces/eliminates the need for expensive test equipment
  - Reduces test preparation time
  - Reduces spare board inventories

The Xilinx XCR3320's JTAG interface includes a TAP Port and a TAP Controller, both of which are defined by the IEEE 1149.1 JTAG Specification. As implemented in the Xilinx XCR3320, the TAP Port includes five pins (refer to Table 10) described in the JTAG specification: t_{CK}, t_{MS}, t_{DI}, t_{DO}, and t_{RSTN}. These pins should be connected to an external pull-up resistor to keep the JTAG signals from floating when they are not being used.

Table 11 defines the dedicated pins used by the mandatory JTAG signals for the XCR3320.

The JTAG specifications define two sets of commands to support boundary-scan testing: high-level commands and low-level commands. High-level commands are executed via board test software on an a user test station such as automated test equipment, a PC, or an engineering workstation (EWS). Each high-level command comprises a sequence of low level commands. These low-level commands are executed within the component under test, and therefore must be implemented as part of the TAP Controller design. The set of low-level boundary-scan commands implemented in the XCR3320 is defined in Table 11. By supporting this set of low-level commands, the XCR3320 allows execution of all high-level boundary-scan commands.

Table 10: JTAG Pin Description

Pin	Name	Description
tck	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the tdi and tdo pins, respectively. tck is also used to clock the TAP Controller state machine.
tms	Test Mode Select	Serial input pin selects the JTAG instruction mode. tms should be driven high during user mode operation.
tdi	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of tck.
tdo	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of tck. The signal is tri-stated if data is not being shifted out of the device.
trstn	Test Reset	Forces TAP controller to test logic reset state. This signal is active low.

Table 11: XCR3320 JTAG Pinout by Package Type

Device: XCR3320	(Pin Number / Macrocell #)				
	t_{CK}	t_{MS}	t_{DL}	t_{DO}	t_{RSTN}
256-pin PBGA	V4	W4	U5	Y4	L18
160-pin LQFP	41	43	42	44	97

Table 12: XCR3320 Low-Level JTAG Boundary-Scan Commands

Instruction (Instruction Code) Register Used	Description
SAMPLE/PRELOAD (00010) Boundary-Scan Register	The mandatory SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the Boundary-Scan Shift-Register prior to selection of the other boundary-scan test instructions.
EXTEST (00000) Boundary-Scan Register	The mandatory EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of Boundary-Scan Shift-Register using the SAMPLE/PRELOAD instruction prior to selection of the EXTEST instruction.
BYPASS (11111) Bypass Register	Places the 1-bit bypass register between the tdi and tdo pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The BYPASS instruction can be entered by holding tdi at a constant high value and completing an Instruction-Scan cycle.
IDCODE (00001) Boundary-Scan Register	Selects the IDCODE register and places it between tdi and tdo, allowing the IDCODE to be serially shifted out of tdo. The IDCODE instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.
HIGHZ (00101) Bypass Register	The HIGHZ instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component. The HIGHZ instruction also forces the Bypass Register between tDI and tDO.
INTEST (00011) Boundary-Scan Register	The INTEST instruction allows testing of the on-chip system logic while the component is assembled on the board. The boundary-scan register is connected between TDI and TDO. Using the INTEST instruction, test stimuli are shifted in one at a time and applied to the on-chip system logic. The test results are captured into the boundary-scan register and are examined by subsequent shifting, Data would typically be loaded onto the latched parallel outputs of boundary-scan shift-register stages using the SAMPLE/PRELOAD instruction prior to selection of the INTEST instruction. NOTE: Following use of the INTEST instruction, the on-chip system logic may be in an indeterminate state that will persist until a system reset is applied. Therefore, the on-chip system logic may need to be reset on return or normal (i.e., non-test) operation.

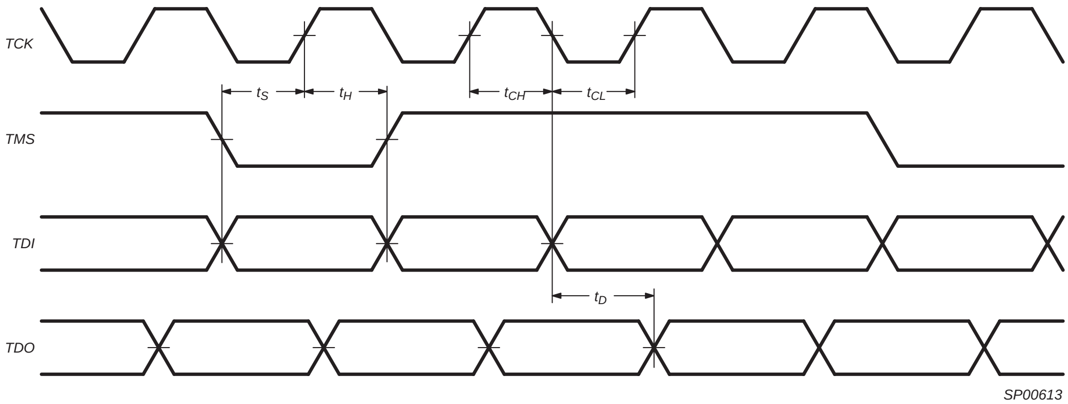


Figure 29: Boundary Scan Timing Diagram

Table 13: Boundary Scan Timing Characteristics

Symbol	Parameter	Min	Max.	Unit
t_S	tdi/tms to tck setup time	20	-	ns
t_H	tdi/tms from tck hold time	0	-	ns
t_{CH}	tck high time	50	-	ns
t_{CL}	tck low time	50	-	ns
f_{TCK}	tck frequency	-	10	MHz
t_D	tck to tdo delay	-	35	ns

Device Configuration Through JTAG

In addition to the normal configuration modes, the XCR3320 can also be configured through the JTAG port. This feature is very useful for design prototyping and debug before the device is put into the final product. In System Configuration of the XCR3320 is supported by Xilinx PC-ISP software. Table 14 shows the ISC commands supported by the XCR3320

To configure the device through the JTAG port, mode pins M0, M1, and M2 should all be held low. M3, as always, should be high and the JTAG pins should be terminated as described in *"Terminations" on page 8* of this data sheet.

Table 14: Low Level ISP Commands

Instruction (Register Used)	Instruction Code	Description
Enable (ISP Shift Register)	1001	Enables the Erase, Program, and Verify commands. Using the ENABLE instruction before the Erase, Program, and Verify instructions allows the user to specify the outputs the device using the JTAG Boundary-Scan SAMPLE/PRELOAD command.
Erase (ISP Shift Register)	1010	Erases the entire EEPROM array. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.
Program (ISP Shift Register)	1011	Programs the data in the ISP Shift Register into the addressed EEPROM row. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.
Verify (ISP Shift Register)	1100	Transfers the data from the addressed row to the ISP Shift Register. The data can then be shifted out and compared with the JEDEC file. The outputs during this operation can be defined by the user.

Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max.	Unit
V_{CC}	Supply voltage	-0.5	4.6	V
V_{IN}	Input voltage	-1.2	5.75	V
V_{OUT}	Output voltage	-0.5	V_{CC} +0.5	V
I_{IN}	Input current	-30	30	mA
T_J	Junction temperature range	-40	150	°C
T_{STG}	Storage temperature range	-65	150	°C

Note:

1. Stresses above these listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.

Operating Range

Product Grade	Temperature	Voltage
Commercial	0 to 70°C	3.3V ±10%
Industrial	-40 to 85°C	3.3V ±10%

DC Electrical Characteristics For Commercial Grade Devices

Commercial temperature range: V_{CC} = 3.0V to 3.6V; 0°C < T_{AMB} < 70°C

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IH}	Input high voltage		**2.0**	**5.5**	**V**
V_{IL}	Input low voltage		-0.3	0.8	V
V_{OH}	Output high voltage	I_{OH} = -8 mA	2.4	-	V
V_{OL}	Output low voltage	I_{OL} = 8 mA	-	0.4	V
I_I	Input leakage current	V_I = 0 or 5.5V	-10	10	µA
I_{CCSB}	Standby current	T_{AMB} = 25°C; no output loads, inputsatV_{CC} or V_{SS}.	-	100	µA
C_{IN}	Input capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz	-	10	pF
C_{IO}	I/O capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz	-	10	pF
C_{CLK}	Clock pin capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz	-	12	pF
R_{DONE}	done pull-up resistor	V_{CC} = 3.0V; V_{IN} = 0V	5	20	kΩ
R_{PD}	Unused I/O pull-down resistor	V_{CC} = 3.6V; V_{IN} = V_{CC}	100	400	kΩ
I_{OZH}	Input leakage	V_{IN} = 5.5V or 3.6V	-10	10	µA
I_{OZL}	Input leakage	V_{IN} = 0V	-10	10	µA

AC Electrical Characteristics For Commercial Grade Devices

Commercial temperature range: V_{CC} = 3.0V to 3.6V; 0°C < T_{AMB} < 70°C

Symbol	Parameter	C7		C10		Unit
		Min.	Max.	Min.	Max.	
Timing Requirements						
t_{CL}	Clock LOW time	2.5		3.0		ns
t_{CH}	Clock HIGH time	2.5		3.0		ns
t_{SU_PAL}	PAL setup time (Global clock)	3.0		4.0		ns
t_{SU_PLA}	PLA setup time (Global clock)	4.5		5.5		ns
t_{SU_XOR}	XOR setup time (Global clock)	5.5		6.5		ns
t_H	Hold time (Global clock)		0		0	ns
Output Characteristics						
t_{PD_PAL}	Input to output delay through PAL		7.5		10.0	ns
t_{PD_PLA}	Input to output delay through PLA		9.0		11.5	ns
t_{PD_XOR}	Input to output delay through XOR		10.0		12.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL		4.5		6.0	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PLA		6.0		7.5	ns
t_{PDF_XOR}	Input (or feedback node) to internal feedback node delay time through XOR		7.0		8.5	ns
t_{CF}	Global clock to feedback delay		3.0		3.5	ns
t_{CO}	Global clock to out delay		6.0		7.5	ns
t_{CS}	Clock skew (variance for switching outputs with common global clock)		1.0		1.5	ns
f_{MAX1}	Maximum flip-flop toggle rate: $\left(\frac{1}{t_{CL} + t_{CH}}\right)$	200		166		MHz
f_{MAX2}	Maximum internal frequency: $\left(\frac{1}{t_{SU-PAL} + t_{CF}}\right)$	166		133		MHz
f_{MAX3}	Maximum external frequency: $\left(\frac{1}{t_{SU-PAL} + t_{CO}}\right)$	111		87		MHz
t_{BUFF}	Output buffer delay (fast)		3.0		4.0	ns
t_{SSR}	Slow slew rate incremental delay		5.0		6.0	ns
t_{EA}	Output enable delay		**10.0**		**12.0**	**ns**
t_{ER}	Output disable delay[1]		**10.0**		**12.0**	**ns**
t_{GTSA}	Global 3-state enable		**10.0**		**12.0**	**ns**
t_{GTSR}	Global 3-state disable		**10.0**		**12.0**	**ns**
t_{RR}	Input to register reset		**10.5**		**12.0**	**ns**
t_{RP}	Input to register preset		**9.5**		**11.0**	**ns**
t_{GRR}	Global reset to register reset		**10**		**12.0**	**ns**
t_{GZIA}	Global ZIA delay		**2.0**		**2.5**	**ns**

Note:

1. Output C_L = 5.0 pF.

DC Electrical Characteristics For Industrial Grade Devices

Industrial temperature range: V_{CC} = 3.0V to 3.6V; -40°C < T_{AMB} < 85°C

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IH}	Input high voltage		2.0	5.5	V
V_{IL}	Input low voltage		-0.3	0.8	V
V_{OH}	Output high voltage	I_{OH} = -8 mA	2.4	-	V
V_{OL}	Output low voltage	I_{OL} = 8 mA	-	0.4	V
I_I	Input leakage current	V_I = 0 or 5.5V	-10	10	µA
I_{CCSB}	Standby current	T_{amb} = 25°C; no output loads, inputs at V_{CC} or V_{SS}.	-	100	µA
C_{IN}	Input capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz	-	10	pF
C_{IO}	I/O capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz	-	10	pF
C_{CLK}	Clock pin capacitance	T_{AMB} = 25°C; V_{CC} = 3.3V; f = 1 MHz	-	12	pF
R_{DONE}	done pull-up resistor	V_{CC} = 3.0V; V_{IN} = 0V	5	20	kΩ
R_{PD}	Unused I/O pull-down resistor	V_{CC} = 3.6V; V_{IN} = V_{CC}	100	400	kΩ
I_{OZH}	Input leakage	V_{IN} = 5.5V or 3.6V	-10	10	µA
I_{OZL}	Input leakage	V_{IN} = 0.0 V	-10	10	µA

AC Electrical Characteristics For Industrial Grade Devices

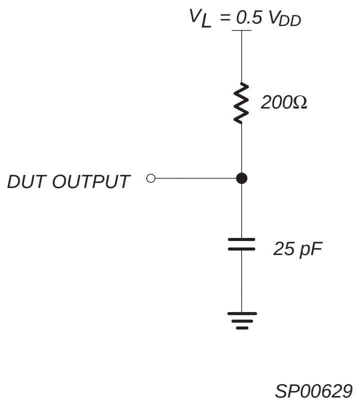
Industrial temperature range: V_{CC} = 3.0V to 3.6V; -40°C < T_{AMB} < 85°C

Symbol	Parameter	N8 Min.	N8 Max.	Unit
Timing Requirements				
t_{CL}	Clock LOW time	2.5		ns
t_{CH}	Clock HIGH time	2.5		ns
t_{SU_PAL}	PAL setup time (Global clock)	3.5		ns
t_{SU_PLA}	PLA setup time (Global clock)	5.0		ns
t_{SU_XOR}	XOR setup time (Global clock)	6.0		ns
t_H	Hold time (Global clock)		0	ns
Output Characteristics				
t_{PD_PAL}	Input to output delay through PAL		8.5	ns
t_{PD_PLA}	Input to output delay through PLA		10	ns
t_{PD_XOR}	Input to output delay through XOR		11	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL		5.0	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PLA		6.5	ns
t_{PDF_XOR}	Input (or feedback node) to internal feedback node delay time through XOR		7.5	ns
t_{CF}	Global clock to feedback delay		3.5	ns
t_{CO}	Global clock to out delay		7.0	ns
t_{CS}	Clock skew (variance for switching outputs with common global clock)		1.0	ns
f_{MAX1}	Maximum flip-flop toggle rate: $\left(\frac{1}{t_{CL} + t_{CH}}\right)$	200		MHz
f_{MAX2}	Maximum internal frequency: $\left(\frac{1}{t_{SU-PAL} + t_{CF}}\right)$	143		MHz
f_{MAX3}	Maximum external frequency: $\left(\frac{1}{t_{SU-PAL} + t_{CO}}\right)$	95		MHz
t_{BUFF}	Output buffer delay (fast)		3.5	ns
t_{SSR}	Slow slew rate incremental delay		5.5	ns
t_{EA}	Output enable delay		11.0	ns
t_{ER}	Output disable delay[1]		11.0	ns
t_{GTSA}	Global 3-state enable		11.0	ns
t_{GTSR}	Global 3-state disable		11.0	ns
t_{RR}	Input to register reset		11.5	ns
t_{RP}	Input to register preset		10.0	ns
t_{GRR}	Global reset to register reset		11	ns
t_{GZIA}	Global ZIA delay		2.5	ns

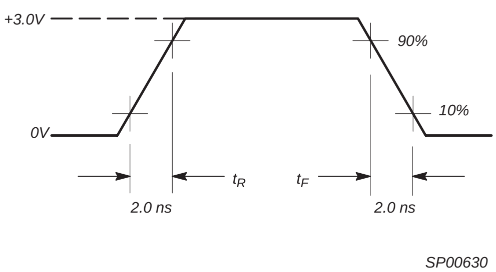
Note:

1. Output C_L = 5.0 pF.

Thevenin Equivalent



Voltage Waveform



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

Device Pin Diagrams

XCR3320 256-pin Plastic BGA

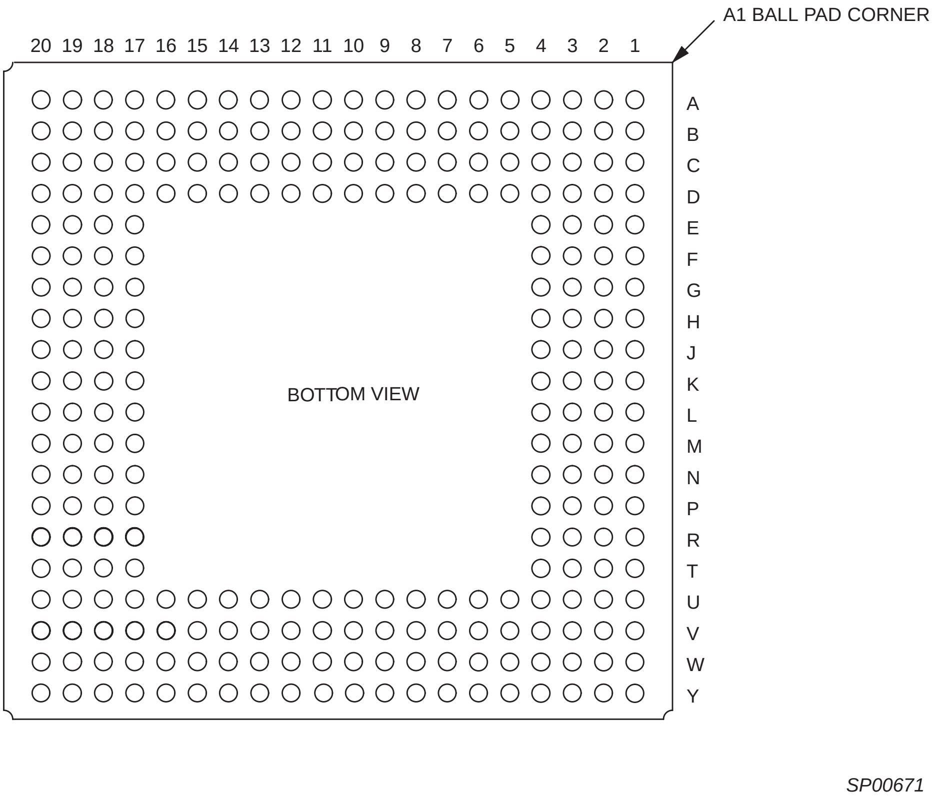


Table 15: 230-pin Function Table

Function is Fast Module_Logic Block_Macrocell. For example, F1_0_56 means Fast Module 1, Logic Block 0, Macrocell 5.

Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball	Function	Pkg Ball
GND	A1	F0_0_9	C1	F0_0_2*	E1	clk_3	L1	F3_2_6*	U1	F3_2_11	W1
F0_2_11	A2	F0_0_10	C2	F0_0_3	E2	gts	L2	F3_2_7	U2	GND	W2
F0_2_9	A3	F0_0_9	C3	F0_0_4*	E3	GND	L3	F3_2_8	U3	F3_0_9	W3
cclk	A4	pgrm	C4	F0_0_5	E4	V_{CC}	L4	GND	U4	tms	W4
F0_2_5*	A5	F0_2_7	C5	F1_2_5	E17	V_{CC}	L17	tdi	U5	F3_0_6	W5
F0_2_2*	A6	F0_2_4	C6	F1_2_4	E18	trstn	L18	V_{CC}	U6	F3_0_3	W6
F0_3_0	A7	F0_2_1	C7	F1_2_3	E19	GND	L19	V_{CC}	U7	F3_0_0*	W7
F0_3_3	A8	F0_3_1	C8	F1_2_2	E20	CLK_7	L20	V_{CC}	U8	F3_1_2	W8
F0_3_6	A9	FO_3_4	C9					GND	U9	F3_1_5	W9
F0_3_9	A10	F0_3_7	C10	F0_1_1	F1	F3_3_11	M1	V_{CC}	U10	F3_1_8	W10
F0_3_10	A11	F1_1_11	C11	F0_1_0*	F2	F3_3_10	M2	V_{CC}	U11	F3_1_11	W11
F1_1_10	A12	F1_1_8	C12	F0_0_0*	F3	F3_3_9	M3	GND	U12	F2_3_9	W12
F1_1_7	A13	F1_1_5*	C13	F0_0_1	F4	GND	M4	V_{CC}	U13	F2_3_6*	W13
F1_1_4	A14	F1_1_2	C14	F1_2_1	F17	GND	M17	V_{CC}	U14	F2_3_3*	W14
F1_1_1	A15	F1_0_0	C15	F1_2_0	F18	F2_1_9	M18	F2_2_6	U15	F2_3_0	W15
F1_0_1	A16	F1_0_3	C16	F1_3_0	F19	F2_1_10	M19	F2_2_8	U16	F2_2_2*	W16
F1_0_4	A17	F1_0_7	C17	F1_3_1	F20	F2_1_11	M19	GND	U17	F2_2_5*	W17
F1_0_8	A18	GND	C18					F2_0_8	U18	F2_2_10	W18
F1_0_10	A19	F1_2_10	C19	F0_1_4*	G1	F3_3_8	N1	F2_0_7	U19	GND	W19
F1_0_11	A20	F1_2_9	C20	F0_1_3*	G2	F3_3_7	N2	F2_0_6*	U20	F2_0_11	W20
				F0_1_2*	G3	F3_3_6	N3				
F0_0_11	B1	F0_0_6*	D1	V_{CC}	G4	F3_3_5	N4	F3_2_9	V1	F3_0_11	Y1
GND	B2	F0_0_7	D2	V_{CC}	G17	F2_1_5*	N17	F3_2_10	V2	F3_0_10	Y2
F0_2_10	B3	F0_0_8	D3	F1_3_2*	G18	F2_1_6	N18	GND	V3	F3_0_8	Y3
resetn	B4	GND	D4	F1_3_3	G19	F2_1_7	N19	tck	V4	tdo	Y4
F0_2_6	B5	F0_2_8	D5	F1_3_4*	G20	F2_1_8	N20	F3_0_7	V5	F3_0_5*	Y5
F0_2_3	B6	done	D6					F3_0_4*	V6	F3_0_2*	Y6
F0_2_0*	B7	V_{CC}	D7	F0_1_8	H1	F3_3_4	P1	F3_0_1	V7	F3_1_0*	Y7
F0_3_2	B8	V_{CC}	D8	F0_1_7	H2	F3_3_3*	P2	F3_1_1	V8	F3_1_3	Y8
F0_3_5	B9	GND	D9	F0_1_6	H3	F3_3_2	P3	F3_1_4*	V9	F3_1_6	Y9
F0_3_8	B10	V_{CC}	D10	F0_1_5	H4	V_{CC}	P4	F3_1_7	V10	F3_1_9	Y10
F0_3_11	B11	V_{CC}	D11	F0_1_5	H17	V_{CC}	P17	F2_3_11	V11	F3_1_10	Y11
F1_1_9	B12	GND	D12	F1_3_6	H18	F2_1_2	P18	F2_3_8	V12	F2_3_10	Y12
F1_1_6*	B13	V_{CC}	D13	F1_3_7	H19	F2_1_3	P19	F2_3_5*	V13	F2_3_7	Y13
F1_1_3	B14	V_{CC}	D14	F1_3_8	H20	F2_1_4	P20	F2_3_2	V14	F2_3_4	Y14
F1_1_0	B15	V_{CC}	D15					F2_2_0*	V15	F2_3_1*	Y15
F1_0_2	B16	F1_0_6	D16	F0_1_11	J1	F3_3_1*	R1	F2_2_3	V16	F2_2_1	Y16
F1_0_5*	B17	GND	D17	F0_1_10	J2	F3_3_0	R2	F2_2_7	V17	F2_2_4	Y17
F1_0_9	B18	F1_2_8	D18	F0_1_9	J3	F3_2_0	R3	GND	V18	F2_2_9	Y18
GND	B19	F1_2_7	D19	GND	J4	F3_2_1*	R4	F2_0_10	V19	F2_2_11	Y19
F1_2_11	B20	F1_2_6*	D20	GND	J17	F2_0_1*	R17	F2_0_9	V20	GND	Y20
				F1_3_9	J18	F2_0_0	R18				
				F1_3_10	J19	F2_1_0	R19				
				F1_3_10	J20	F2_1_1*	R20				
				clk_2	K1	F3_2_2	T1				
				clk_1	K2	F3_2_3*	T2				
				clk_0	K3	F3_2_4	T3				
				V_{CC}	K4	F3_2_5	T4				
				V_{CC}	K17	F2_0_5	T17				
				clk_4	K18	F2_0_4	T18				
				clk_5	K19	F2_0_3*	T19				
				clk_6	K20	F2_0_2	T20				

*Represents multi-function pin

260-pin Description Table

Function is Fast Module_Logic block_Macrocell. For example, F1_0_5 means Fast Module 1, Logic block 0, Macrocell 5.

Table 16: Pin Description

Symbol	Pin Numbers	Type	Description
V_{CC}	D7, D8, D10, D11, D13, D14, D15, G4, G17, K4, K17, L4, L17, P4, P17, U6, U7, U8, U10, U11, U13, U14	-	Positive power supply.
GND	A1, B2, B19, C3, C18, D4, D9, D12, D17, J4, J17, L3, L19, M4, M17, U4, U9, U12, U17, V3, V18, W2, W19, Y20	-	Ground supply.
resetn	B4	I	During configuration, resetn forces the start of initialization. After configuration, resetn is a direct input which can be used to asynchronously reset all the flip-flops. If the global reset is not being used, this pin should be pulled high. If the rise time of the prgmn signal is greater than 1 microsecond, this signal must be held low until prgmn is high.
cclk	A4	I/O	In the master modes, cclk is an output which strobes configuration data in. In the slave or synchronous peripheral mode, cclk is an input synchronous with the data on din or D[7:0]. After configuration, this pin should be pulled low.
done	D6	I/O	done is a bi-directional signal with a weak pull-up resistor attached. As an output, done pulling high indicates configuration is complete. As an input, a low level on done will delay the enabling of user I/O. If only one device is used, this pin can be left floating. If multiple devices are daisy chained, an external pull-up should be used.
prgmn	C4	I	prgmn is an active-low input that forces the restart of configuration and initialization and resets the boundary-scan circuitry. After configuration, the pin should be pulled high. This signal must have a rise time less than 1 microsecond. If the rise time of this signal is greater than 1 microsecond, resetn must be held low until prgmn is high.
spmi	Y5	O	Special purpose configuration pin that must be left floating during configuration for all configuration modes. After configuration the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
mpmi	W13	O	Special purpose configuration pin that must be left floating during configuration for all configuration modes. After configuration the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
din	E1	I	During slave serial or master serial configuration modes, **din** accepts serial configuration data synchronous with cclk. During parallel configuration modes, din is the D[0] input. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
M2	N17	I	**M2/M1/M0** are used to select the configuration mode. After configuration, the pins are user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
M0	G18		
M1	G20		
M3	A6	I	**M3** should be pulled high during configuration for all configuration modes. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.

Table 16: Pin Description (Continued)

Symbol	Pin Numbers	Type	Description
tdi tdo tck tms trstn	U5 Y4 V4 W4 L18	I O I I I	**Test Data In, Test Data Out, Test Clock, Test Mode Select, Test Reset** are dedicated pins for boundary-scan through the JTAG port. If JTAG is not being used, **tdi, tck, tms, and trstn** should be terminated with a weak pull-up resistor. tdo can be left unterminated. See "Terminations" on page 8 for more information.
hdc	B7	O	**High During Configuration (hdc)** is output high when the XCR3320 is in the configuration state. hdc is used as a control output indicating that configuration is in progress. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
ldcn	V9	O	**Low During Configuration (ldcn)** is output low when the XCR3320 is in the configuration state. ldcnis used as a control output indicating that configuration is in progress. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
crcerrn	C13	I/O	**crcerrn** goes Low when the XCR3320 detects a CRC error or an invalid perambleduring configuration. The XCR3320 that detected the error will go into the initialization state and will not resume configuration until prgmn and resetn are both high. Once configuration has resumed crcerrn will go high. During configuration, an internal pull-up is enabled. If only one device is used, this pin can be left floating. If multiple devices are daisy chained, an external pull-up should be used. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
gts	L2	I	**Global 3-state** is an active-High dedicated input used to 3-state the I/Os and activate the internal pull-down resistors. If this feature is not used, the pin should be pulled Low.
cs0n cs1 wrn	B17 W17 B13	I	**cs0n/cs1/wrn** are used in the peripheral configuration mode. The XCR3320 is selected when cs0n and wrn are Low and cs1 is High. After configuration, these pins are user-programmable I/O. cs0N and wrn require no external termination. See "Terminations" on page 8 for more information. If cs1 is not used as an I/O after configuration in synchronous peripheral mode, the 3-state property should be used to disable the internal pull-down resistor. See the section on "Synchronous Peripheral Mode" on page 19 for more information.
A[19:0]	N4, P2, R1, R4, T2, P19, U1, V6, Y6, W7, Y7, V13, W14, Y15, V15, W16, U20, T19, R17, R20	O	In the master parallel configuration mode, **A[19:0]** address the configuration EEPROM. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
D[7:0]	G1, A5, G3, D1, F2, F3, E3, E1	I	During master parallel, peripheral, and slave parallel configuration modes, **D[7:0]** receive configuration data. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
dout	D20	O	During configuration, **dout** is the serial data out that is used to drive the din of daisy-chained slave devices. Data on dout changes on the falling edge of cclk. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.

XCR3320 - 160-Pin Plastic TQFP

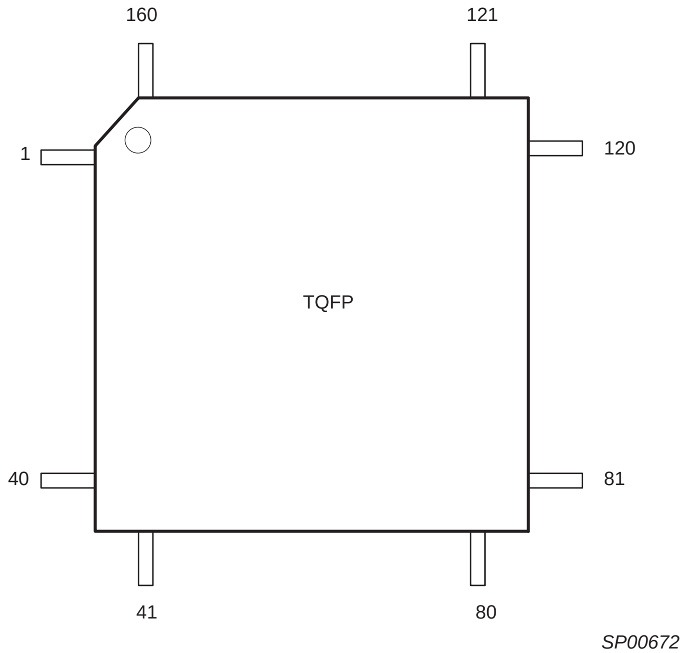


Table 17: 160-pin Function Table

Function is Fast Module_Logic Block_Macrocell. For example, F1_0_5 means Fast Module 1, Logic Block 0, Macrocell 5.

Number	Function	Number	Function	Number	Function	Number	Function
1	F0_0_6*	41	TCK		V_{CC}	121	V_{CC}
2	F0_0_5	42	TDI	82	F2_0_6*	122	F1_0_6
3	F0_0_4*	43	TMS	83	F2_0_5	123	F1_0_5*
4	F0_0_3	44	TDO	84	F2_0_4	124	GND
5	F0_0_2*	45	F3_0_6	85	F2_0_3*	125	F1_0_4
6	F0_0_1	46	F3_0_5*	86	F2_0_2	126	F1_0_3
7	F0_0_0	47	GND	87	F2_0_1*	127	F1_0_2
8	GND	48	F3_0_4*	88	F2_0_0	128	F1_0_1
9	F0_1_0	49	F3_0_3	89	GND	129	F1_0_0
10	F0_1_1	50	F3_0_2*	90	F2_1_0	130	V_{CC}
11	F0_1_2 *	51	F3_0_1	91	F2_1_1*	131	F1_1_0
12	F0_1_3	52	F3_0_0*	92	F2_1_2	132	F1_1_1
13	F0_1_4*	53	V_{CC}	93	F2_1_3*	133	F1_1_2
14	F0_1_5	54	F3_1_0*	94	F2_1_4	134	F1_1_3
15	V_{CC}	55	F3_1_1	95	F2_1_5*	135	F1_1_4
16	F0_1_6	56	F3_1_2	96	F2_1_6	136	F1_1_5*
17	GND	57	F3_1_3	97	TRSTN	137	GND
18	clk_0	58	F3_1_4*	98	GND	138	F1_1_6*
19	clk_1	59	F3_1_5	99	V_{CC}	139	V_{CC}
20	clk_2	60	GND	100	CLK_7	140	F0_3_6
21	clk_3	61	F3_1_6	101	CLK_6	141	GND
22	gts	62	V_{CC}	102	CLK_5	142	F0_3_5
23	V_{CC}	63	F2_3_6*	103	CLK_4	143	F0_3_4
24	GND	64	GND	104	GND	144	F0_3_3
25	F3_3_6	65	F2_3_5*	105	F1_3_6	145	F0_3_2
26	F3_3_5*	66	F2_3_4	106	V_{CC}	146	F0_3_1
27	F3_3_4	67	F2_3_4*	107	F1_3_5	147	F0_3_0
28	F3_3_3*	68	F2_3_2	108	F1_3_4*	148	V_{CC}
29	F3_3_2	69	F2_3_1*	109	F1_3_3	149	F0_2_0*
30	F3_3_1*	70	F2_3_0	110	F1_3_2*	150	F0_2_1
31	F3_3_0	71	V_{CC}	111	F1_3_1	151	F0_2_2*
32	GND	72	F2_2_0*	112	F1_3_0	152	F0_2_3
33	F3_2_0	73	F2_2_1	113	GND	153	F0_2_4
34	F3_2_1*	74	F2_2_2*	114	F1_2_0	154	GND
35	F3_2_2	75	F2_2_3	115	F1_2_1	155	F0_2_5*
36	F3_2_3*	76	F2_2_4	116	F1_2_2	156	F0_2_6
37	F3_2_4	77	GND	117	F1_2_3	157	CCLK
38	F3_2_5	78	F2_2_5*	118	F1_2_4	158	DONE
39	F3_2_6*	79	F2_2_6	119	F1_2_5	159	RESETN
40	V_{CC}	80	V_{CC}	120	F1_2_6*	160	PGRM

*Represents multi-function pins

160 Pin Description Table

Function is Fast Module_Logic block_Macrocell. For example, F1_0_5 means Fast Module 1, Logic block 0, Macrocell 5.

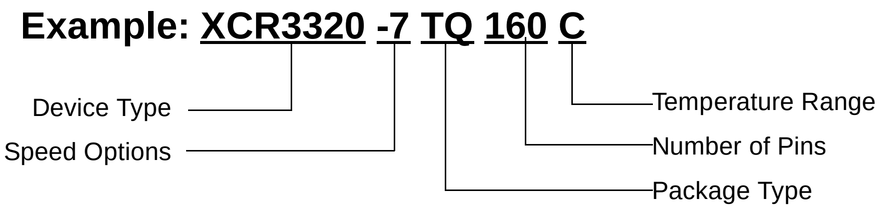
Table 18: Pin Function Description

Symbol	Pin Number	Type	Description
V_{CC}	15, 23, 40, 53, 62, 71, 80, 81, 99, 106, 121, 130, 139, 148	-	Positive power supply.
GND	8, 17, 24, 32, 47, 60, 64, 77, 89, 98, 104, 113, 124, 137, 141, 154	-	Ground supply.
resetn	159	I	During configuration, **resetn** forces the start of initialization. After configuration, resetn is a direct input which can be used to asynchronously reset all the flip-flops. If the global reset is not being used, this pin should be pulled High. If the rise time of the prgmn signal is greater than 1 µs, this signal must be held low until prgmn is High.
cclk	157	I/O	In the master modes, **cclk** is an output which strobes configuration data in. In the slave or synchronous peripheral mode, cclk is an input synchronous with the data on din or D[7:0]. After configuration, this pin should be pulled Low.
done	158	I/O	**done** is a bi-directional signal with a weak pull-up resistor attached. As an output, done pulling High indicates configuration is complete. As an input, a Low level on done will delay the enabling of user I/O. If only one device is used, this pin can be left floating. If multiple devices are daisy chained, an external pull-up should be used.
prgmn	160	I	**prgmn** is an active-low input that forces the restart of configuration and initialization and resets the boundary-scan circuitry. After configuration, the pin should be pulled high. This signal must have a rise time less than 1 microsecond. If the rise time of this signal is greater than 1 microsecond, resetn must be held low until prgmn is high.
spmi	46	O	Special purpose configuration pin that must be left floating during configuration for all configuration modes. After configuration the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
mpmi	63	O	Special purpose configuration pin that must be left floating during configuration for all configuration modes. After configuration the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
din	5	I	During slave serial or master serial configuration modes, **din** accepts serial configuration data synchronous with cclk. During parallel configuration modes, din is the D[0] input. After configuration, the pin is a user-programmable I/O, and no external termination is required. See the section on terminations for more information.
M2	95	I	**M2/M1/M0** are used to select the configuration mode. After configuration, the pins are user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
M0	110		
M1	108		
M3	151	I	**M3** should be pulled high during configuration for all configuration modes. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
tdi tdo tck tms trstn	42 44 41 43 97	I O I I I	**Test Data In, Test Data Out, Test Clock, Test Mode Select, Test Reset** are dedicated pins for boundary-scan through the JTAG port. If JTAG is not being used, tdi, tck, tms, and trstn should be terminated with a weak pull-up resistor. tdo can be left unterminated. See "Terminations" on page 8 for more information.

Table 18: Pin Function Description (Continued)

Symbol	Pin Number	Type	Description
hdc	149	O	**High During Configuration (hdc)** is output high when the XCR3320 is in the configuration state. hdc is used as a control output indicating that configuration is in progress. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
ldcn	58	O	**Low During Configuration (ldcn)** is output low when the XCR3320 is in the configuration state. ldcnis used as a control output indicating that configuration is in progress. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
crcerrn	136	I/O	**crcerrn** goes Low when the XCR3320 detects a CRC error or an invalid perامble during configuration. The XCR3320 that detected the error will go into the initialization state and will not resume configuration until prgmn and resetn are both High. Once configuration has resumed crcerrn will go High. During configuration, an internal pull-up is enabled. If only one device is used, this pin can be left floating. If multiple devices are daisy chained, an external pull-up should be used. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
gts	22	I	**Global 3-state** is an active-high dedicated input used to 3-state the I/Os and activate the internal pull-down resistors. If this feature is not used, the pin should be pulled Low.
cs0n cs1 wrn	123 78 138	I	**cs0n/cs1/wrn** are used in the peripheral configuration mode. The XCR3320 is selected when cs0n and wrn are Low and cs1 is High. After configuration, these pins are user-programmable I/O. cs0N and wrn require no external termination. See "Terminations" on page 8for more information. If cs1 is not used as an I/O after configuration in synchronous peripheral mode, the 3-state property should be used to disable the internal pull-down resistor. See "Synchronous Peripheral Mode" on page 19 for more information.
A[19:0]	26, 28, 30, 34, 36, 93, 39, 48, 50, 52, 54, 65, 67, 69, 72, 74, 82, 85, 87, 91	O	In the master parallel configuration mode, **A[19:0]** address the configuration EEPROM. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
D[7:0]	13, 155, 11, 1, 9, 7, 3, 5	I	During master parallel, peripheral, and slave parallel configuration modes, **D[7:0]** receive configuration data. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.
dout	120	O	During configuration, **dout** is the serial data out that is used to drive the din of daisy-chained slave devices. Data on dout changes on the falling edge of cclk. After configuration, the pin is a user-programmable I/O, and no external termination is required. See "Terminations" on page 8 for more information.

Ordering Information



Speed Options
-10: 10 ns pin-to-pin delay
-8: 8 ns pin-to-pin delay
-7: 7.5 ns pin-to-pin delay

Temperature Range
C = Commercial, T_A = 0°C to +70°C
I = Industrial, T_A = –40°C to +85°C

Packaging Options
TQ160: 160-pin TQFP
BG256: 256-ball BGA

Component Availability

Pins		160	256
Type		Plastic TQFP	Plastic BGA
Code		TQ160	BG256
XCR3320	-10	C	C
	-8	I	I
	-7	C	C

Revision Table

Date	Version #	Revision
8/19/99	1.0	Initial Xilinx release.
2/10/00	1.1	Converted to Xilinx Format and updated.
8/10/00	1.2	Updated Ordering Information: changed TQ144 to TQ160 Pakage Options.
10/9/00	1.3	Added Discontinuation Notice.