FAIRCHILD
SEMICONDUCTOR™

74ALVCH162240
Low Voltage 16-Bit Inverting Buffer/Line Driver with Bushold and 26Ω Series Resistors in Outputs

General Description

The ALVCH162240 contains sixteen inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The ALVCH162240 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

The 74ALVCH162240 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVCH162240 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with output capability up to 3.6V.

The 74ALVCH162240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features
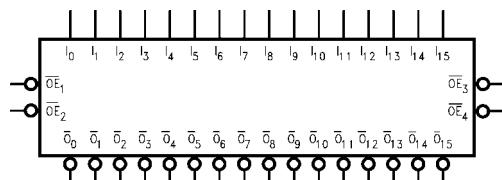
- 1.65V to 3.6V V_{CC} supply operation
- 3.6V tolerant control inputs and outputs
- Bushold on data inputs eliminating the need for external pull-up/pull-down resistors
- 26Ω series resistors in outputs
- t_{PD}
  - 3.8 ns max for 3.0V to 3.6V V_{CC}
  - 4.3 ns max for 2.3V to 2.7V V_{CC}
  - 7.6 ns max for 1.65V to 1.95V V_{CC}
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

Ordering Code:

Order Number	Package Number	Package Descriptions
74ALVCH162240T	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
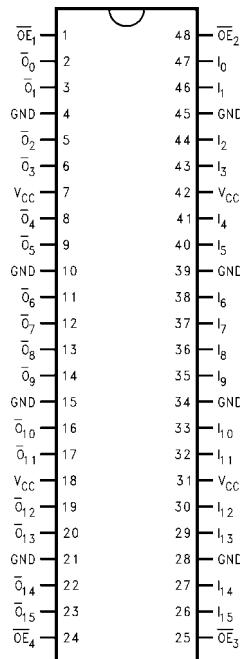
Logic Symbol

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0–I_{15}	Bushold Inputs
$\overline{O}_0$–$\overline{O}_{15}$	Outputs

74ALVCH162240

Connection Diagram

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         ┌───────┐
 OE₁ ──│ 1   48 │── OE₂
  O₀ ──│ 2   47 │── I₀
  O₁ ──│ 3   46 │── I₁
 GND ──│ 4   45 │── GND
  O₂ ──│ 5   44 │── I₂
  O₃ ──│ 6   43 │── I₃
 VCC ──│ 7   42 │── VCC
  O₄ ──│ 8   41 │── I₄
  O₅ ──│ 9   40 │── I₅
 GND ──│ 10  39 │── GND
  O₆ ──│ 11  38 │── I₆
  O₇ ──│ 12  37 │── I₇
  O₈ ──│ 13  36 │── I₈
  O₉ ──│ 14  35 │── I₉
 GND ──│ 15  34 │── GND
 O₁₀ ──│ 16  33 │── I₁₀
 O₁₁ ──│ 17  32 │── I₁₁
 VCC ──│ 18  31 │── VCC
 O₁₂ ──│ 19  30 │── I₁₂
 O₁₃ ──│ 20  29 │── I₁₃
 GND ──│ 21  28 │── GND
 O₁₄ ──│ 22  27 │── I₁₄
 O₁₅ ──│ 23  26 │── I₁₅
 OE₄ ──│ 24  25 │── OE₃
         └───────┘
```

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

| Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance
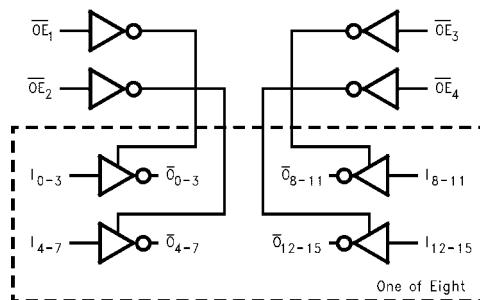
Functional Description

The 74ALVCH162240 contains sixteen inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagram

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O) (Note 2)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V_{CC}		
			2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		1.65 - 1.95		0.35 x V_{CC}	
			2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 μA	1.65 - 3.6	V_{CC} - 0.2		
		I_{OH} = −2 mA	1.65	1.2		
		I_{OH} = −4 mA	2.3	1.9		
		I_{OH} = −6 mA	2.3	1.7		V
			3	2.4		
		I_{OH} = −8 mA	2.7	2		
		I_{OH} = −12 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 μA	1.65 - 3.6		0.2	
		I_{OL} = 2 mA	1.65		0.45	
		I_{OL} = 4 mA	2.3		0.4	
		I_{OL} = 6 mA	2.3		0.55	V
			3		0.55	
		I_{OL} = 8 mA	2.7		0.6	
		I_{OL} = 12 mA	3		0.8	
I_I	Input Leakage Current	$0 \le V_I \le 3.6V$	3.6		±5.0	μA
$I_{I(HOLD)}$	Bushold Input Minimum Drive Hold Current	V_{IN} = 0.58V	1.65	25		
		V_{IN} = 1.07V	1.65	−25		
		V_{IN} = 0.7V	2.3	45		
		V_{IN} = 1.7V	2.3	−45		μA
		V_{IN} = 0.8V	3.0	75		
		V_{IN} = 2.0V	3.0	−75		
		$0 < V_O \le 3.6V$	3.6		±500	
I_{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$	3.6		±10	μA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC}$ − 0.6V	3 - 3.6		750	μA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$								Units
		$C_L = 50$ pF				$C_L = 30$ pF				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay	1.3	3.8	1.5	4.3	1.0	3.8	1.5	7.6	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.3	4.3	1.5	5.6	1.0	5.1	1.5	9.8	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.3	4.1	1.5	4.5	1.0	4.0	1.5	7.2	ns

Capacitance

Symbol	Parameter	Conditions		$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance	$V_I = 0V$ or V_{CC}		3.3	6	pF
C_{OUT}	Output Capacitance	$V_I = 0V$ or V_{CC}		3.3	7	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	$f = 10$ MHz, $C_L = 50$ pF	3.3	20	pF
				2.5	20	

AC Loading and Waveforms
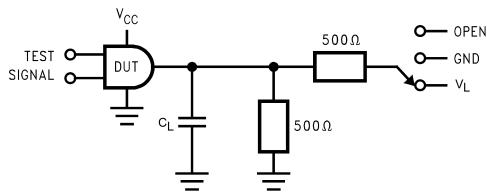
FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: f = 1MHz; t_r = t_f = 2ns; Z_0 = 50Ω

Symbol	V_{CC}			
	3.3V $\pm$ 0.3V	2.7V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$
V_L	6V	6V	$V_{CC}*2$	$V_{CC}*2$
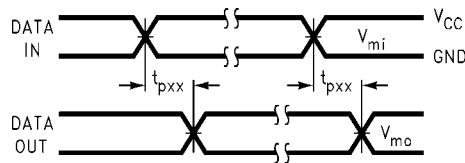
FIGURE 2. Waveform for Inverting and Non-Inverting Functions
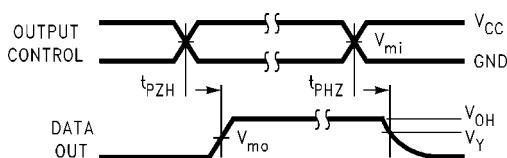
**FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**
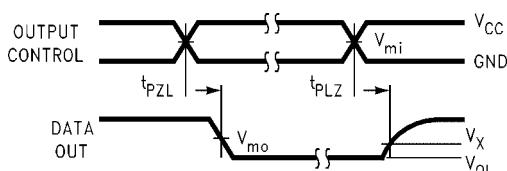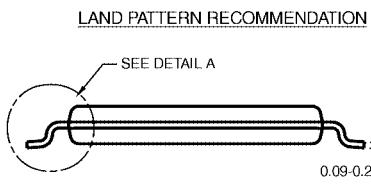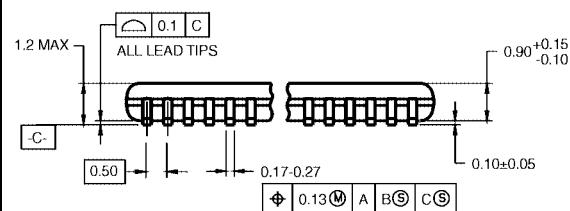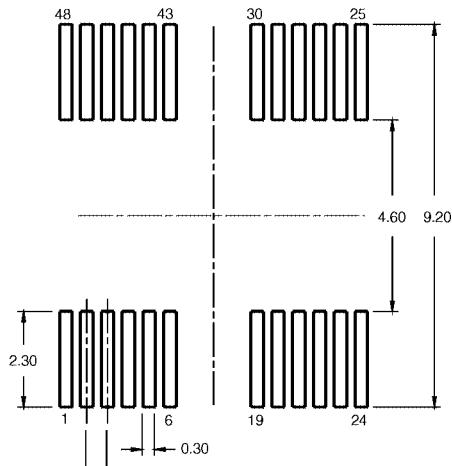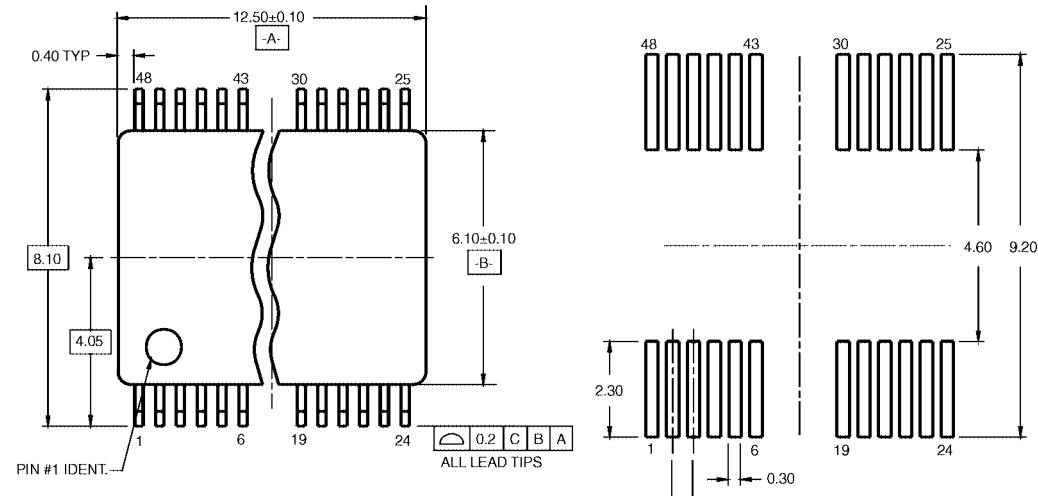
**FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**

Physical Dimensions inches (millimeters) unless otherwise noted

12.50±0.10
-A-

0.40 TYP

48 43 30 25

8.10

4.05

6.10±0.10
-B-

1 6 19 24

PIN #1 IDENT.

| △ | 0.2 | C | B | A |
ALL LEAD TIPS

| △ | 0.1 | C |
ALL LEAD TIPS

1.2 MAX

-C-

0.50   0.17-0.27

0.90 +0.15 -0.10

0.10±0.05

| ⊕ | 0.13 Ⓜ | A | B Ⓢ | C Ⓢ |
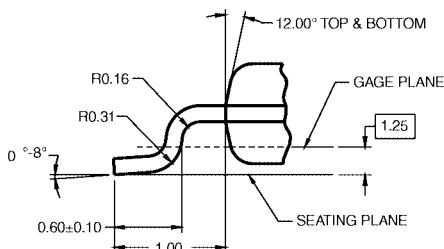
DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

LAND PATTERN RECOMMENDATION

48 43 30 25

4.60   9.20

2.30

1 6 19 24

0.30

0.50

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTOM

R0.16

R0.31

GAGE PLANE

1.25

0°-8°

0.60±0.10

1.00

SEATING PLANE

DETAIL A

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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